PROJECT
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TITLE
Radiation Pre-Evaluation of Actel FPGA RT54SX32-S

EUROPEAN SPACE AGENCY
CONTRACT REPORT

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SUMMARY

This report presents the results from Heavy Ion test of Actel FPGA RT54SX-S manufactured by Matsushita (MEC) in a 0.25µm technology.

No SEU in the R- register cells have been observed under static conditions up to LET= 64.5 MeV/mg/cm^2. In GEO orbit using CREME96 the R-register upset rate is calculated to be less than $2 \cdot 10^{-16}$ errors/device/day.

Irradiation with heavy ions under 5 MHz dynamic condition resulted in errors which had the same signature as if they were proper SEU. When lowering the FPGA operating frequency by a factor of 4 to 1.25 MHz no errors could be observed. The errors observed in 5 MHz dynamic mode are very likely due to transient effects which are clocked through to the output.

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Changes between issues are marked with a left-bar.

Issue	Date	Paragraphs affected	Change information
1	27 Sept 2001	All	New document

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1. INTRODUCTION

This report presents the results from Heavy Ion test of Actel FPGA RT54SX-S manufactured by Matsushita (MEC) in a 0.25µm technology.

2. RT54SX-S DETAILS

The architecture of Actel's RT54SX-S devices is an enhanced version of Actel's SX-A device architecture. The RT54SX-S devices are manufactured using a 0.25µm technology at the Matsushita (MEC) facility. The RT54SX-S family incorporates up to four layers of metal interconnects.

To achieve good SEU requirements each register cell (R-Cell) in the RT54SX-S are build up with Triple Module Redundancy (TMR) (Figure 2.1)
The R-cells in the SX-S devices consists of three master and three slave latches gated by opposite edges of the clock. The feedback path of each of the three latches is voted with the outputs of the other two latches. If one of the three latches is struck by an ion and starts to change state, the voting with the other two latches prevents the change from feeding back and permanently latching.
With this solution the latches is continuously corrected and theoretically the only possibility for a SEU in a R- register is to have two latches hit by two ions within the recovery time of the transient created by the ions.

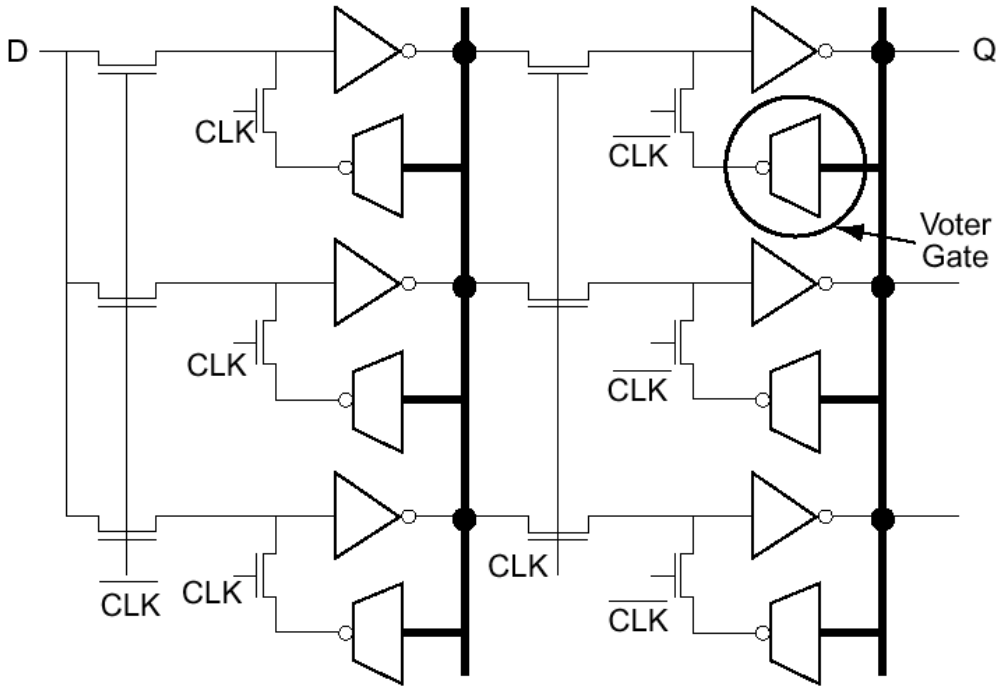

Figure 2.1 Schematic picture of R-Cell in RT54SX-S with tripled master and slave latches and voted feedback.

3. TEST SAMPLES

Two RT54SX32S from the same wafer lot were used as test samples, both in 256 pin ceramic flat package. The devices were serialised as S/N 01 and S/N 02.

Delidded samples were used for SEE tests. The chip surface was covered with coat measured to be about 10 µm thick. The coat was not removed before irradiation tests.

ACTEL PART #	:	RT54SX32S-CQ256BPE60
WAFER LOT #	:	T25JSP03A
DATE CODE	:	0043

Marking / *Top side*	Marking / *Bottom Side*
ESD-logo QML	T25JSP03A
Actel Logo	004
RT54SX32S	USA
CQ256B 0043	

4. TEST TECHNIQUES

4.1 General

The general concept is to load data into the DUT, pause for a pre-set time and thereafter read data and check for errors. New data are loaded into the DUT at the same time as old are read out. All this is repeated continuously during irradiation. With long pause time the DUT is tested in static condition and by setting the pause time to zero the DUT is tested in dynamic condition.

A flow chart of the test sequence is given in Fig 4.1.1. Any detected errors will be stored in FIFO's, and the DUT will be loaded with new data again. The cycle will then be repeated. Failing read/write operations from/to the DUT will determine the functionality. The clock speed is variable up to 5 MHz. Error Data are serially transferred from the FIFO to a PC where data are analyzed. For each DUT, errors can be traced down to logic module, logic value and position.

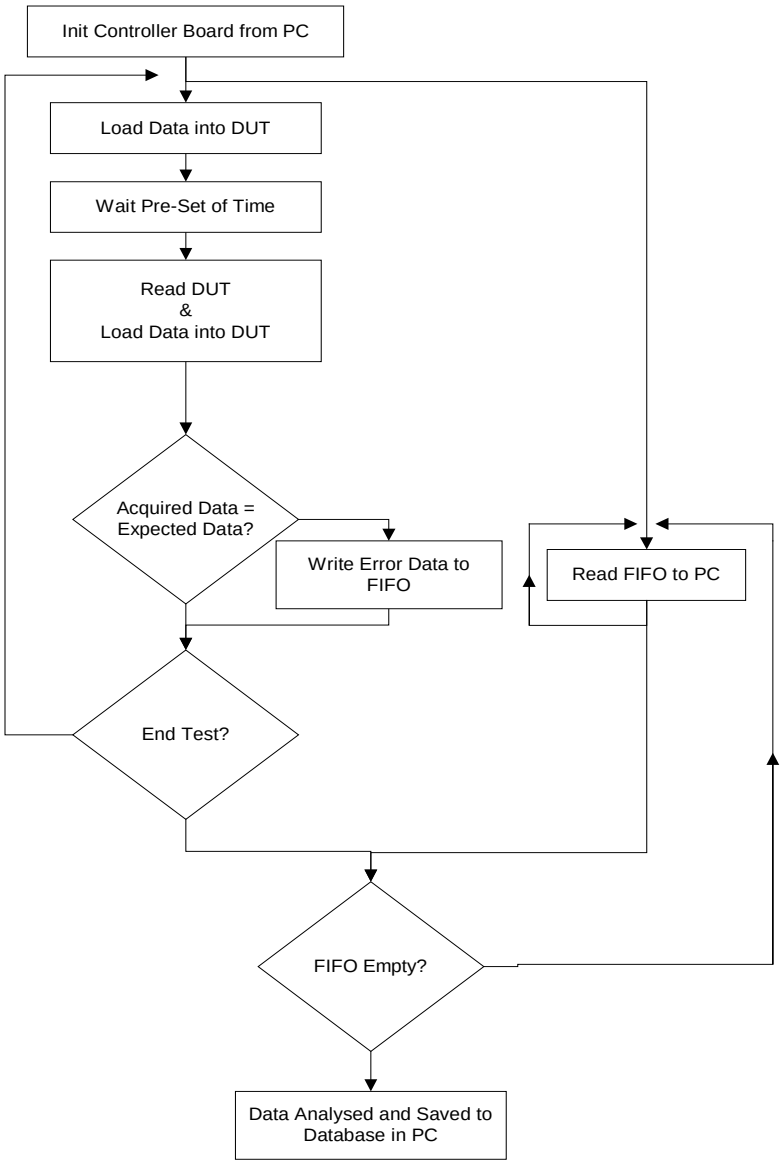

Fig 4.1.1 Flow chart of the test sequence.

4.2 Test Boards

The test system consist of two boards, one Controller board managing the test sequence and the serial interface to the PC and one DUT board housing two Devices Under Test (DUT). A principal drawing is given in Fig 4.2.1 .

The Controller board tests one DUT at a time using a "virtual golden chip" test method. The principal of the measuring technique is to compare each output from the DUT with the correct data stored in SRAM's. The general concept of the error detection and test sequence is shown in Fig 4.1.1. The DUT is continually cycled while the outputs of selected ring counters are compared with the "golden chip". When an error is detected (when outputs do not match), the state of all outputs and position in cycle of the failing ring counter will be temporarily stored in FIFO's. Data in the FIFO's is continually send to a PC through a RS232 serial interface. After each test run the data are analyzed and stored in a database by the controlling PC.

The controller board also control the power supply for the DUT's by relays and send status signals to a Data Logger connected to the board.

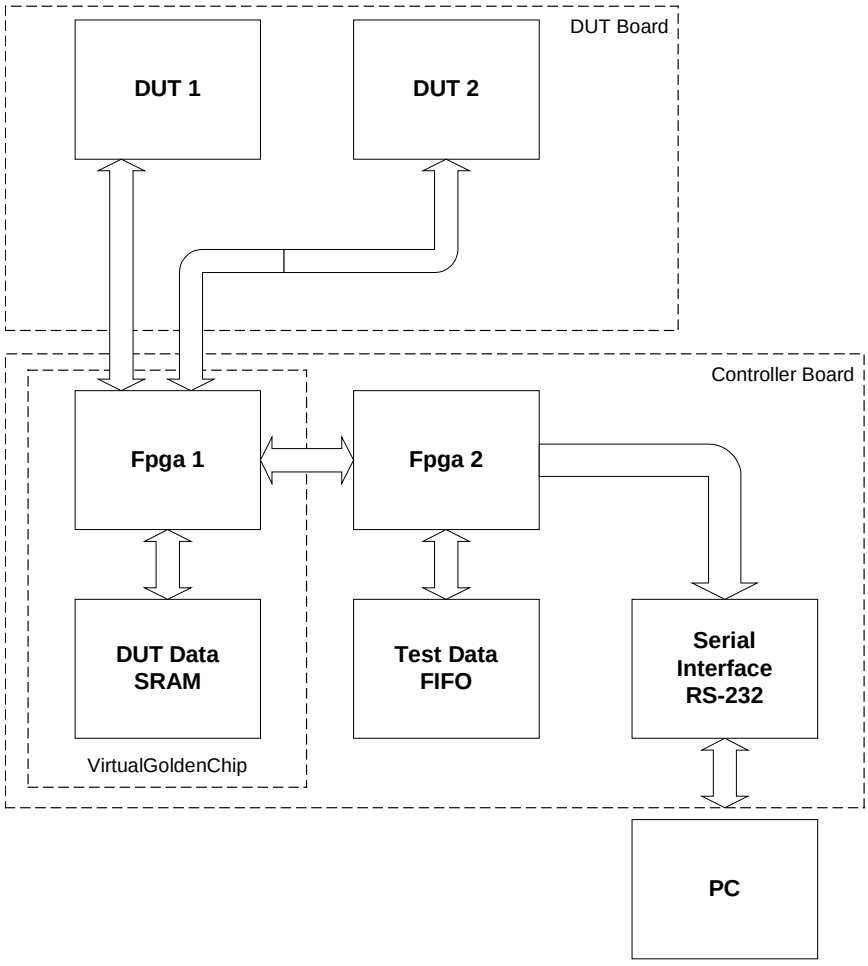

Fig 4.2.1 Principal drawing of DUT board and Controller Board

4.3 DUT Test Program Layout

The DUT's have been programmed with eight parallel shift registers, each register consist of "128 bit" of TMR R-cells. This design use up 95% of available register cells in the FPGA..

The two devices were programmed at Actel/USA with the Saab Ericsson DUT design , using the "Sculpture programmer". The used Actel programming S/W was at the time not a released and qualified S/W.

4.4 Test Conditions

The bias condition was 2.5Volt for the array (V_{CCA}) and 3.3Volt for the I/Os (V_{CCI}).

Heavy ion irradiations have been performed under both static condition and 5 MHz dynamic and 1.25 MHz dynamic conditions, where data are continuously clocked through the registers. In all tests checkerboard data are loaded into the shift registers.

4.4.1 Static Condition

Between each load and read/check of the 128-bit shift registers the DUT is paused for one second, while the frequency for clocking data in and out was 5 MHz.

4.4.2 Static Inverted Clock Condition

This test is performed exactly as the Static test but the clock signal into the DUT has been inverted. This means that during the time the DUT is paused the clock signal is high instead of low. Thus, the data are stored in the master latch instead of the slave latch in the register cell. The aim of the test was to verify any difference between the master and slave latch.

4.4.3 5 MHz Dynamic Condition

The pause between load and read/check of the 128-bit shift registers was set to zero. Checkerboard data are thus continuously loaded into the shift registers with 5 MHz. Compared to the Static test each shift register was clocked and read/checked $4 \cdot 10^4$ times more in this mode.

4.4.4 1.25 MHz Dynamic Condition

This test is performed exactly as 5 MHz Dynamic but with 4 times lower frequency, in order to verify the relation between error rate and dynamic test frequency.

5. SEE RESULTS

No tests with ^{252}Cf has been performed due to the fact that the this device type had a 10 μm coating layer on top of the four metal layers and the low penetration depth of the fission fragments.

Single Event Effects tests have been performed at the Heavy Ion Facility in UCL, Belgium.
The Single Event Upset results are presented in graphical form in Fig 6.1. Individual results from all measurements including the used ion beam and fluences are given in Table 6.1

In neither of the two static test modes could any SEU be the detected. The results indicate a cross section for SEU less than 10^{-10} cm^2/bit.

In the 5 MHz dynamic test mode a few upsets were detected. The error data events were found to be evenly spread over time and all 8 shift registers. It seems to be no polarisation between logic high and low errors.
The comparison of the shift register data takes place 50 ns after the data are clocked out.

In the 1.25 MHz dynamic test mode no upsets were detected. With the tested fluence and a linear relation of errors to the test frequency, two to three errors were expected in this run.

The static tests indicate that the TMR register cells have a LET threshold for SEU, which is larger then 65 MeV/mg/cm^2.

The observed errors in the dynamic tests are likely due to glitches descending from transients at ion hits. From the current test set-up it is not possible to determine where the transient errors occur. The test data indicate a LET threshold between 20 and 34 MeV/mg/cm^2 for the transient errors.

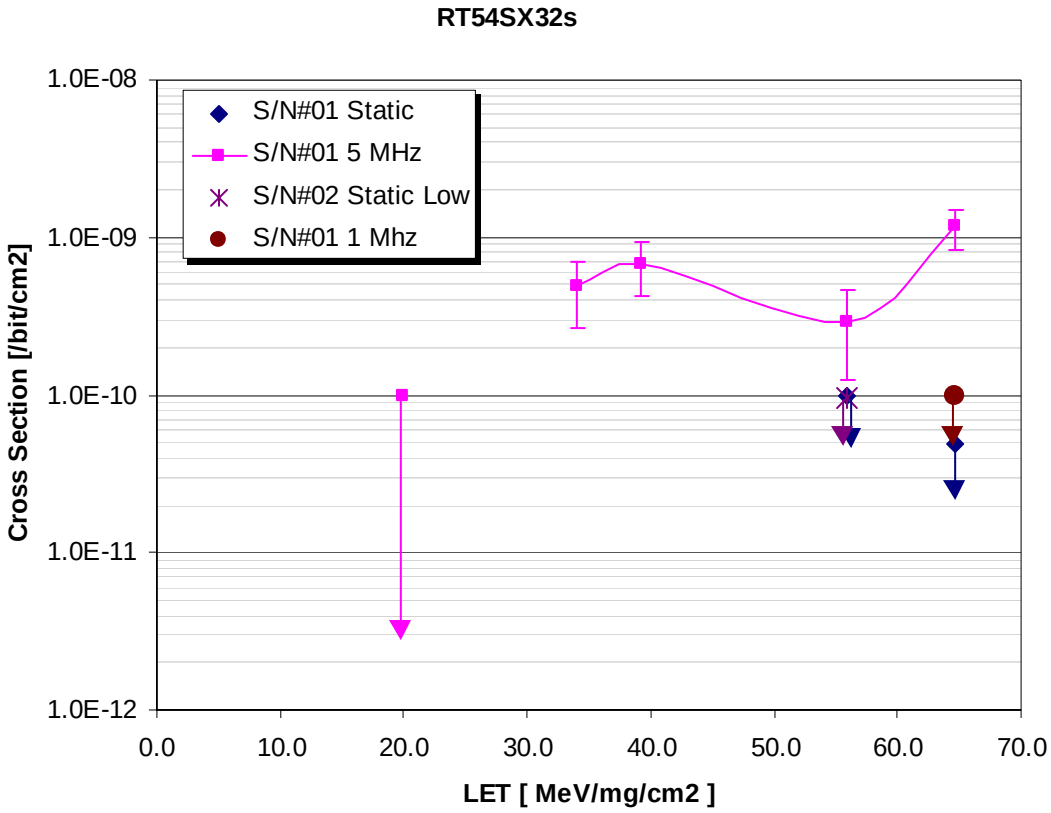

Fig 5.1 *Single Event Upset cross section as a function of LET value for RT54SX32S. Errors have only been detected in the 5 MHz dynamic test mode. The data points with arrows indicate fluence for test run without errors. The error bars are the standard deviation indicating counting statistics for each test run.*

Table 5.1 *Summary of data for all performed test runs at RT54SX32S.*

Test Run	Fluence	Mean Flux	Ion	Tilt	LET_{eff}	DUT	Number of Errors			Cross Section	Test Mode
#	Ions/cm^2	Ions/cm^2•s		degree	MeV•mg/cm^2	Sn#	Sum	0-1*	1-0*	cm^2/bit	
1	1.0E+06	6764	Xe	0°	55.9	01	0	0	0	<9.8E-10	Static
2	1.0E+07	7593	Xe	0°	55.9	01	0	0	0	<9.8E-11	Static
3	1.0E+07	8557	Xe	0°	55.9	01	3	1	2	2.9E-10	5 MHz Dynamic
4	1.0E+07	12941	Xe	0°	55.9	02	0	0	0	<9.8E-11	Static Inverted Clock
5	2.0E+07	5610	Xe	30°	64.58	01	0	0	0	<4.9E-11	Static
6	1.0E+07	7824	Xe	30°	64.58	01	12	3	9	1.2E-09	5 MHz Dynamic
7	1.0E+07	10312	Xe	30°	64.58	01	0	0	0	<9.8E-11	1.25 MHz Dynamic
11	1.0E+07	9368	Kr	30°	39.26	01	7	4	3	6.8E-10	5 MHz Dynamic
12	1.0E+07	11469	Kr	0°	34	01	5	2	3	4.9E-10	5 MHz Dynamic
13	1.0E+07	7000	Ar	45°	19.9	01	0	0	0	<9.8E-11	5 MHz Dynamic

*0-1 is number of errors when logic one was read but logic low was expected. 1-0 is the reverse case.

6. CONCLUSION

No SEU in the R- register cells have been observed under static conditions up to LET= 64.5 MeV/mg/cm^2. In GEO orbit using CREME96 the R-register upset rate is calculated to be less than 2e-16 errors/device/day.

Irradiation with heavy ions under 5 MHz dynamic condition resulted in errors which had the same signature as if they were proper SEU. When lowering the FPGA operating frequency by a factor of 4 to 1.25 MHz no errors could be observed. From the static condition test it was concluded that the R-cells do not upset. Thus, the errors observed in 5 MHz dynamic mode are very likely due to transient effects which are clocked through to the output.
Heavy ion induced transients are known to occur in many technologies. The duration and magnitude of the transients are, however, technology and circuitry design dependent. In the present experimental set-up it is not possible to isolate the error data to certain areas or functions of the device.
The present results with no errors at 1.25 MHz and about 10 events at 5 MHz (for a fluence of $1 \cdot 10^7$ cm^{-2} Xenon ions) rise the question what will happen at mission relevant operating frequencies.

With a LET threshold for transients at LET=34 MeV/mg/cm^2 value, the error rate for GEO has been calculated with CREME96 to be $7 \cdot 10^{-14}$ errors/device/day. This estimated error rate is design- and frequency specific and are valid for a device operating at 5 MHz using only R-register resources. The sensitivity of C-modules has not been tested.