ESA-QCA0007S-C

HIREL EXPERTISE
HIREX
ENGINEERING

RADIATION TEST REPORT

Heavy Ions Testing of

LM139J

Quad Voltage Comparator

from National Semiconductor

ESA Purchase Order No 181635 dated 13/08/98

European Space Agency Contract Report

The work described in this report was done under ESA contract.
Responsibility for the contents resides in the author or organization that prepared it

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Date : October 29, 1998

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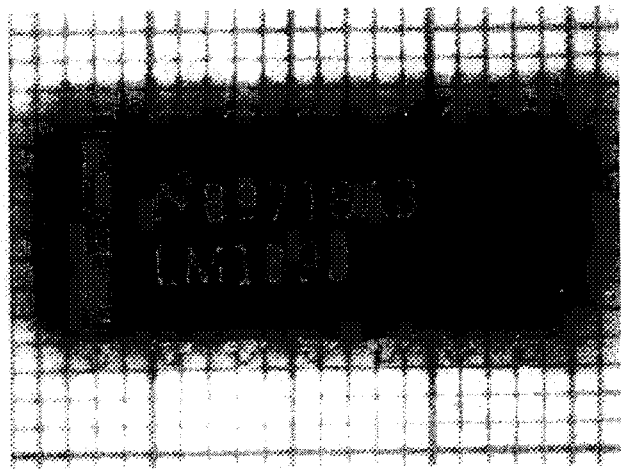
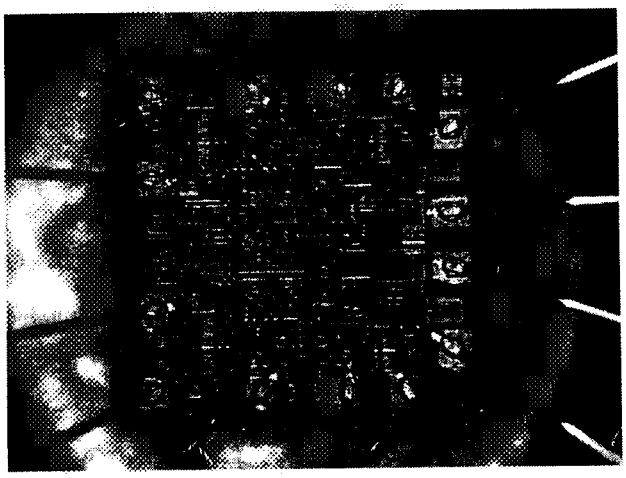
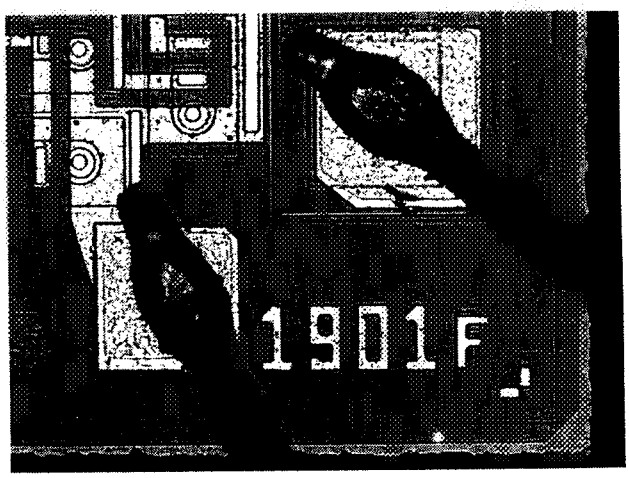






IV. DEVICE TEST PATTERN DEFINITION

IV.1 PREPARATION OF TEST HARDWARE AND PROGRAM

Overall device emulation, SEU and Latch-up detection, data storage and processing were implemented using an in-house test hardware and an application specific test board.

The generic in-house test equipment is driven by a PC computer through a RS232 line. All power supplies and input signals are delivered and monitored by the in-house equipment which also stores in its memory the output data from the device throughout the specific test board.

The application specific test board allowed to interface the standard test hardware with the device under test, in order to correctly emulate the relevant part, to record all the different type of errors during the irradiation and to set output signal for processing and storage by the standard test equipment.

At the end of each test run, data are transferred to the PC computer through the RS232 link for storage on hard disk or floppies.

IV.2 GENERIC TEST SET-UP

The complete test equipment is constituted of:

- A PC computer (to configure and interface with the test system and store the data),
- An electronic rack with the instrumentation functions provided by a set of electronic modules,
- A mother board under vacuum which allows for the sequential test of up to 4 devices
- A digital oscilloscope to store analog upset waveform

Generic device test set-up is presented in Figure IV-1.

IV.2.1 Mother board description (ref. IL110)

The motherboard acts as a standard interface between each DUT test board and the control unit :
For each DUT board slot , the following signals can be considered:

- 8 inputs signals
  - 4 programmable power supplies
  - 4 programmable clocks
- 8 output signals
  - 4 logic counting signals
  - 2 fast analog signals
  - 2 accurate analog signals

- Each device needs a dedicated plug-in test board compatible with IL110 mother board.
- IL110 board has been designed to comply with Louvain Test facilities .
- The number of slots is limited to four

Operation is multiplexed and only one slot is powered at one time.

Mother board synoptic is shown in Figure IV-2.

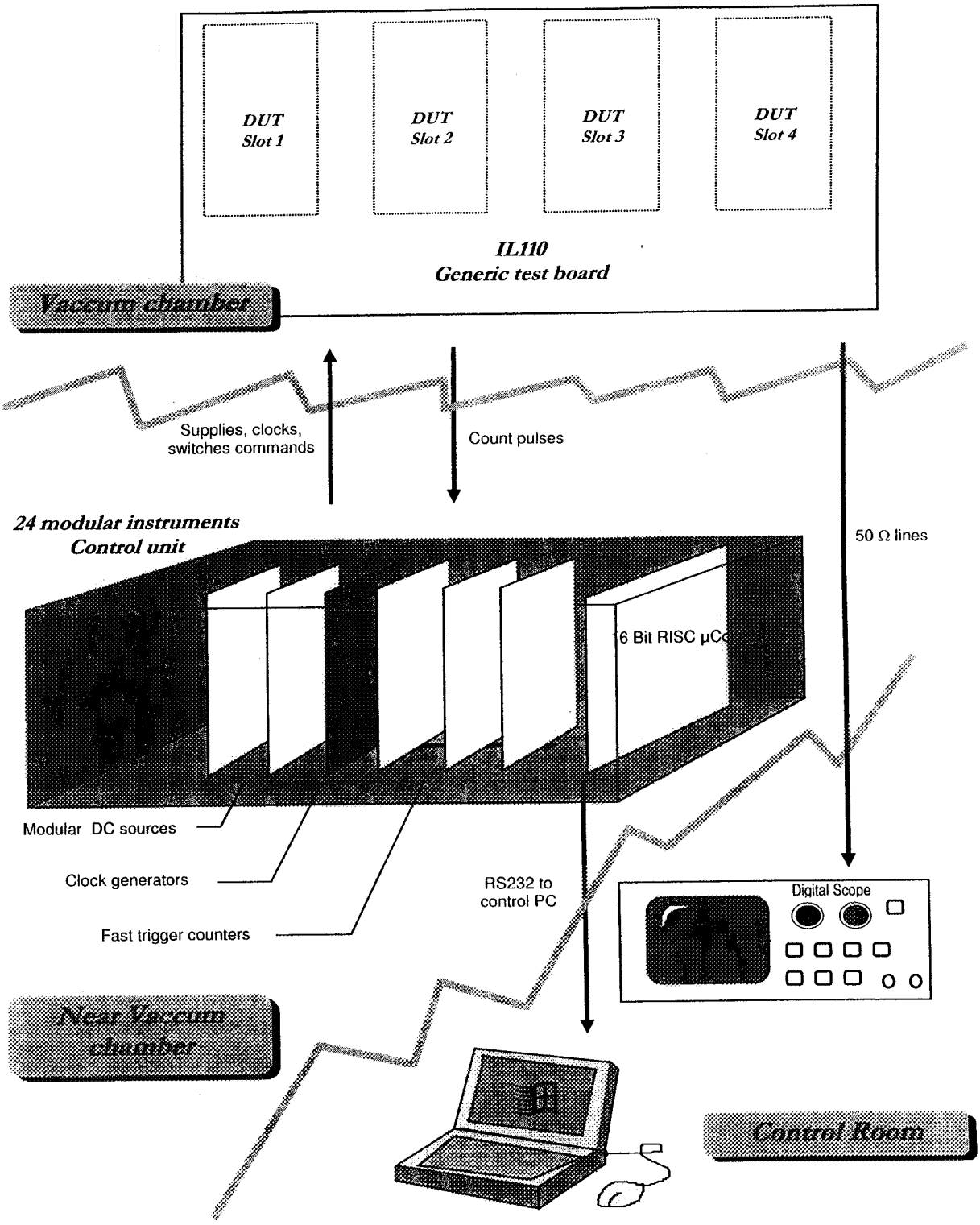


Figure IV-1 - Generic Device Test Set-up

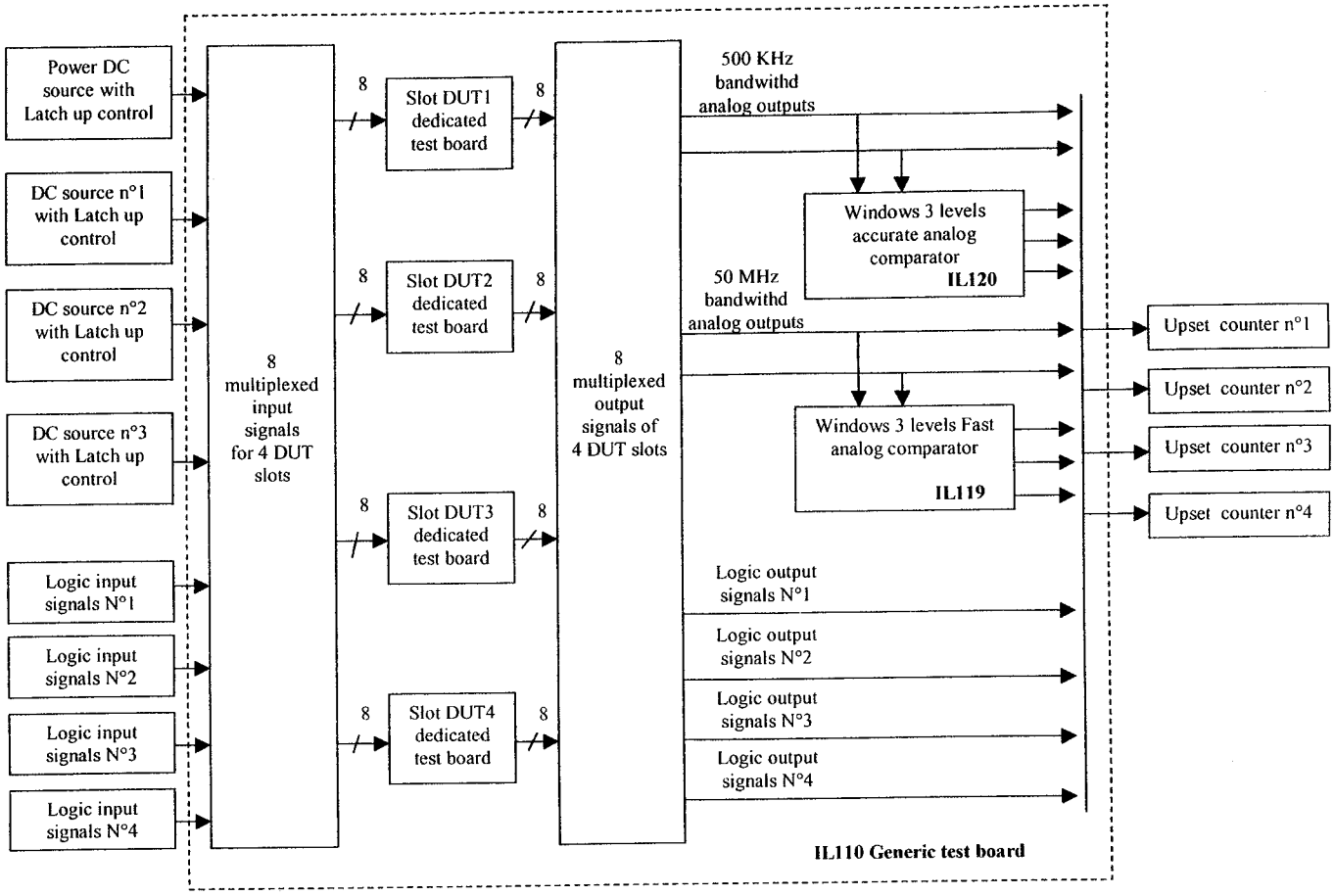


Figure IV-2 - Mother board synoptic

IV.2.2 DUT Test board description

The device under test is mounted on a specific board support which is plugged onto the motherboard.
Mechanical outlines : 141 mm x 50 mm, wrapping or printed circuit board with two 20 pins connectors.
According to test set up and device operating conditions, the test board can accept the mounting of :

- The DUT package with beam positioning constraints (unique for Louvain facilities)
- The golden chip
- The pattern generator
- any interface circuit such as buffer, latches ...
- a standalone micro controller if necessary...

Note : Beam focus diameter is limited to maximum 25 mm, to prevent the exposure of others devices which might be sensitive.

IV.3 TEST CONFIGURATIONS

Two test configurations have been used :

- First one is equivalent to a design implemented on XMM, called "Virgo Design" in the present report, where the comparator is used in a latched command which is triggered when the comparator input level exceeds a given threshold. Command re-initialization requires a power off-power-on cycle of the equipment.

- Second configuration is the comparator function itself where the amplifier output is always saturated, the output signal direction depending on the relative magnitude of the two comparator inputs.

IV.3.1 Virgo Design

Virgo Application :

- This comparator is used to control a shunt over-current with voltage levels from 10 to 30mV.
- The latch section is designed using discrete components (2 transistors and one diode).
- The only way to re-initialize the latch (when level comparison is over passed) is to switch off power supply.

Test principle :

The comparator input levels are generated using two programmable sources.

Each input is connected to a resistor bridge (divider by 10) and de-coupling capacitors that present an impedance equivalent to the one used in the application.

The latch is slightly modified (a resistor is added to the base of T02 (see Figure IV-3) which correspond to Q04 in Virgo drawing), in order to implement a RESET command allowing continuous testing of the component without switching off power supply after each UPSET.

A delay circuit is added for automatic reset of the latch, after a wait state of 1ms in order to detect which SEU is a transient pulse only and which one induces a permanent state.

Types of events detected :

- Transient upset limited to the comparator.
- Comparator or latch upset leading to a latch change.

Functional Check :

A 100µs @ 1Hz signal modifying the reference threshold and allowing activation of counting function.

Design change to improve upset tolerance :

Adding a de-coupling capacitor of 1 nFon the base of T02 allows introduction of a wait state on the locking of the transistor latch : thus transients at the outputs of the comparator would be filtered.

Different test set-up conditions :

Two different set-up conditions have been used and corresponding bias figures are given in the here below table :

Test board		Signal definition	Signal state	Set-up Cond. 1	Set-up Cond. 2
DC source	PVI	DUT supply	10V 1.6mA	5mA limit threshold	
DC source	VI1	Reference voltage input		300mV	300mV
DC source	VI2	Line voltage input		290mV	250mV
Scope chan 1	FO1	Latch output	10V to 0V	5V / Div	
Scope chan 2	FO2	Comparator output	10V to 0V	5V / Div	
Counter 1	FO1	Latch output	10V to 0V	Trig @ 5V ↓	
Counter 2	FO2	Comparator output	10V to 0V	Trig @ 8V ↓	
Counter 3	LO1	Latched SEU	Logic level	Trig @2.5V ↑	

Note : Actual differential input level is computed as follow :
(Reference) – (line) + (50mV external hysteresis effect with R1 resistor).

Table IV-1 - Virgo Design Test Conditions

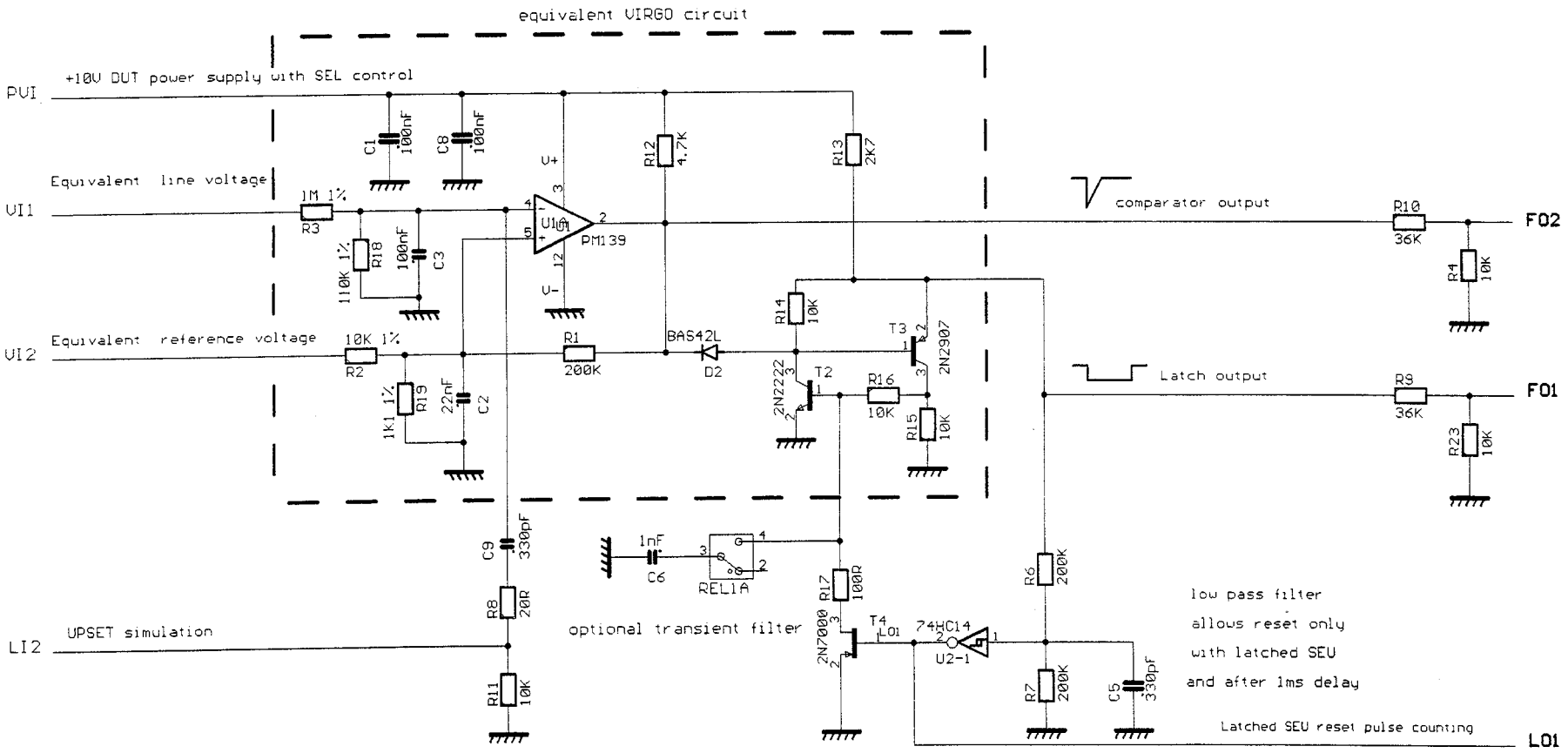


Figure IV-3 - LM139 Virgo Design Synoptic

IV.3.2 Comparator Application

Test principle :

The comparator input levels are generated using two programmable sources.

Types of events detected :

Comparator output is at +10 Volts in absence of event.
Transients are detected and counted into two different bins :

- Large errors, corresponding to the 2 Volts threshold : Comparator output transients with an amplitude higher than 8 volts are counted.
- Small errors, corresponding to the 8 Volts threshold : Comparator output transients with an amplitude higher than 2 volts (thus, include the large errors) are counted.

Functional Check :

A 100µs @ 1Hz signal modifying the reference threshold and allowing activation of counting function.

Different test set-up conditions :

Two different set-up conditions have been used and corresponding bias figures are given in the here below table :

Test board		Signal definition	Signal state	Set-up Cond. 1	Set-up Cond. 2
			Close to GND	Half supply CMV	
DC source	PVI	DUT supply	10V, 1.6mA	5mA limit threshold	
DC source	VI1	+ input		100mV	7.08V
DC source	VI2	- input		50mV	7.02V
Scope chan 1	FO1	Comparator output	10V to 0V	5V / Div	
Counter 1	FO1	small	10V to 0V	Trig @ 8V ↓	
Counter 2	FO2	large	10V to 0V	Trig @ 2V ↓	

Note : Actual differential input level is calculated as follow : (+input) – (-input)

Table IV-2 - LM139 Comparator Test Conditions

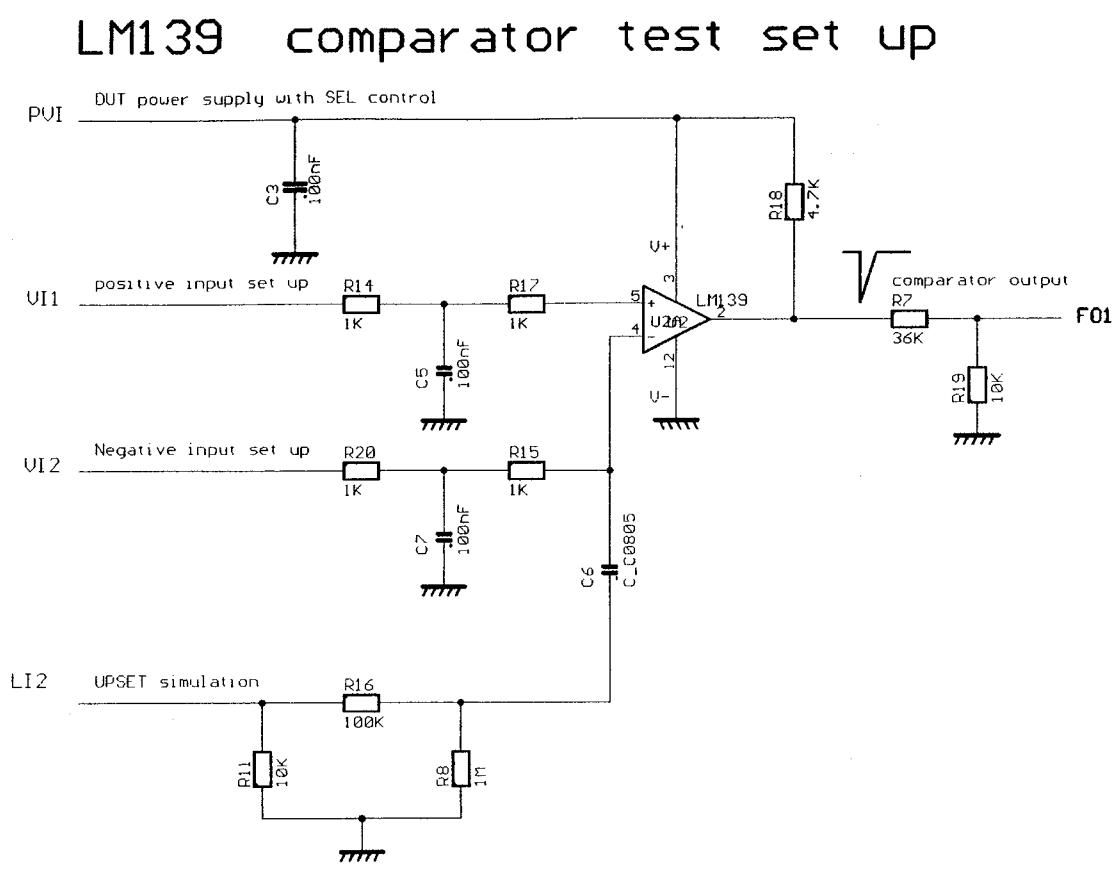


Figure IV-4 - LM139 Comparator Test Synoptic

Table VI-3 – Test results on National Semiconductor LM139 using Virgo configuration
Test T009 Virgo Condition 1 plus 1nF filtering capacitor

Run ID No	Test ID No	Sample ID No	Ion ID No	Date	Angle °	Eff. LET Mev/mg/cm²	Run Time sec	Eff. Time sec	Flux P/cm²/sec	TID per Sample Rads (Si)	Fluence P/cm²	Eff. Fluence P/cm²	Errors		
													Comparator	Latch	Latched SEU
R00012	T009	S004	I004	24/09/98	0	14,1	160	-	6,25 E+03	4,81 E+02	1,00 E+06	-	348	348	0
R00013	T009	S004	I004	24/09/98	45	19,94	189	-	5,29 E+03	8,00 E+02	1,00 E+06	-	323	323	0
R00014	T009	S004	I004	24/09/98	60	28,2	114	-	4,39 E+03	1,03 E+03	5,00 E+05	-	125	126	0
R00086	T009	S005	I004	25/09/98	0	14,1	156	-	3,21 E+03	9,49 E+02	5,00 E+05	-	198	197	0
R00087	T009	S005	I004	25/09/98	45	19,94	228	-	2,19 E+03	1,11 E+03	5,00 E+05	-	195	192	0
R00088	T009	S005	I004	25/09/98	60	28,2	196	-	2,56 E+03	1,34 E+03	5,02 E+05	-	85	84	0
R00121	T009	S005	I005	26/09/98	0	5,85	51	-	9,80 E+03	1,38 E+03	5,00 E+05	-	143	143	0
R00122	T009	S005	I005	26/09/98	45	8,27	71	-	7,04 E+03	1,45 E+03	5,00 E+05	-	125	125	0
R00123	T009	S005	I005	26/09/98	60	11,7	94	-	5,32 E+03	1,54 E+03	5,00 E+05	-	59	59	0
R00127	T009	S004	I005	26/09/98	0	5,85	28	-	1,79 E+04	1,78 E+03	5,00 E+05	-	149	149	0
R00128	T009	S004	I005	26/09/98	45	8,27	114	-	4,39 E+03	1,84 E+03	5,00 E+05	-	97	96	0
R00129	T009	S004	I005	26/09/98	60	11,7	156	-	3,21 E+03	1,94 E+03	5,00 E+05	-	107	106	0
R00267	T009	S005	I003	27/09/98	0	34	59	-	5,08 E+03	2,07 E+03	3,00 E+05	-	161	135	0
R00268	T009	S005	I003	27/09/98	45	48,08	83	-	3,61 E+03	2,31 E+03	3,00 E+05	-	132	116	0
R00269	T009	S005	I003	27/09/98	60	68	118	-	2,54 E+03	2,63 E+03	3,00 E+05	-	125	108	0
R00270	T009	S004	I003	27/09/98	60	68	114	-	2,63 E+03	2,26 E+03	3,00 E+05	-	133	110	0
R00271	T009	S004	I003	27/09/98	45	48,08	74	-	4,05 E+03	2,49 E+03	3,00 E+05	-	144	130	0
R00272	T009	S004	I003	27/09/98	0	34	57	-	5,26 E+03	2,66 E+03	3,00 E+05	-	146	134	0
R00287	T009	S004	I007	27/09/98	60	3,4	50	-	6,00 E+03	3,43 E+03	3,00 E+05	-	0	0	0
R00288	T009	S005	I007	27/09/98	60	3,4	49	-	6,12 E+03	3,40 E+03	3,00 E+05	-	0	0	0
R00289	T009	S005	I007	27/09/98	0	1,7	79	-	1,27 E+04	3,43 E+03	1,00 E+06	-	0	0	0

Ion ID	Specy	Energy MeV	LET Mev/mg/cm²	Range µm
I004	40-Ar	150	14,1	42
I005	20-Ne	78	5,85	45
I003	84-Kr	316	34	43
I007	10-B	41	1,7	80

Sample ID	SN	Part Type	Date Code	Comments
S004	#1	LM139J	9706	National Semiconductor DC9706
S005	#2	LM139J	9712	National Semiconductor DC9712

Note	Condition 1 :	VI1	Reference voltage input	300mV
		VI2	Line voltage input	290mV

Table VI-4 - Results on National Semiconductor LM139 using comparator configuration
Test T010 – Comparator Condition 1

Run ID No	Test ID No	Sample ID No	Ion ID No	Date	Angle °	Eff. LET Mev/mg/cm²	Run Time sec	Eff. Time sec	Flux P/cm²/sec	TID per Sample Rads (Si)	Fluence P/cm²	Eff. Fluence P/cm²	Errors Small	Errors Large
R00019	T010	S005	I004	24/09/98	0	14,1	82	-	6,10 E+03	1,13 E+02	5,00 E+05	-	282	275
R00020	T010	S005	I004	24/09/98	45	19,94	118	-	4,24 E+03	2,72 E+02	5,00 E+05	-	298	288
R00021	T010	S005	I004	24/09/98	60	28,2	172	-	2,91 E+03	4,98 E+02	5,00 E+05	-	244	225
R00083	T010	S004	I004	25/09/98	0	14,1	144	-	3,47 E+03	1,14 E+03	5,00 E+05	-	335	325
R00084	T010	S004	I004	25/09/98	45	19,94	215	-	2,33 E+03	1,30 E+03	5,00 E+05	-	326	316
R00085	T010	S004	I004	25/09/98	60	28,2	317	-	1,58 E+03	1,52 E+03	5,00 E+05	-	342	309
R00118	T010	S004	I005	26/09/98	0	5,85	50	-	1,00 E+04	1,57 E+03	5,00 E+05	-	234	224
R00119	T010	S004	I005	26/09/98	45	8,27	103	-	4,85 E+03	1,64 E+03	5,00 E+05	-	240	237
R00120	T010	S004	I005	26/09/98	60	11,7	134	-	3,73 E+03	1,73 E+03	5,00 E+05	-	262	251
R00137	T010	S005	I005	26/09/98	60	11,7	129	-	3,88 E+03	1,64 E+03	5,00 E+05	-	220	207
R00138	T010	S005	I005	26/09/98	45	8,27	82	-	6,10 E+03	1,70 E+03	5,00 E+05	-	275	264
R00139	T010	S005	I005	26/09/98	0	5,85	63	-	7,94 E+03	1,75 E+03	5,00 E+05	-	283	271
R00273	T010	S004	I003	27/09/98	0	34	49	-	6,12 E+03	2,82 E+03	3,00 E+05	-	289	216
R00274	T010	S004	I003	27/09/98	45	48,08	78	-	3,85 E+03	3,05 E+03	3,00 E+05	-	287	228
R00275	T010	S004	I003	27/09/98	60	68	107	-	2,80 E+03	3,38 E+03	3,00 E+05	-	295	221
R00276	T010	S005	I003	27/09/98	60	68	101	-	2,97 E+03	2,96 E+03	3,00 E+05	-	290	227
R00277	T010	S005	I003	27/09/98	45	48,08	76	-	3,95 E+03	3,19 E+03	3,00 E+05	-	299	230
R00278	T010	S005	I003	27/09/98	0	34	53	-	5,66 E+03	3,35 E+03	3,00 E+05	-	309	238
R00279	T010	S005	I007	27/09/98	60	3,4	65	-	4,62 E+03	3,37 E+03	3,00 E+05	-	164	133
R00280	T010	S005	I007	27/09/98	45	2,4	46	-	6,52 E+03	3,38 E+03	3,00 E+05	-	141	133
R00281	T010	S005	I007	27/09/98	0	1,7	34	-	8,82 E+03	3,39 E+03	3,00 E+05	-	106	103
R00282	T010	S004	I007	27/09/98	0	1,7	33	-	9,09 E+03	3,39 E+03	3,00 E+05	-	111	109
R00283	T010	S004	I007	27/09/98	45	2,4	46	-	6,52 E+03	3,40 E+03	3,00 E+05	-	126	121
R00284	T010	S004	I007	27/09/98	60	3,4	92	-	3,26 E+03	3,41 E+03	3,00 E+05	-	122	103

Ion ID	Specy	Energy MeV	LET Mev/mg/cm²	Range µm
I004	40-Ar	150	14,1	42
I005	20-Ne	78	5,85	45
I003	84-Kr	316	34	43
I007	10-B	41	1,7	80

Sample ID	SN	Part Type	Date Code	Comments
S004	#1	LM139J	9706	National Semiconductor DC9706
S005	#2	LM139J	9712	National Semiconductor DC9712

Note	Condition 1 :			
		VI1	+ input	100mV
		VI2	- input	50mV

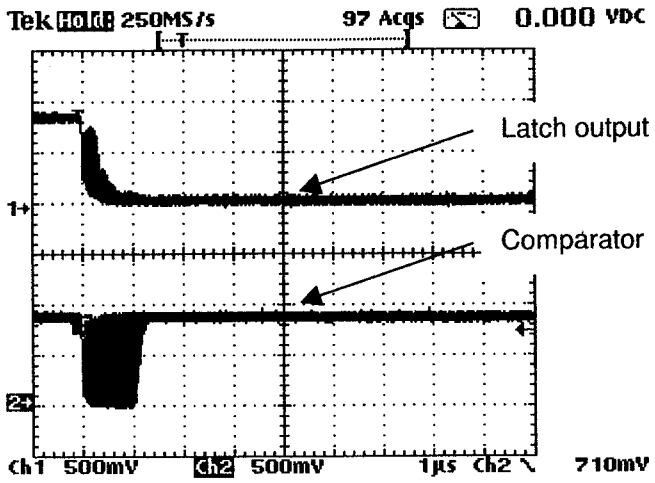
Table VI-5 - Results on National Semiconductor LM139 using comparator configuration
Test T011 – Comparator Condition 2

Run ID No	Test ID No	Sample ID No	Ion ID No	Date	Angle °	Eff. LET Mev/mg/cm²	Run Time sec	Eff. Time sec	Flux P/cm²/sec	TID per Sample Rads (Si)	Fluence P/cm²	Eff. Fluence P/cm²	Errors Small	Errors Large
R00022	T011	S005	I004	24/09/98	0	14,1	83	-	6,02 E+03	6,11 E+02	5,00 E+05	-	207	206
R00023	T011	S005	I004	24/09/98	60	28,2	192	-	2,60 E+03	8,36 E+02	5,00 E+05	-	113	111

Ion ID	Specy	Energy MeV	LET Mev/mg/cm²	Range µm
I004	40-Ar	150	14,1	42
I005	20-Ne	78	5,85	45
I003	84-Kr	316	34	43
I007	10-B	41	1,7	80

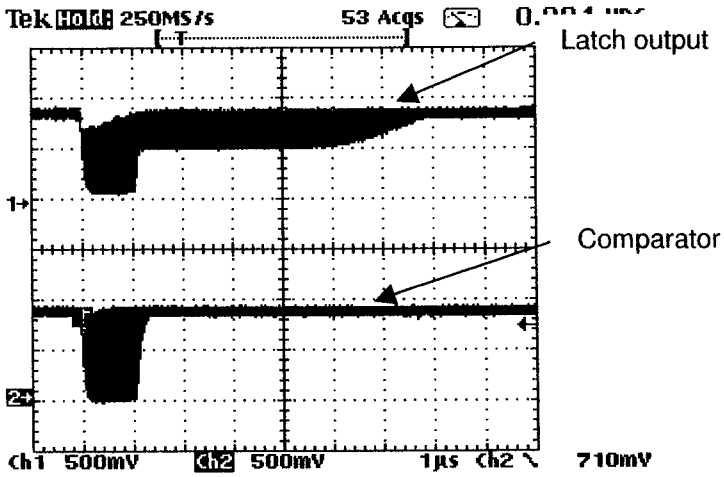
Sample ID	SN	Part Type	Date Code	Comments
S004	#1	LM139J	9706	National Semiconductor DC9706
S005	#2	LM139J	9712	National Semiconductor DC9712

Note	Condition 2 :	VI1	+ input	7.08V
		VI2	- input	7.02V



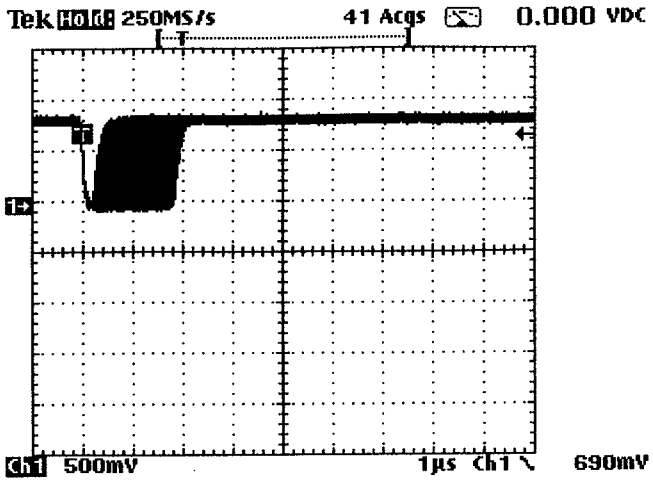
(5V/div 2µs)
In this case, the change of the latch state can be observed

Figure VI-2 – Typical Waveform, Virgo configuration without filter capacitor



(5V/div 2µs)
This scope record shows that the latch output change
does not latch thanks to the filtering capacitor

Figure VI-3 – Typical Waveform, Virgo configuration with 1nF capacitor filter



(5V/div 1µs)
This scope record shows the envelop of SEU pulses of different transient duration

Figure VI-4 – Typical Waveform, Comparator configuration

VII. CONCLUSION

SEU test have been conducted on LM139J Quad Voltage Comparator from National Semiconductor, using the heavy ions available at the University of Louvain facility.

SEU susceptibility was obtained through the error cross section versus LET curve for two different test configurations.

The effect of a capacitor filter applied in the Virgo equivalent configuration has been assessed and drastic improvement has been obtained.

With these results, upset predictions on XMM orbit, can be performed for each error type and the risk associated with the present Virgo design can be assessed.

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RADIATION TEST REPORT

Heavy Ions Testing of

PM139 (PMI)

Quad Voltage Comparator

from Analog Devices

ESA Purchase Order No 181635 dated 13/08/98

European Space Agency Contract Report

The work described in this report was done under ESA contract.
Responsibility for the contents resides in the author or organization that prepared it

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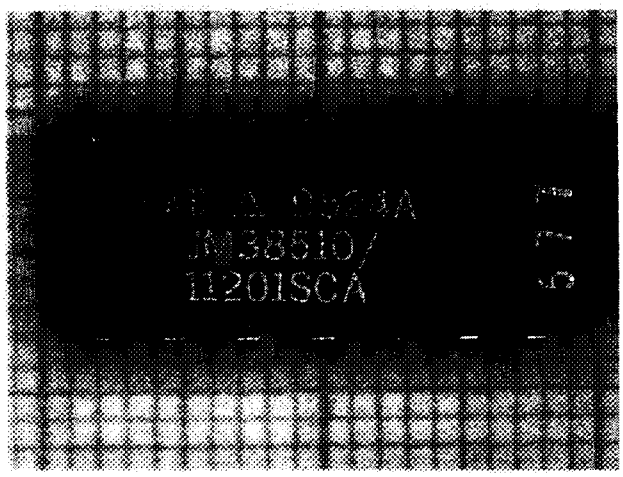
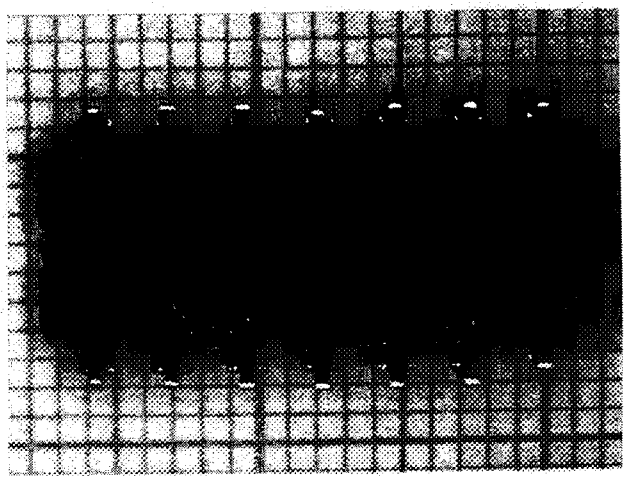
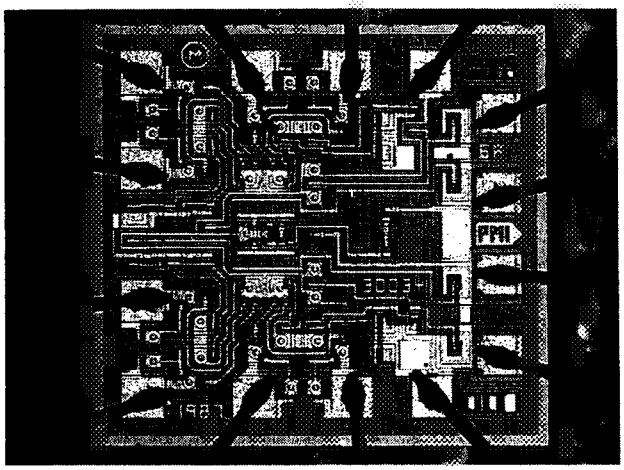


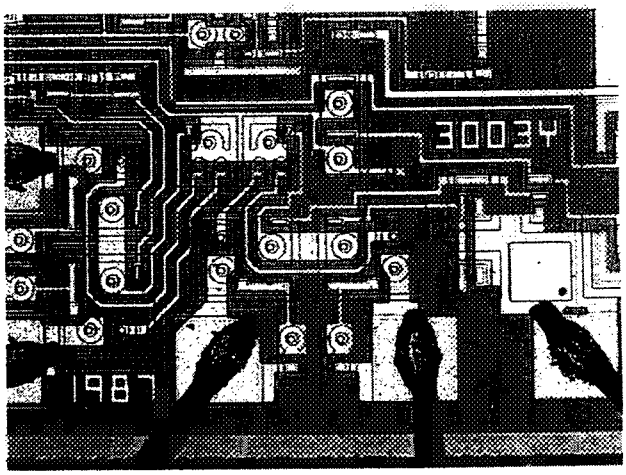
Top view



Bottom view



Full view



Die marking

IV. DEVICE TEST PATTERN DEFINITION

IV.1 PREPARATION OF TEST HARDWARE AND PROGRAM

Overall device emulation, SEU and Latch-up detection, data storage and processing were implemented using an in-house test hardware and an application specific test board.

The generic in-house test equipment is driven by a PC computer through a RS232 line. All power supplies and input signals are delivered and monitored by the in-house equipment which also stores in its memory the output data from the device throughout the specific test board.

The application specific test board allowed to interface the standard test hardware with the device under test, in order to correctly emulate the relevant part, to record all the different type of errors during the irradiation and to set output signal for processing and storage by the standard test equipment.

At the end of each test run, data are transferred to the PC computer through the RS232 link for storage on hard disk or floppies.

IV.2 GENERIC TEST SET-UP

The complete test equipment is constituted of:

- A PC computer (to configure and interface with the test system and store the data),
- An electronic rack with the instrumentation functions provided by a set of electronic modules,
- A mother board under vacuum which allows for the sequential test of up to 4 devices
- A digital oscilloscope to store analog upset waveform

Generic device test set-up is presented in Figure IV-1.

IV.2.1 Mother board description (ref. IL110)

The motherboard acts as a standard interface between each DUT test board and the control unit :
For each DUT board slot , the following signals can be considered:

- 8 inputs signals
  - 4 programmable power supplies
  - 4 programmable clocks
- 8 output signals
  - 4 logic counting signals
  - 2 fast analog signals
  - 2 accurate analog signals

- Each device needs a dedicated plug-in test board compatible with IL110 mother board.
- IL110 board has been designed to comply with Louvain Test facilities .
- The number of slots is limited to four

Operation is multiplexed and only one slot is powered at one time.

Mother board synoptic is shown in Figure IV-2.

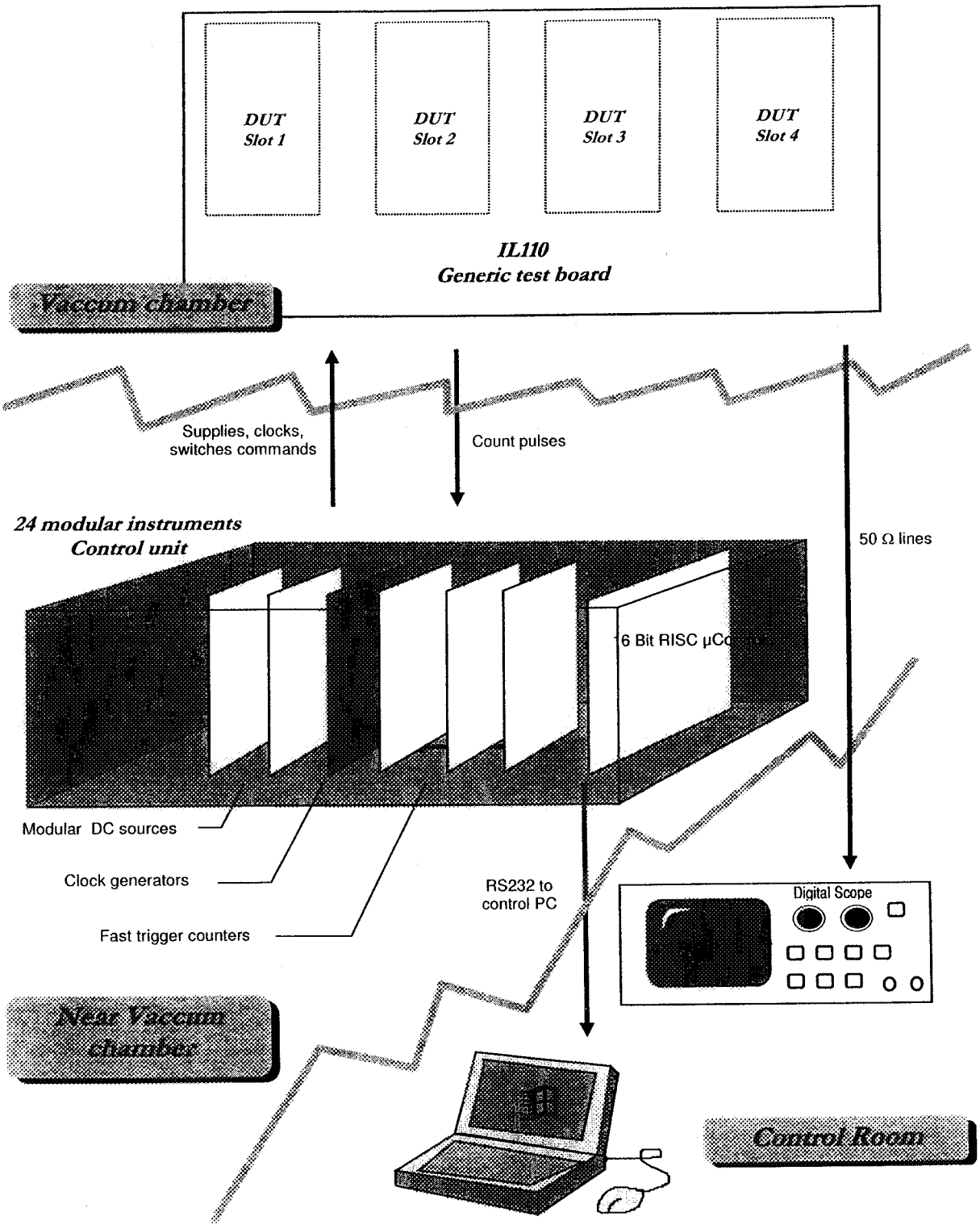


Figure IV-1 - Generic Device Test Set-up

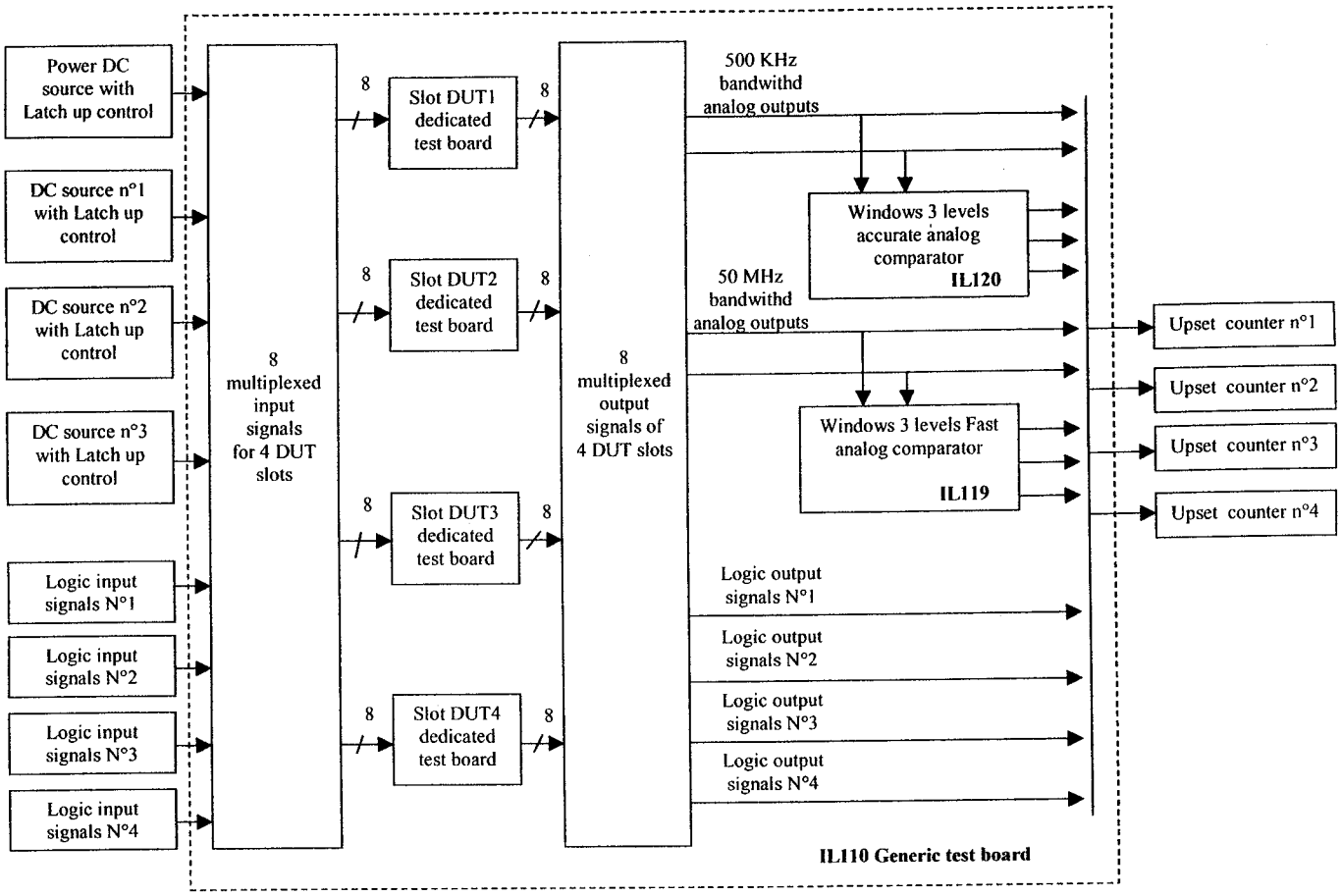


Figure IV-2 - Mother board synoptic

IV.2.2 DUT Test board description

The device under test is mounted on a specific board support which is plugged onto the motherboard.
Mechanical outlines : 141 mm x 50 mm, wrapping or printed circuit board with two 20 pins connectors.
According to test set up and device operating conditions, the test board can accept the mounting of :

- The DUT package with beam positioning constraints (unique for Louvain facilities)
- The golden chip
- The pattern generator
- any interface circuit such as buffer, latches ...
- a standalone micro controller if necessary...

Note : Beam focus diameter is limited to maximum 25 mm, to prevent the exposure of others devices which might be sensitive.

IV.3 TEST CONFIGURATIONS

Two test configurations have been used :

- First one is equivalent to a design implemented on XMM, called "Virgo Design" in the present report, where the comparator is used in a latched command which is triggered when the comparator input level exceeds a given threshold. Command re-initialization requires a power off-power-on cycle of the equipment.

- Second configuration is the comparator function itself where the amplifier output is always saturated, the output signal direction depending on the relative magnitude of the two comparator inputs.

IV.3.1 Virgo Design

Virgo Application :

- This comparator is used to control a shunt over-current with voltage levels from 10 to 30mV.
- The latch section is designed using discrete components (2 transistors and one diode).
- The only way to re-initialize the latch (when level comparison is over passed) is to switch off power supply.

Test principle :

The comparator input levels are generated using two programmable sources.

Each input is connected to a resistor bridge (divider by 10) and de-coupling capacitors that present an impedance equivalent to the one used in the application.

The latch is slightly modified (a resistor is added to the base of T02 (see Figure IV-3) which correspond to Q04 in Virgo drawing), in order to implement a RESET command allowing continuous testing of the component without switching off power supply after each UPSET.

A delay circuit is added for automatic reset of the latch, after a wait state of 1ms in order to detect which SEU is a transient pulse only and which one induces a permanent state.

Types of events detected :

- Transient upset limited to the comparator.
- Comparator or latch upset leading to a latch change.

Functional Check :

A 100µs @ 1Hz signal modifying the reference threshold and allowing activation of counting function.

Design change to improve upset tolerance :

Adding a de-coupling capacitor of 1 nFon the base of T02 allows introduction of a wait state on the locking of the transistor latch : thus transients at the outputs of the comparator would be filtered.

Different test set-up conditions :

Two different set-up conditions have been used and corresponding bias figures are given in the here below table :

Test board		Signal definition	Signal state	Set-up Cond. 1	Set-up Cond. 2
DC source	PVI	DUT supply	10V 1.6mA	5mA limit threshold	
DC source	VI1	Reference voltage input		300mV	300mV
DC source	VI2	Line voltage input		290mV	250mV
Scope chan 1	FO1	Latch output	10V to 0V	5V / Div	
Scope chan 2	FO2	Comparator output	10V to 0V	5V / Div	
Counter 1	FO1	Latch output	10V to 0V	Trig @ 5V ↓	
Counter 2	FO2	Comparator output	10V to 0V	Trig @ 8V ↓	
Counter 3	LO1	Latched SEU	Logic level	Trig @2.5V ↑	

Note : Actual differential input level is computed as follow :
(Reference) – (line) + (50mV external hysteresis effect with R1 resistor).

Table IV-1 - Virgo Design Test Conditions

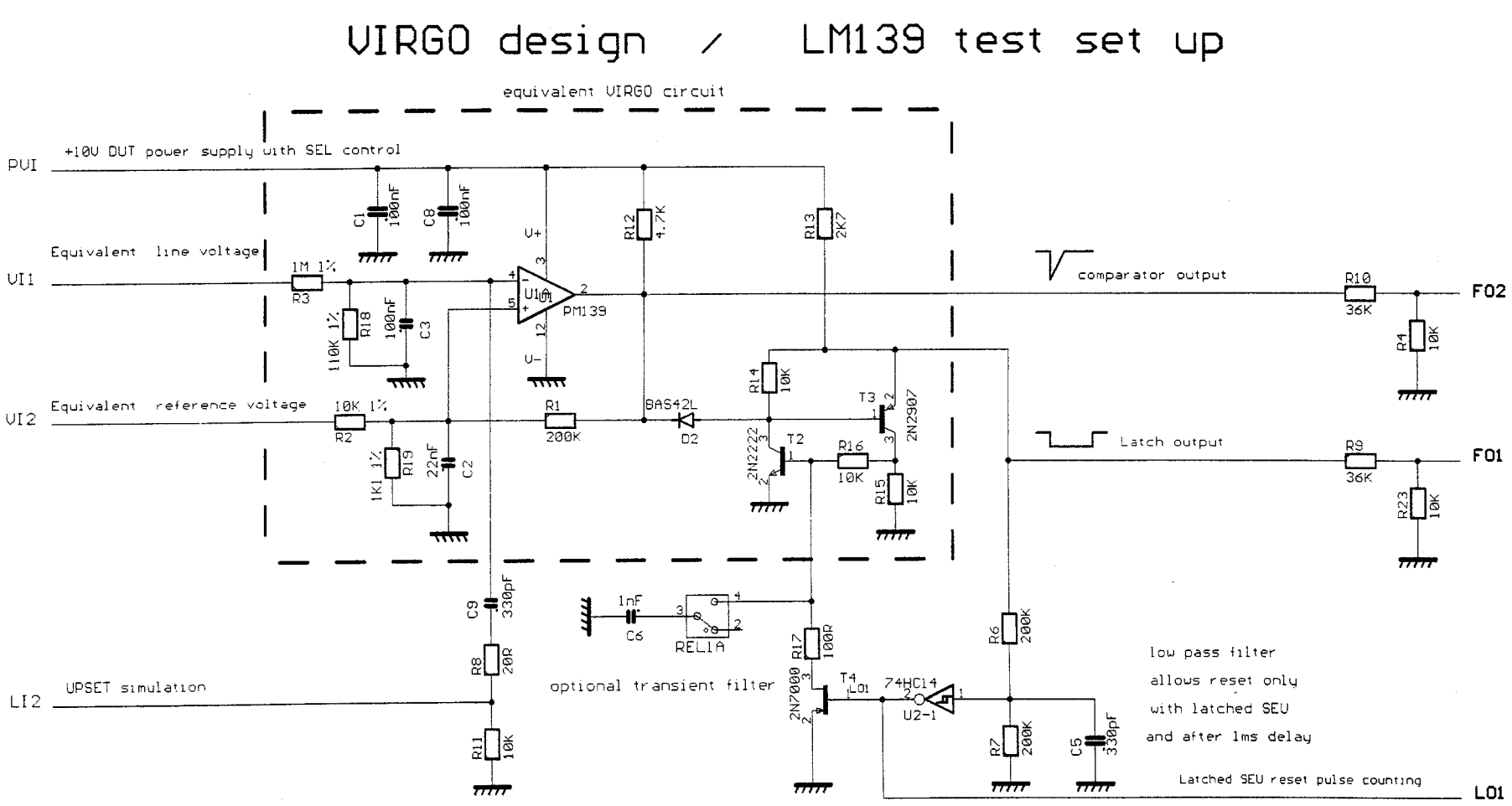


Figure IV-3 - LM139 Virgo Design Synoptic

IV.3.2 Comparator Application

Test principle :

The comparator input levels are generated using two programmable sources.

Types of events detected :

Comparator output is at +10 Volts in absence of event.
Transients are detected and counted into two different bins :

- Large errors, corresponding to the 2 Volts threshold : Comparator output transients with an amplitude higher than 8 volts are counted.
- Small errors, corresponding to the 8 Volts threshold : Comparator output transients with an amplitude higher than 2 volts (thus, include the large errors) are counted.

Functional Check :

A 100µs @ 1Hz signal modifying the reference threshold and allowing activation of counting function.

Different test set-up conditions :

Two different set-up conditions have been used and corresponding bias figures are given in the here below table :

Test board		Signal definition	Signal state	Set-up Cond. 1	Set-up Cond. 2
			Close to GND	Half supply CMV	
DC source	PVI	DUT supply	10V, 1.6mA	5mA limit threshold	
DC source	VI1	+ input		100mV	7.08V
DC source	VI2	- input		50mV	7.02V
Scope chan 1	FO1	Comparator output	10V to 0V	5V / Div	
Counter 1	FO1	small	10V to 0V	Trig @ 8V ↓	
Counter 2	FO2	large	10V to 0V	Trig @ 2V ↓	

Note : Actual differential input level is calculated as follow : (+input) – (-input)

Table IV-2 - PM139 Comparator Test Conditions

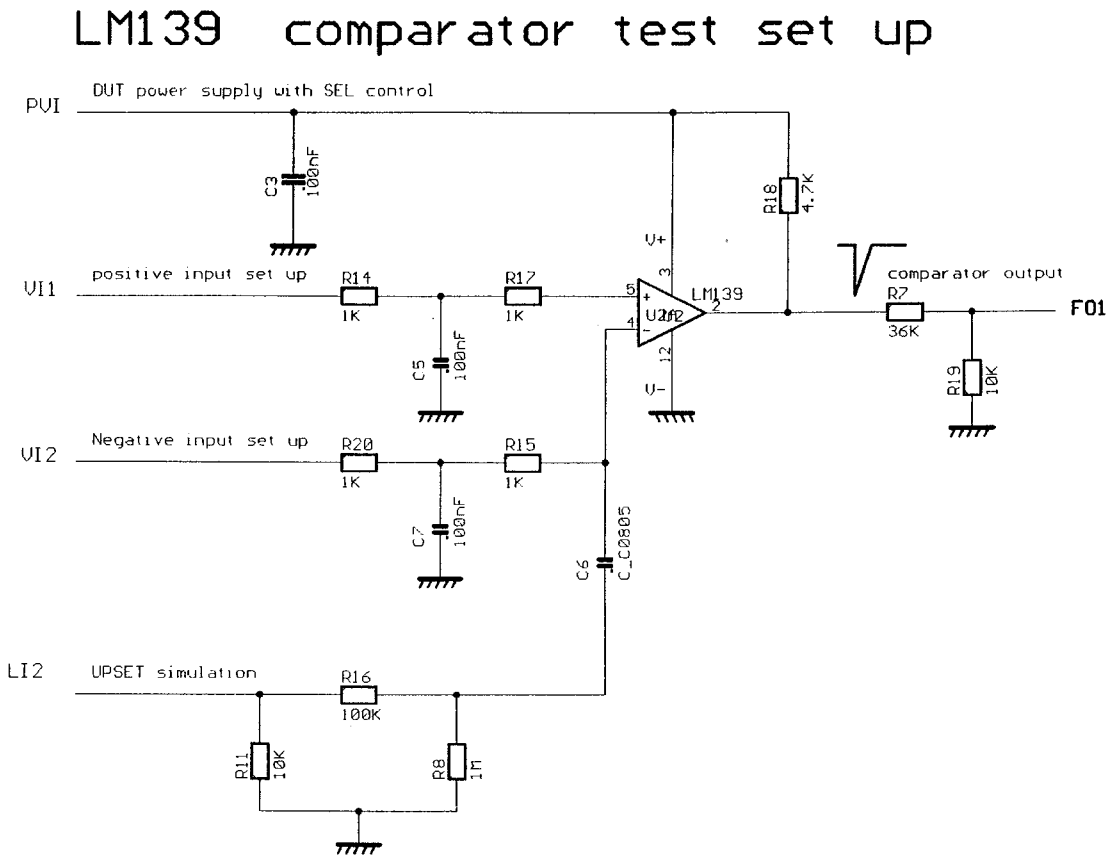


Figure IV-4 - PM139 Comparator Test Synoptic

V. TEST FACILITIES

Test at the cyclotron accelerator was performed at Université de Louvain (UCL) in Louvain la neuve (Belgium) under HIREX Engineering responsibility.
2 delidded samples were irradiated, while #971 was kept as reference.

V.1 BEAM SOURCE

In collaboration with the European Space Agency (ESA), the needed equipment for single events studies using heavy ions has been built and installed on the HIF beam line in the experimental hall of Louvain-la-Neuve cyclotron.
CYCLONE is a multi particle, variable energy, cyclotron capable of accelerating protons (up to 75 MeV), alpha particles and heavy ions. For the heavy ions, the covered energy range is between 0.6 MeV/AMU and 27.5 MeV/AMU. For these ions, the maximal energy can be determined by the formula :

$$110\ Q^2/M$$

where Q is the ion charge state, and M is the mass in Atomic Mass Units.

The heavy ions are produced in a double stage Electron Cyclotron Resonance (ECR) source. Such a source allows to produce highly charged ions and ion "cocktails". These are composed of ions with the same or very close M/Q ratios. The cocktail ions are injected in the cyclotron, accelerated at the same time and extracted separately by a fine tuning of the magnetic field or a slight changing of the RF frequency. This method is very convenient for a quick change of ion (in a few minutes) which is equivalent to a LET variation.

V.2 BEAM SET-UP

V.2.1 Ion Beam Selection

The LET range was obtained by changing the ion species and incident energy and changing the angle of incidence between the beam and the chip, Table VI-2, Table VI-3, Table VI-4, and Table VI-5 provide the ions which were used to determine the LET threshold and the asymptotic cross section within the LET range for this heavy ion characterization. In addition ion energy, LET, range and tilt angle are also provided for each test run.

V.2.2 Flux Range

Particle flux could be varied from few hundred ions/cm²/sec up to a ten thousand ions/cm²/sec under normal operations (tilt 0°).

V.2.3 Particle Fluence Levels

Fluence level was comprised between 3 x10E5 and 1 x10E6 ions/cm²

V.2.4 Dosimetry

The current UCL Cyclotron dosimetry system and procedures were used.

V.2.5 Accumulated Total Dose

Table VI-2 to Table VI-5 provide for each run the equivalent total dose (rad(Si)) received by each device under test.
For each device, the total amount is below 5 x10E+03 rads.

V.2.6 Test Temperature Range

All the tests performed were conducted at ambient temperature.

VI. RESULTS

Virgo test configuration :

As mentioned in paragraph IV.3.1, the effect of Single Event Upset was monitored and counted at three different locations of the test circuit :

- At the output of the comparator, see F01 line in Figure IV-3, (which is the only device irradiated on the board),
- At the output of the latch to see any transient propagated by the comparator, see F02 line in Figure IV-3.
- If the latch state has changed permanently, a third counter is incremented after a time delay period of 100 ms, see L01 line in Figure IV-3.

Table VI-2and Table VI-3 give the test results using the Virgo configuration without the filtering capacitor for two different operating conditions.

The main result from all runs using the first test configuration is that nearly every transient detected at the comparator output is also detected at the latch output and in absence of the filtering capacitor, the latch state changes permanently.

Table VI-4 give the test results using the Virgo configuration with the filtering capacitor added.

It can be seen that the add-on filter with a capacitor of 1nF is efficient as no latched SEU errors could be detected anymore (No more permanent latch state change).

Comparator test configuration :

In this configuration and in absence of event, the output comparator is fixed to +10 volts and transients errors, which will switch the comparator output towards zero, will be detected with two different threshold levels :

- Large error : transient signal amplitude higher than the 8 volts threshold,
- Small error : transient signal amplitude signal higher than the 2 volts threshold

Table VI-5 give the test results using the comparator configuration.

The main result from all runs, is that most of the transients fall in the large error category.

Test results comparison :

Two samples have been tested in both test configurations and results are very consistent.
Comparison between the two test configurations, i.e. Virgo (comparator errors) and the stand-alone comparator (small errors), is provided in Figure VI-1 where the number of errors have been averaged on the two samples. Table VI-1 provides the corresponding figures.
It can be noted a strong effect of the tilt angle in the error cross-section

Lastly typical waveforms observed with the scope are provided in Figure VI-2, Figure VI-3, Figure VI-4, in the following respective configurations, Virgo, Virgo with 1nF filtering capacitor and lastly, comparator configuration.

Table VI-2 – Test results on Analog Devices PM139 using Virgo configuration
Test T007 Virgo Condition 1

Run ID No	Test ID No	Sample ID No	Ion ID No	Date	Angle °	Eff. LET Mev/mg/cm²	Run Time sec	Eff. Time sec	Flux P/cm²/sec	TID per Sample Rads (Si)	Fluence P/cm²	Eff. Fluence P/cm²	Errors		
													Comparator	Latch	Latched SEU
R00008	T007	S016	I004	24/09/98	60	28,2	204	-	2,45 E+03	1,74 E+03	5,00 E+05	-	110	123	123
R00228	T007	S016	I003	27/09/98	0	34	46	-	6,52 E+03	3,12 E+03	3,00 E+05	-	175	175	175

Ion ID	Specy	Energy MeV	LET Mev/mg/cm²	Range µm
I004	40-Ar	150	14,1	42
I005	20-Ne	78	5,85	45
I003	84-Kr	316	34	43
I007	10-B	41	1,7	80

Sample ID	SN	Part Type	Date Code	Comments
S016	#576	PM139	9524A	Analog devices / PMI
S017	#679	PM139	9524A	Analog devices / PMI

Note	Condition 1 :			
		VI1	Reference voltage input	300mV
		VI2	Line voltage input	290mV

Table VI-3 – Test results on Analog Devices PM139 using Virgo configuration
Test T008 Virgo Condition 2

Run ID No	Test ID No	Sample ID No	Ion ID No	Date	Angle °	Eff. LET Mev/mg/cm²	Run Time sec	Eff. Time sec	Flux P/cm²/sec	TID per Sample Rads (Si)	Fluence P/cm²	Eff. Fluence P/cm²	Errors		
													Comparator	Latch	Latched SEU
R00004	T008	S016	I004	24/09/98	0	14,1	223	-	4,48 E+03	9,02 E+02	1,00 E+06	-	304	304	304

Ion ID	Specy	Energy MeV	LET Mev/mg/cm²	Range µm
I004	40-Ar	150	14,1	42
I005	20-Ne	78	5,85	45
I003	84-Kr	316	34	43
I007	10-B	41	1,7	80

Sample ID	SN	Part Type	Date Code	Comments
S016	#576	PM139	9524A	Analog devices / PMI
S017	#679	PM139	9524A	Analog devices / PMI

Note	Condition 2 :			
		VI1	Reference voltage input	300mV
		VI2	Line voltage input	250mV

Table VI-4 – Test results on Analog Devices PM139 using Virgo configuration
Test T009 Virgo Condition 1 plus 1nF filtering capacitor

Run ID No	Test ID No	Sample ID No	Ion ID No	Date	Angle °	Eff. LET Mev/mg/cm²	Run Time sec	Eff. Time sec	Flux P/cm²/sec	TID per Sample Rads (Si)	Fluence P/cm²	Eff. Fluence P/cm²	Errors		
													Comparator	Latch	Latched SEU
R00006	T009	S016	I004	24/09/98	0	14,1	190	-	5,26 E+03	1,35 E+03	1,00 E+06	-	307	307	0
R00007	T009	S016	I004	24/09/98	45	19,94	149	-	3,36 E+03	1,51 E+03	5,00 E+05	-	151	151	0
R00009	T009	S016	I004	24/09/98	60	28,2	199	-	2,51 E+03	1,96 E+03	5,00 E+05	-	99	99	0
R00089	T009	S017	I004	25/09/98	0	14,1	76	-	6,58 E+03	7,24 E+02	5,00 E+05	-	178	159	0
R00090	T009	S017	I004	25/09/98	45	19,94	116	-	4,31 E+03	8,83 E+02	5,00 E+05	-	191	178	0
R00091	T009	S017	I004	25/09/98	60	28,2	170	-	2,94 E+03	1,11 E+03	5,00 E+05	-	142	130	0
R00124	T009	S017	I005	26/09/98	0	5,85	44	-	1,14 E+04	1,16 E+03	5,00 E+05	-	122	122	0
R00125	T009	S017	I005	26/09/98	45	8,27	65	-	7,69 E+03	1,22 E+03	5,00 E+05	-	110	110	0
R00126	T009	S017	I005	26/09/98	60	11,7	86	-	5,81 E+03	1,32 E+03	5,00 E+05	-	113	112	0
R00130	T009	S016	I005	26/09/98	0	5,85	79	-	6,33 E+03	2,75 E+03	5,00 E+05	-	40	40	0
R00131	T009	S016	I005	26/09/98	45	8,27	108	-	4,63 E+03	2,82 E+03	5,00 E+05	-	135	131	0
R00132	T009	S016	I005	26/09/98	60	11,7	144	-	3,47 E+03	2,91 E+03	5,00 E+05	-	81	77	0
R00133	T009	S016	I005	26/09/98	0	5,85	71	-	7,04 E+03	2,96 E+03	5,00 E+05	-	103	103	0
R00229	T009	S016	I003	27/09/98	0	34	48	-	6,25 E+03	3,29 E+03	3,00 E+05	-	180	146	0
R00230	T009	S016	I003	27/09/98	45	48,08	59	-	5,08 E+03	3,52 E+03	3,00 E+05	-	185	150	0
R00231	T009	S016	I003	27/09/98	60	68	90	-	3,33 E+03	3,84 E+03	3,00 E+05	-	156	119	0
R00232	T009	S017	I003	27/09/98	60	68	87	-	3,45 E+03	1,85 E+03	3,00 E+05	-	177	132	0
R00233	T009	S017	I003	27/09/98	45	48,08	61	-	4,92 E+03	2,08 E+03	3,00 E+05	-	149	119	0
R00234	T009	S017	I003	27/09/98	0	34	37	-	8,11 E+03	2,24 E+03	3,00 E+05	-	204	165	0
R00285	T009	S017	I007	27/09/98	60	3,4	75	-	4,00 E+03	2,98 E+03	3,00 E+05	-	0	0	0
R00286	T009	S016	I007	27/09/98	60	3,4	59	-	5,08 E+03	4,58 E+03	3,00 E+05	-	0	0	0

Ion ID	Specy	Energy MeV	LET Mev/mg/cm²	Range µm
I004	40-Ar	150	14,1	42
I005	20-Ne	78	5,85	45
I003	84-Kr	316	34	43
I007	10-B	41	1,7	80

Sample ID	SN	Part Type	Date Code	Comments
S016	#576	PM139	9524A	Analog devices / PMI
S017	#679	PM139	9524A	Analog devices / PMI

Note	Condition 1 :			
		VI1	Reference voltage input	300mV
		VI2	Line voltage input	290mV

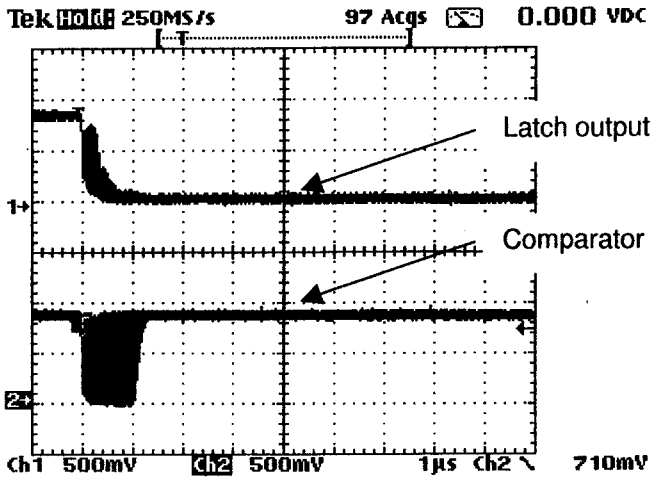
Table VI-5 - Results on Analog Devices PM139 using comparator configuration
Test T010 – Comparator Condition 1

Run ID No	Test ID No	Sample ID No	Ion ID No	Date	Angle °	Eff. LET Mev/mg/cm²	Run Time sec	Eff. Time sec	Flux P/cm²/sec	TID per Sample Rads (Si)	Fluence P/cm²	Eff. Fluence P/cm²	Errors Small	Errors Large
R00016	T010	S017	I004	24/09/98	0	14,1	86	-	5,81 E+03	2,26 E+02	5,00 E+05	-	238	240
R00017	T010	S017	I004	24/09/98	45	19,94	120	-	4,17 E+03	3,85 E+02	5,00 E+05	-	280	253
R00018	T010	S017	I004	24/09/98	60	28,2	155	-	3,23 E+03	6,11 E+02	5,00 E+05	-	280	241
R00080	T010	S016	I004	25/09/98	0	14,1	139	-	3,60 E+03	2,08 E+03	5,00 E+05	-	264	261
R00081	T010	S016	I004	25/09/98	45	19,94	199	-	2,51 E+03	2,24 E+03	5,00 E+05	-	266	242
R00082	T010	S016	I004	25/09/98	60	28,2	292	-	1,71 E+03	2,46 E+03	5,00 E+05	-	334	291
R00115	T010	S016	I005	26/09/98	60	11,7	287	-	2,47 E+03	2,59 E+03	7,09 E+05	-	340	331
R00116	T010	S016	I005	26/09/98	45	8,27	161	-	3,11 E+03	2,66 E+03	5,00 E+05	-	228	221
R00117	T010	S016	I005	26/09/98	0	5,85	70	-	7,14 E+03	2,71 E+03	5,00 E+05	-	225	221
R00134	T010	S017	I005	26/09/98	0	5,85	69	-	7,25 E+03	1,36 E+03	5,00 E+05	-	207	202
R00135	T010	S017	I005	26/09/98	45	8,27	95	-	5,26 E+03	1,43 E+03	5,00 E+05	-	229	225
R00136	T010	S017	I005	26/09/98	60	11,7	133	-	3,76 E+03	1,52 E+03	5,00 E+05	-	258	250
R00254	T010	S016	I003	27/09/98	0	34	62	-	4,84 E+03	4,01 E+03	3,00 E+05	-	342	271
R00255	T010	S016	I003	27/09/98	45	48,08	78	-	3,85 E+03	4,24 E+03	3,00 E+05	-	291	242
R00256	T010	S016	I003	27/09/98	60	68	123	-	2,44 E+03	4,57 E+03	3,00 E+05	-	246	184
R00257	T010	S017	I003	27/09/98	60	68	128	-	2,34 E+03	2,57 E+03	3,00 E+05	-	281	219
R00258	T010	S017	I003	27/09/98	45	48,08	87	-	3,45 E+03	2,80 E+03	3,00 E+05	-	301	239
R00259	T010	S017	I003	27/09/98	0	34	63	-	4,76 E+03	2,96 E+03	3,00 E+05	-	308	240
R00290	T010	S016	I007	27/09/98	60	3,4	84	-	5,95 E+03	4,61 E+03	5,00 E+05	-	197	178
R00291	T010	S016	I007	27/09/98	45	2,4	60	-	8,33 E+03	4,63 E+03	5,00 E+05	-	193	172
R00292	T010	S016	I007	27/09/98	0	1,7	35	-	1,43 E+04	4,64 E+03	5,00 E+05	-	172	149
R00293	T010	S017	I007	27/09/98	0	1,7	42	-	1,19 E+04	2,99 E+03	5,00 E+05	-	162	140
R00294	T010	S017	I007	27/09/98	45	2,4	86	-	5,81 E+03	3,01 E+03	5,00 E+05	-	225	206
R00295	T010	S017	I007	27/09/98	60	3,4	118	-	4,24 E+03	3,04 E+03	5,00 E+05	-	255	239

Ion ID	Specy	Energy MeV	LET Mev/mg/cm²	Range µm
I004	40-Ar	150	14,1	42
I005	20-Ne	78	5,85	45
I003	84-Kr	316	34	43
I007	10-B	41	1,7	80

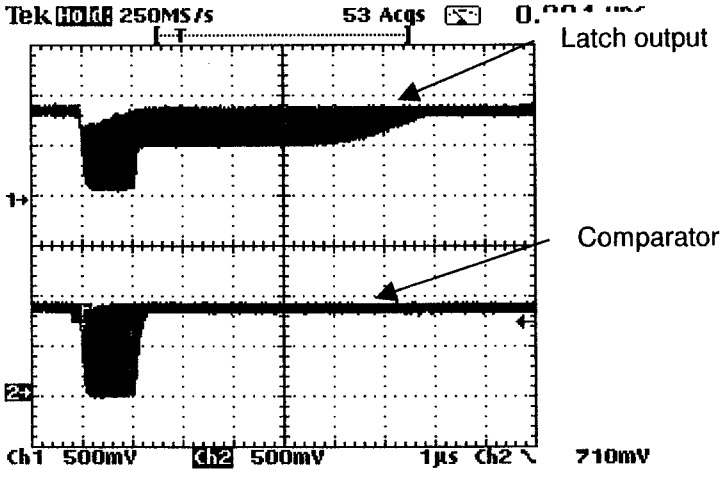
Sample ID	SN	Part Type	Date Code	Comments
S016	#576	PM139	9524A	Analog devices / PMI
S017	#679	PM139	9524A	Analog devices / PMI

Note	Condition 1 :	VI1	+ input	100mV
		VI2	- input	50mV



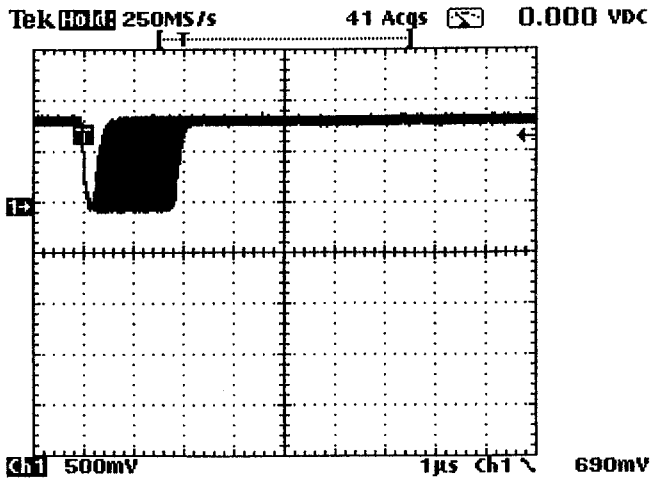
(5V/div 2µs)
In this case, the change of the latch state can be observed

Figure VI-2 – Typical Waveform, Virgo configuration without filter capacitor



(5V/div 2µs)
This scope record shows that the latch output change
does not latch thanks to the filtering capacitor

Figure VI-3 – Typical Waveform, Virgo configuration with 1nF capacitor filter



(5V/div 1µs)
This scope record shows the envelop of SEU pulses of different transient duration

Figure VI-4 – Typical Waveform, Comparator configuration

VII. CONCLUSION

SEU test have been conducted on PM139 Quad Voltage Comparator from Analog Devices, using the heavy ions available at the University of Louvain facility.

SEU susceptibility was obtained through the error cross section versus LET curve for two different test configurations.

The effect of a capacitor filter applied in the Virgo equivalent configuration has been assessed and drastic improvement has been obtained.

With these results, upset predictions on XMM orbit, can be performed for each error type and the risk associated with the present Virgo design can be assessed.