Radiation SEE Characterisation of ADSP-21020 Digital Signal Processors.

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Abstract

This paper presents Cf-252 and heavy ion Single Event Effects results obtained on commercially available ADSP-21020 Digital Signal Processors from Analog Devices. Register testing and register test results from three lots are compared and discussed.

I. Introduction

Radiation performance verification is one of the key elements in the development of a European radiation tolerant high performance 32-bit floating-point Digital Signal Processor (DSP). This project, both ESA and EC sponsored, transfers the US Analog Devices 21020 DSP design into a European semiconductor foundry having a suitable process for space qualification. The European DSP, the TSC21020E, will be manufactured by TEMIC/Matra MHS using their SCMOS 2RT+, 0.6 micron, 1 poly/3 metal process. In parallel with the design transfer, large efforts were put into the development of radiation test boards and test systems for verification tests.

One test system, the Single Event Effects (SEE) system, developed by Fraunhofer/IMS2 in Dresden, has been used during Californium-252 laboratory testing at ESTEC and during two heavy ion test campaigns, one at Brookhaven National Laboratory (BNL), USA and one at University Catholique de Louvain (UCL), Belgium. Results from the Cf-252 and BNL testing, which covered Register SEE testing of commercially available ADSP21020 DSP's from Analog Devices, will be presented here. The Cf-252 results are presented in a summary format whereas the heavy ion results are detailed in depth. The SEE test system and test conditions used will only be briefly described as a recent paper, presented at the 3rd ESA Electronic Components Conference, April 1997, covers these issues [1].

In support of one of the first TSC21020E users, the ESA Automated Transfer Vehicle (ATV) project, two Analog Devices ADSP-21020 DSPs from a flight demonstration lot were initially SEE characterised. These DSPs were primarily SEE tested in order to characterise their latch-up behaviour and to get a first impression of their Single Event Upset (SEU) sensitivity. In addition and for comparison, devices from other lots were also tested at the same time. In total, data are presented for four lots based on date codes: the ATV lot "A" d/c 9211/9528, a second lot "B" d/c 9426, a third lot "B1" d/c 9211/9502 and a fourth lot "C" d/c 9623. The three first lots use Analog Devices Revision 1 die; the 1996 lot, representing the latest Analog Devices re-design with DSP's processed and assembled at the new Singapore foundry, uses Revision 3 die.

II. Devices

Initially only the external marking could be used as a "lot" identifier so the following classifications were used:

Lot "A" ADSP-21020 TG-80/883B DI/B32744 G 2A
921/9528 (ATV) s/n : AT1 & AT2.

Lot "B" ADSP-21020 TG-120/883B DI/B46880 C 4A
9426 s/n : B01, B02, B03 & B04.

Lot "B1" ADSP-21020 TG-120/883B DI/B32744 C 2A
9211/9502 s/n : B30, B35 & B36.

Lot "C" ADSP-21020 KG-133 I I/P54921-3.0 9623
(Singapore) s/n : C01 to C10.

All types were packaged in 223-pin ceramic PGA's, cavity down.

It was also known, that the first three lot had dies from an earlier mask design - Revision 1, whereas lot "C" had die from the new mask design - Revision 3.

In order to explain the different radiation responses, a comparative construction analysis was carried out at NMRC, Ireland, on lot "A", lot "B" and lot "C" devices. This analysis confirmed that both "A" and "B" devices were essentially the same. They had identical die surface markings. Metallisation structure, widths and spacing were the same. Polysilicon width is 0.7 um. Both types were fabricated without an epitaxial layer. The p-type substrate concentration is approximately 1.5 x 10^{15} cc^{-3} with an n-well depth of approximately 4.8 um in both cases.

The "C" type is also fabricated using a double metal, single polysilicon 0.7 um CMOS technology. However this device has an epitaxial layer depth of approximately 12 um with a p-type substrate concentration of approximately 4 x 10^{18} cc^{-3}. The n-well depth is approximately 2.7 um. The metallisation structure is also slightly different to the other two devices, while the die surface markings show a mask date of 1995 as opposed to 1991.

III. SEE Test System and "Register Test"

As detailed in [1], the SEE test system uses a 2-processor distributed system consisting of a host Personal Computer (PC), a commercial available transputer board and a dedicated DSP test board, with the 21020 DSP installed cavity down. A 3-way channel communication link connects the host PC and the DSP test board together.

In summary, the DSP or Device Under Test (DUT) is interfaced with programme and data memory banks, boot-up circuitry and dual port memory for communication with the host PC. Serial links (at 10Mb/s) are implemented for data transfer between the DUT board and the host PC covering; loading of programme code, its execution and reporting of SEE events. The transputer board is used mainly to drive the serial links and execute the real time part of the host application. The MMI and file transfer operations are handled by the PC. Due to the high throughput authorised by the serial links, a high interaction between the control system and the DUT board is possible and allows the transfer of extensive messages and events.

The test board consists of 2 PCB boards of 160 mm x 233 mm connected together and a exchangeable DUT board of 83 mm x 83 mm carrying a 21020 DSP. As these DSP's are packaged in 223-pin ceramic PGA's cavity down, the DUT board has been designed with a rectangular hole of 24 mm x 24 mm allowing particle SEE testing to be carried out, see Figure 1. Exchangeable DUT boards allow adaptation to other type of packages such as MQFP.

Further hardware and software features incorporated in this design can be found in [1], however, for the "Register Test" as used here, the following can be summarised: In general, this programme loads a known test pattern into testable registers and check for errors. The used version tests 160 registers which cover a total of 4608 bits. Continuous and automatic testing is assured by a latch-up protection system and a watch-dog timer. Test parameters used and error types recorded are -

Test Parameters

+VDD	- +5.0 V
+Clock speed	- 16MHz
+RT cycle time	- 1000 ms
+Latch-up triggering	- 228 mA (BNL)
+Latch-up timing	- 1ms
+Watch-dog timing	- 1ms
+Test Pattern	- AA or 55

Error Grouping

+SEU	-	Register Errors (4608 bits)
+0-1	-	bit changed from 0 to 1
+1-0	-	bit changed from 1 to 0
+MU	-	Multiple bit flips
+SEL	-	Latch-up, high I
+Wd	-	Watch-Dog time out errors
+CC	-	Corrupted Control Flow
+AE	-	Address Errors
+DS	-	Failed DSP response

During a SEE test, test information and test progress are displayed on the PC in real time and two files, a test information file and a error protocol file, are stored on the PC. The test information file stores general information related to a test whereas the error protocol file collects all information received from the DSP.

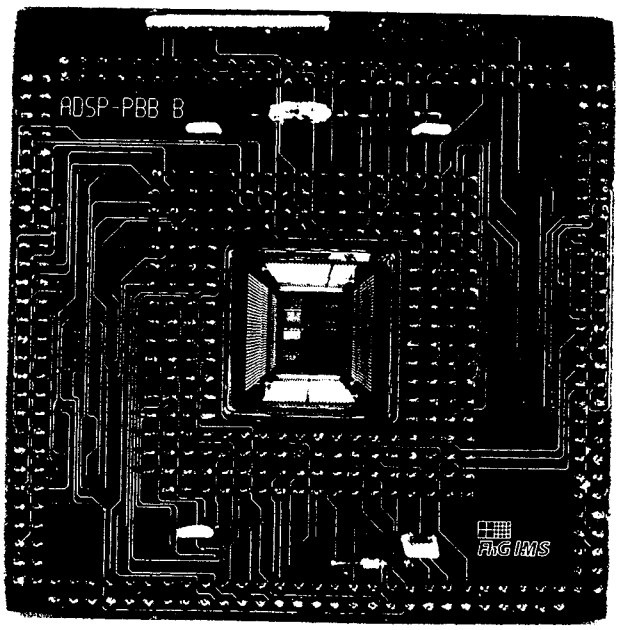

Figure 1. 21020 DUT test board lay-out.
PCB size 83 x 83 mm.

ATV ADSP-21020 TG-80/883B DI/B32744 G 2A 9211/9528												
Latch-up triggering level 228 mA.												
File	Fluence	SEU	0-1	1-0	Per Bit	SEL	Device	CC	Wd	AE	DS	MU
A0x	4629582	6394	1334	5060	**3.0E-7**	1937	**4.2E-4**	223	153	121	88	0
Latch-up triggering level 203 mA.												
File	Fluence	SEU	0-1	1-0	Per Bit	SEL	Device	CC	Wd	AE	DS	MU
A0x	3239049	4813	1043	3770	**3.2E-7**	1910	**5.9E-4**	171	112	74	60	2

Table 1A. "CASE" Summary Results Lot "A", Analog Devices Revision 1 die.

AD ADSP-21020 TG120/883B DI/B46880 C 4A 9426												
Latch-up triggering level 228 mA.												
File	Fluence	SEU	0-1	1-0	Per Bit	SEL	Device	CC	Wd	AE	DS	MU
B0x	2334412	3091	689	2402	**2.9E-7**	159	**6.8E-5**	98	77	48	44	0
Latch-up triggering level 240 mA.												
File	Fluence	SEU	0-1	1-0	Per Bit	SEL	Device	CC	Wd	AE	DS	MU
B03	5888451	6746	1524	5222	**2.5E-7**	420	**7.1E-5**	225	133	100	115	1
Latch-up triggering level 150 mA.												
File	Fluence	SEU	0-1	1-0	Per Bit	SEL	Device	CC	Wd	AE	DS	MU
B03	2871353	3456	762	2694	**2.6E-7**	218	**7.6E-5**	113	64	35	27	0

Table 1B. "CASE" Summary Results Lot "B", Analog Devices - Revision 1 die.

AD ADSP-21020 TG120/883B DI/B32744 C 2A 9211/9502												
Latch-up triggering level 228 mA.												
File	Fluence	SEU	0-1	1-0	Per Bit	SEL	Device	CC	Wd	AE	DS	MU
B35	358280	431	93	338	**2.6E-7**	133	**3.7E-4**	13	5	10	8	0
Latch-up triggering level 240 mA.												
File	Fluence	SEU	0-1	1-0	Per Bit	SEL	Device	CC	Wd	AE	DS	MU
B36	2260555	2029	428	1601	**2.0E-7**	711	**3.1E-4**	70	35	28	26	0

Table 1C. "CASE" Summary Results Lot "B1", Analog Devices - Revision 1 die.

AD ADSP-21020 KG-133 I/P54921-3.0 9623												
Latch-up triggering level 228 mA.												
File	Fluence	SEU	0-1	1-0	Per Bit	SEL	Device	CC	Wd	AE	DS	MU
C0x	647660	703	128	575	**2.4E-7**	2	**3.1E-6**	14	13	9	10	0
Latch-up triggering level 203 mA.												
File	Fluence	SEU	0-1	1-0	Per Bit	SEL	Device	CC	Wd	AE	DS	MU
C0x	2659874	2635	408	2227	**2.2E-7**	2	**7.5E-7**	77	30	36	40	0
Latch-up triggering level 240 mA.												
File	Fluence	SEU	0-1	1-0	Per Bit	SEL	Device	CC	Wd	AE	DS	MU
C0x	3635273	3455	553	2913	**2.1E-7**	0	**2.8E-7**	79	45	46	37	1
Latch-up triggering level 150 mA.												
File	Fluence	SEU	0-1	1-0	Per Bit	SEL	Device	CC	Wd	AE	DS	MU
C0x	5800762	5350	831	4519	**2.0E-7**	30	**5.2E-6**	118	65	47	54	0

Table 1D. "CASE" Summary Results Lot "C", Analog Devices - Revision 3 die.

IV. Test Conditions and Test Facilities

All results presented here were obtained with VDD = 5.0 Volt at the DSP and running the same Register test programme. Test pattern used were either AAAAAAAA or 55555555, thus always a 50/50 pattern.

"CASE"

Californium-252 Assessment of Single-event Effects (CASE) were carried out at the ESTEC/QCA facility by using a 1.78 microcurie source. Testing was carried out in vacuum with fission fragment fluxes ranging from 475 to 2756 ions/cm^2/min. The average Linear Energy Transfer (LET) of Cf-252 at the surface of the DUT is 43.0 MeV/(mg/cm^2).

Heavy Ion

SEE heavy ion testing was carried out at the twin Tandem Van de Graff accelerator at BNL. The dedicated SEU test facility in target room 4 was used. Testing was carried out with ^{19}F ions at 80 MeV, ^{28}Si ions at 186 MeV, ^{35}Cl ions at 208 MeV and ^{56}Fe ions at 248 MeV covering a LET range of 5.21 to 42.3 MeV/(mg/cm^2). Testing was carried out in August 1996, ref. (BNL9608).

V. SEE Test Results

"CASE"

Initial experience in SEE testing ADSP-21020 DSP was obtained during a large number of tests carried out at the ESTEC "CASE" facility [2]. Testing covered different test conditions in order to optimise test settings and assess reliable running. Test results for the various lots and different test conditions have been summarised in Table 1A to 1D. Devices tested (file), Fluence in particles per cm^2, number of register SEUs, 0-1/1-0 transitions, register cross section results per cm^2, number of SELs, latch-up cross section results per device and numbers of other types of errors can be found in these tables. With latch-up behaviour being of particular concern, each table presents the SEE results against the latch-up protection level used. As can be seen from these tables, fairly consistent SEU data were obtained within each mask group whereas some variation in SEL is apparent. If we consider the Revision 1 lots (Table 1A to 1C), the ATV tested devices, lot "A", showed the highest SEU cross section sensitivity, with values between 3.2 E-7 to 3.0 E-7 cm^2/per bit. Lot "B" showed slightly lower cross section values ranging from 2.9E-7 to 2.5E-7 cm^2/per bit and lot "B1" the lowest with values between 2.6E-7 to 2.0E-7 cm^2/per bit. Altogether fairly consistent results when considering device/lot/test variations. The cross section results for Revision 3 (lot "C") appear to be slightly less sensitive with values ranging from 2.4E-7 to 2.0E-7 cm^2/per bit. In general very uneven 0-1/1-0 bit error distributions were noted. The 0-1/1-0 ratio for Revision 1 devices balance around a ratio of 21/79 and Revision 3 devices to a ratio of 15/85.

From the tables significant change in latch-up sensitivity is noticeable. Each lot shows the highest SEL value at the lowest triggering level, thus indicating that higher triggering levels should have been selected. However, when comparing the SEL results per triggering level, lot "A" appears to be the most sensitive with values around 4 to 6E-4 cm^2/per device followed by lot "B1" with values around 3 to 4E-4 cm^2/per device and lot "B" with values around 7 to 8E-5 cm^2/per device. The improved SEL sensitivity of lot "C", with values around 5E-6 to 3E-7 cm^2/per device, match very well with the technology data retrived from the construction analysis as given in section II. So in general for the "CASE" tests, Revision 3 devices appear less sensitive to SEE effects.

Heavy Ion

Two devices from each of lots "A", "B" and "C" were heavy ion tested at BNL. SEE results were obtained as given in graphical form in Figures 2 to 7. These graphs show, as a function of ion LET, the SEE cross section sensitivity per cm^2 per bit or per device. All data points shown correspond to an average value derived from all tests at that particular LET.

With SEE data presented in one graph, as shown in Figure 2 for lot "A", and in Figure 3 for lot "C", a direct comparison of the different sensitivities can be viewed. Results for lot "B" are very similar to the "A" behaviour, expect for SELs, so no "B" graph has been included. SEE results for all three lots have been further compared in Figures 4 to 7. Register 0 to 1 and 1 to 0 SEU transitions per bit can be found in Figure 4, register results per device in Figure 5, non register results per device in Figure 6 and SEL results per device in Figure 7.

In Figures 2 and 3, SEE results have been grouped as; register SEUs, non register SEUs and SELs. Register SEUs include both 0-1 and 1-0 errors whereas non register SEUs are all other errors grouped together. Include here are the number of corrupted control flows, watch-dog reset errors, address errors and failing DSP responses. Finally the graphs have been completed with the latch-up sensitivity.

In general for lot "A", a register SEU threshold was observed around a LET of 5.0 MeV/(mg/cm^2) with a saturated cross section level of about 3E-3 cm^2/device. As further shown in Figure 4, there is a strong tendency for 1 to 0 bit flips resulting in a much lower 0 to 1 bit flip rate with a threshold LET value around 11.5 MeV/(mg/cm^2). The transition ratio changes from approximately 1 to 99 at the 0 to 1 LET threshold, then shows a short constant region of about 40/60 and finally arriving at a ratio of about 15/85, a value not so far away from the Cf-252 ratio of 21/79. The register SEU statistics at higher LETs become poor due to increased latch-up sensitivity. The SEL threshold LET was found to be around 16.0 MeV/(mg/cm^2) since only one SEL was recorded

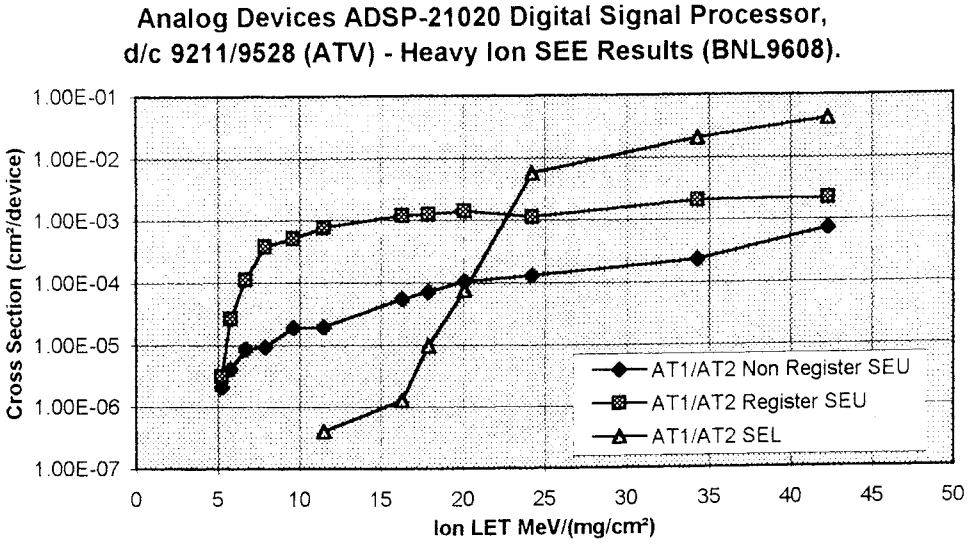

Figure 2. Lot "A" Revision 1 SEE results presented as cross section (cm²/device).

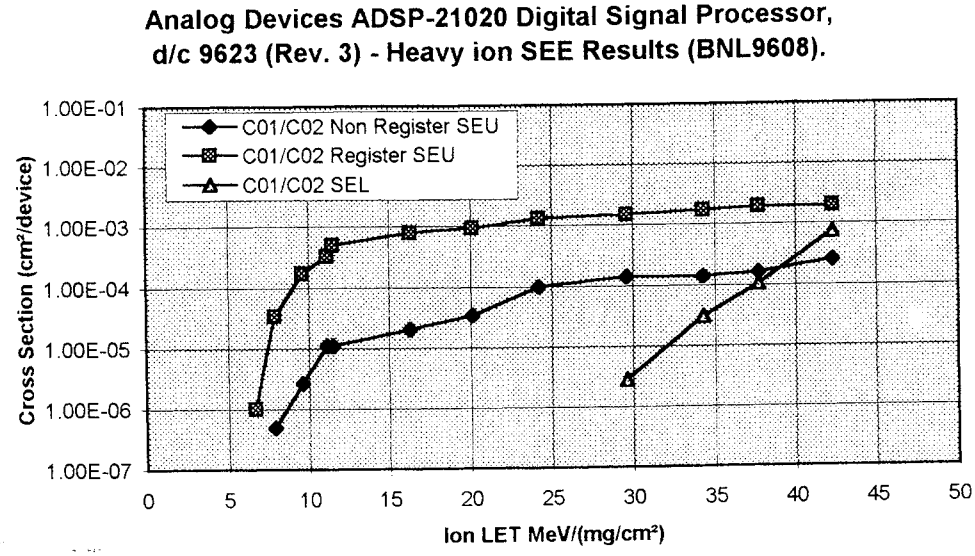

Figure 3. Lot "C" Revision 3 SEE results presented as cross section (cm²/device).

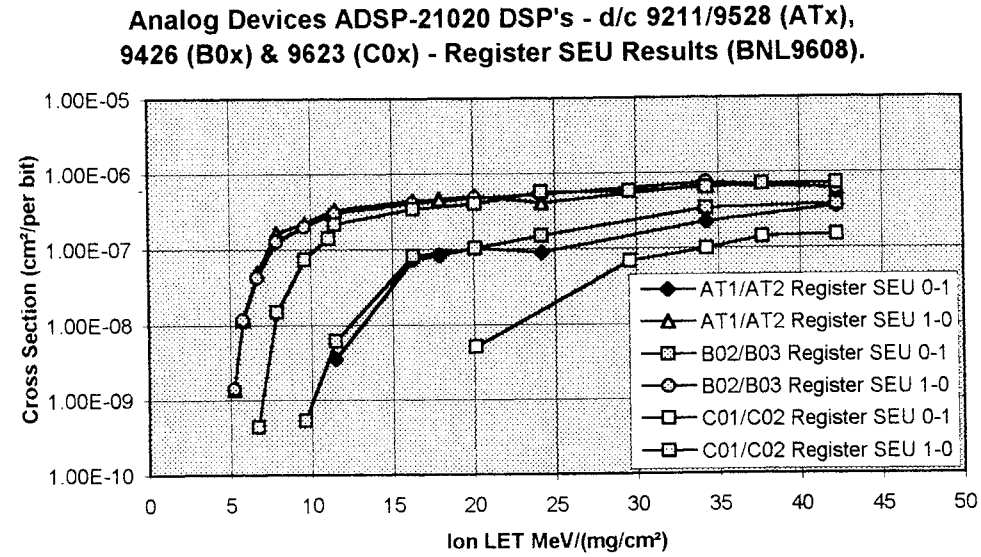

Figure 4. 0-1/1-0 Register SEU cross section (cm²/bit) for the three lots tested.

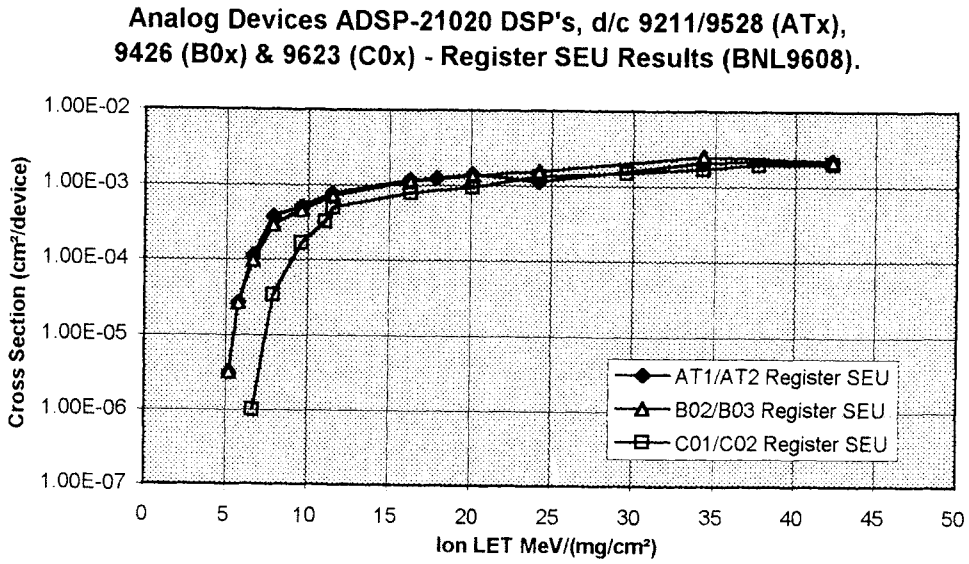

Figure 5. Register SEU cross section (cm²/device) for the three lots tested.

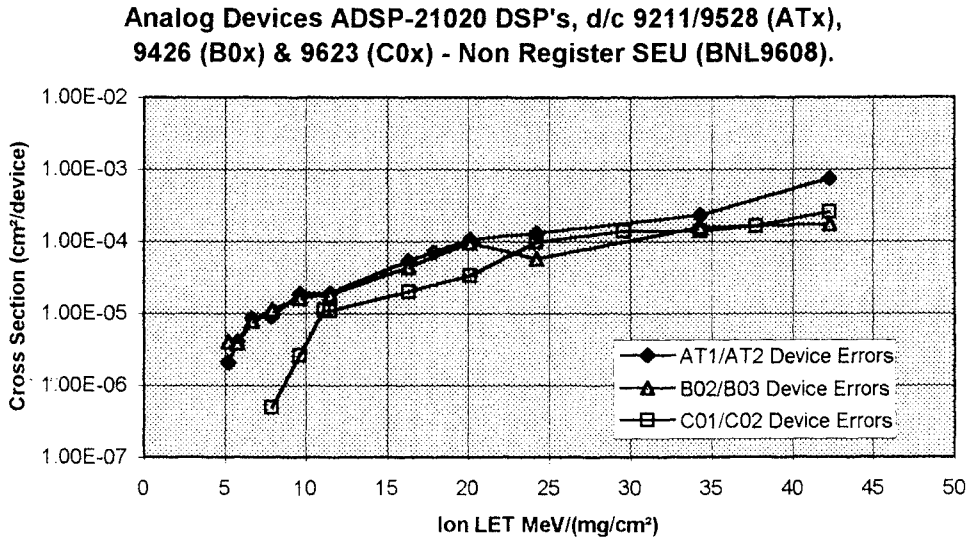

Figure 6. Non Register SEU cross section (cm²/device) for the three lots tested.

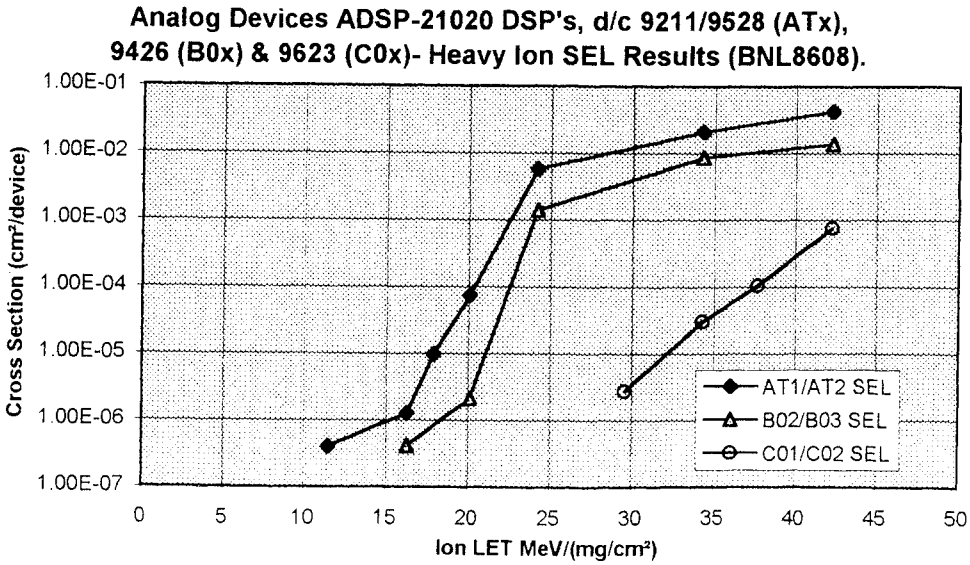

Figure7. Latch-up SEL cross section (cm²/device) for the three lots tested.

at the lower LET 11.5 MeV/(mg/cm²). The SEL sensitivity curve rises rapidly towards a saturated cross section level of >4.0E-2 cm²/device where the average latch-up rate, at a LET of 42.3 MeV/(mg/cm²), is one per 23 ions/cm² ! Testing at higher LETs gets complicated due to the recovery time needed. At this LET the effective test time has been reduced to 27 % and shows a SEU/SEL error ratio of 5/95 or 1 SEU per 19 SELs ! Hence no testing was carried out beyond this point.

Lot "C" results appear to be slightly better with a register SEU threshold around a LET of 7.0 MeV/(mg/cm²), however, with a very similar saturated cross section level of about 3E-3 cm²/device. As further shown in Figures 4 to 7, also the 0 to 1 and 1 to 0 transitions change in a better direction, higher LET, as well as the register SEUs and non register SEUs, as further evident from Figure 5 and Figure 6, respectively. The change in latch-up sensitivity is noticeable as can be seen in Figure 7. Here a LET threshold of about 30 MeV/(mg/cm²) can be reported. This value, compared to the SEL results for the two other lots, is well understood when considering the technology information given in section II.

Apart from the SEL differences, lot "B" results for register SEUs, 0-1/1-0 transitions SEUs and non register SEUs, come very close to the "A" tested devices as evidenced in Figures 4 to 6. These results, both LET threshold and cross section values, come very close to values previously published by F. Bezerra et.al.[3].

VI. Conclusions

With the verification of the SEE test system, the "Register test" programme and the SEE characterisation of three Analog Devices lots, the basic ground work has been performed for a full SEE characterisation of the TSC21020E, the European, radiation tolerant, high performance, 32-bit floating-point, DSP. Additionally, the SEE characterisation of both Revision 1 and Revision 3 devices have contributed significantly to our knowledge on the usage of ADSP-21020 in space. Obviously if Analog Devices ADSP21020 DSPs need to fly, Revision 3 devices will be favoured, however, SEE verification characterisation, mission prediction and the use of a latch-up protection system, are minimum precautions to take in order to work towards mission success.

VII. References

[1] R. Harboe-Sørensen, P. Armbruster, T. Müller, H. G . Despang, P. Nauber, "Californium-252 SEE Evaluation of 32-bit Floating Point DSP Test System", Paper Presented at the 3rd EECC, ESTEC, April 1997.

[2] R. Harboe-Sorensen, "Test Methods for Single Event Upset/Latch-up", Radiat. Phys. Chem. Vol. 43, No 1-2, pp 165-74, 1994.

[3] F. Bezerra, D. Hardy, R. Velazco and H. Ziade, "Tilmicro, A New SEU and Latch-up Tester for Microprocessors. Initial Results on 32-bit Floating Point DSPs", RADECS'95,Arcachon, France, Sep. 1995, pp 296-301.