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EUROPEAN SPACE AGENCY CONTRACT REPORT

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Title

AM29F800B-120SC, 8 MBIT FLASH FROM AMD
AM29LV800B-120SC, 8 MBIT FLASH FROM AMD

TOTAL IONISING DOSE CHARACTERIZATION TEST REPORT

ESA/ESTEC Contract No. 11755/95/NL/NB-WO1/CO1

	Name and Function	Date	Signature
Prepared by :	SALMINEN A. Project manager	20/10/97	
Verified by :	DOUCIN B. (HMS)	01/12/97	
Approved by :	CARLOTTI C (HMS)	2/12/97	
Authorized by :	HARBOE SØRENSEN R. ESTEC Technical Officer		
Application authorized by :			

Document type	Nb WBS	Summary: 5 V and 3.3 V memories were tested under total ionising dose irradiation to study the effect of supply voltage on the radiation sensitivity. This report presents the results obtained on 8 Mbit AMD FLASH.

SUMMARY OF RESULTS

Test sample characteristics :

Part Name :	AM29F800B-120SC AM29LV800B-120SC	**Function :**	1 M x 8 Flash
Technology :	CMOS, 0.5 µm	**Package :**	48-pin plastic TSOP
Manufacturer :	AMD	**Location :**	USA
Sample size :	3 (5 V), 3 (3.3 V)	**Date Code :**	9620 (5V), 9625 (3.3V)

TID test results

Functional test

The following table summarises the failure doses of TID test:

S/N	V_{CC} V	Dose at failure krad(Si)	Annealing	Remarks
06	**5**	29.9	No functional recovery	Erasure failure
07	**5**	29.9	No functional recovery	Erasure failure
08	**5**	29.9	No functional recovery	Erasure failure
24	**3.3**	20.4	No functional recovery	Erasure failure
25	**3.3**	14.8	No functional recovery	Erasure failure
26	**3.3**	20.4	No functional recovery	Erasure failure

Only erasure failures were encountered. No read errors were detected during irradiation.

No devices recovered in the high temperature annealing of 168 h at 85°C.

Functional test conclusion

The results of these experiments demonstrate that 8 Mbit Flash AM29F800B-120SC from AMD, when biased at 5 V, is less sensitive to ionising radiation than AM29LV800B-120SC biased at 3.3 V.

Parametric test

The following table summarises the average dose levels for both bias at which sensitive parameters have drifted **20%**:

Symbol	Parameter	Dose Level/krad(Si)	
		V_{CC} = 5 V	V_{CC} = 3.3 V
I_{CCSB}	Standby Supply Current	35	>60
I_{CCOP}	Operating Supply Current	30	>60
V_{OL}	Output Voltage Low Level	35	35
V_{OH}	Output Voltage High Level	25	25
T_{ACS}	Chip Select Access Time	30	20

The parameters of the 5 V and 3.3 V devices remained stable up to the dose when the erasure failure occured. Standby and operational power supply currents are at a high level at maximum doses. Also output voltages indicated complete failure of the 3.3 V devices.

Parametric test conclusion

The results of these experiments demonstrate that there in no clear difference in the radiation sensitivity of 8 Mbit Flash AM29F800B-120SC AMD biased at 5 V and AM29LV800B-120SC biased at 3.3 V.

DOCUMENT CHANGE LOG

Issue/ Revision	Date	Modification Nb	Modified pages	Observations
1	20/10/97			Original Edition

PAGE ISSUE RECORD

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1. INTRODUCTION

The aim of this work is to investigate radiation effects in low voltage technologies. The study is focused on memory devices, which require lower voltage to achieve higher integration. Parts selected consists of SRAMs (1 Mbit, 2 types), DRAMs (16 Mbit, 2 types), and FLASH memories (8 Mbit, 2 types).

The object of this document is to describe the irradiations performed on the AMD 8 Mbit AM29F800B-120SC and AM29LV800B-120SC in order to measure their sensitivity to ionising radiation under the influence of two supply voltage levels.

Irradiations were performed in March 1997 (10^{th}-17^{th}) according to the procedures referenced in the following paragraph.

This work was performed in the frame of the WO1/CO1 for ESTEC Contract n°11755/95/NL/NB.

2. REFERENCE DOCUMENTS

[1] ESA/SCC 22900-4 ESA Basic Specification for Total Dose Steady-State Irradiation

[2] AMD Manufacturer Data Sheet

[3] Description of the VTT memory tester, AUT/PRO/76/96 (in Finnish)

3. PART DETAILS

3.1. DEVICE IDENTIFICATION

3.1.1. References

Type : AM29F800B-120SC
AM29LV800B-120SC
Manufacturer : AMD
Place : USA
Packaging : 44-pin plastic SOP

3.1.2. Function

1 M x 8 Bit Flash

3.1.3. Technology

CMOS, 0.5 µm (See next page for further details)

3.1.4. Part Procurement

Origin	:	VTT Automation, Finland
Level	:	Standard Level
Temperature range	:	0°C, +70°C (Industrial)
Date code	:	9625 (LV), 9620 (F)
Screening	:	/
Sample size	:	3 (biased at 5 V), 3 (biased at 3.3 V)
Manufacturer Marking	:	AM29LV800B-120SC 9620FGA, 1996 AMD (Low Voltage)
		AM29F800B-120SC 9625CGA, 1996 AMD (5 V)
Detailed specifications:		Manufacturer Data sheet

3.1.5. Previous TID details/history

No specific radiation data on these devices.

3.2. TECHNICAL INFORMATION

The functionality and the parametric integrity of the devices were examined prior to irradiation. No screening nor burn-in were carried out during this study.

General information

Name	AMD AM29(F/LV)800B-120
Package Marking	AM29F800B-120SC 9620FGA, 1996 AMD AM29LV800B-120SC 9625CGA L, 1996 AMD
Access time/ns at 5V	120
Temperature range/°C	0, +70
Organisation	1 M x 8 Bit
Supply Voltage/V	4.5-5.5/ 2.7-3.6

Technology

Name	AMD AM29(F/LV)800B-120
CMOS	yes
Epitaxial layer	*
Architecture	*
Design rules	CS29AF (0.5 µm)
Die size	5 mm x 10 mm (LV) 4.95 mm x 10.5 (F)
Cell size	*

* The missing information was unsuccessfully required from the manufacturer.

4. TEST DESCRIPTION

4.1. IRRADIATION FACILITY

Name MMS Cobalt 60-source, model Shepherd 484

Location Matra Marconi Space France
37, avenue Louis Bréguet
78146 VELIZY-VILLACOUBLAY Cedex
France

Activity < 8.9 curies.

Calibration 10/03/97.

4.2. TID TEST SET-UP

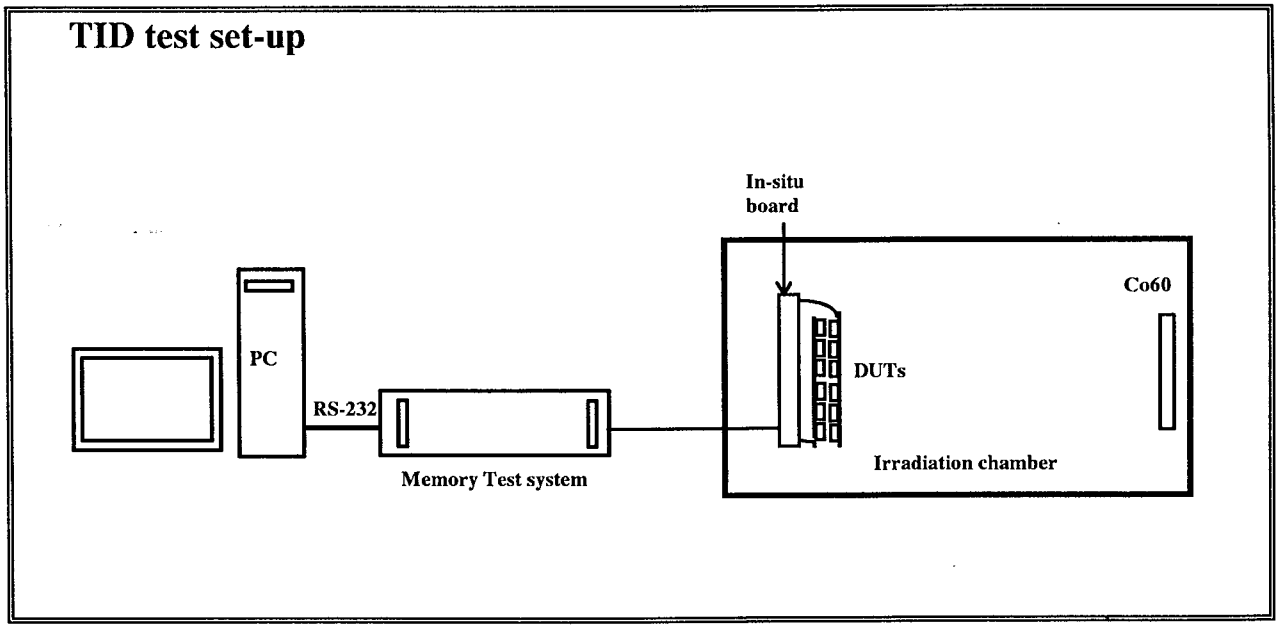

Fig. 1. Description of the TID test set-up.

The DUTs were soldered on small PCB's with pin headers. They were mounted on the two large PCB's that were biased at 5 V and 3.3 V. The distance from 5 V and 3.3 V devices were 2 mm from package to package. The difference in dose rates was taken into account when computing the doses received by the devices.

The device under test was selected by a chip select logic located in the In-situ board. The supply voltage was provided by the memory tester. A complete description of the memory tester is given in [3].

The test sequence flow chart is given in fig. 4.2.

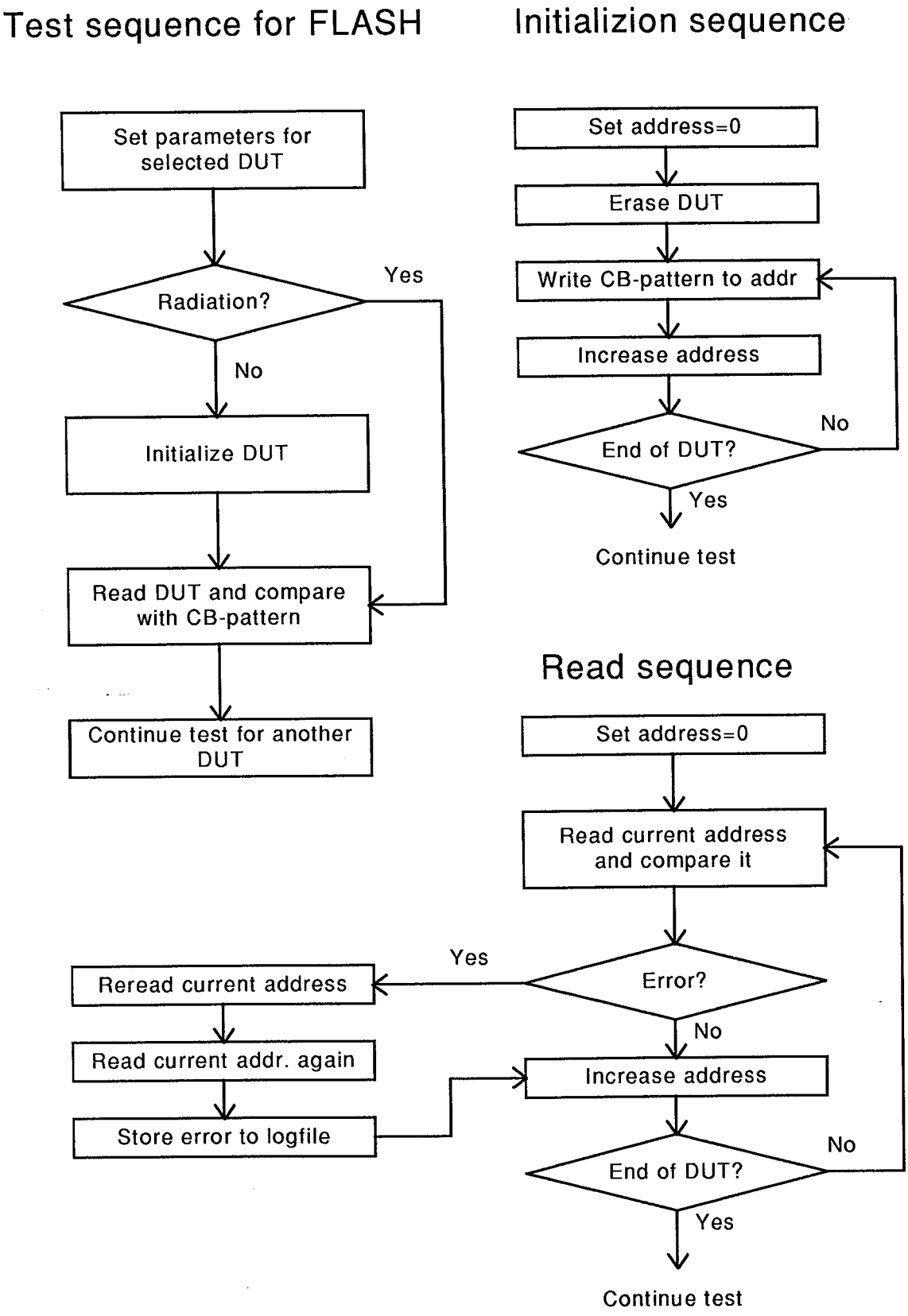

Fig. 4.2. The test sequence flow chart of an individual device with write and read sequencies.

The write and read cycles during functional test were as follows:

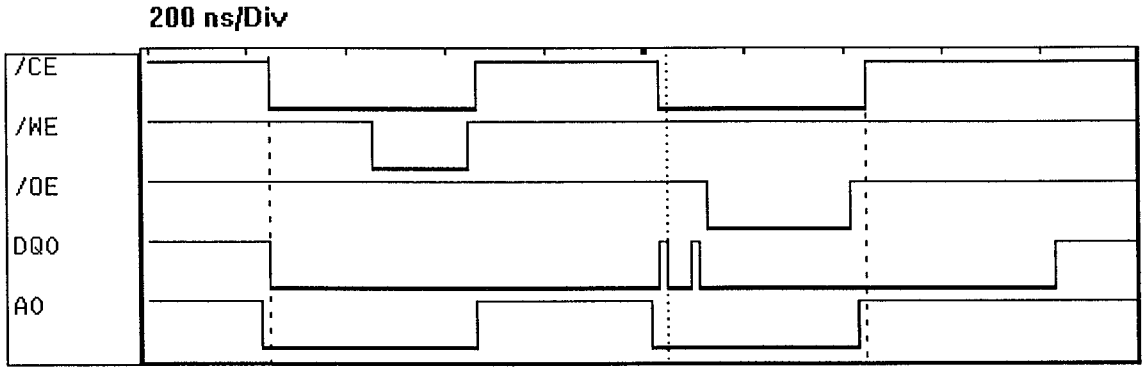

Fig. 4.3. Write Cycle of AMD Flash device during functional test.

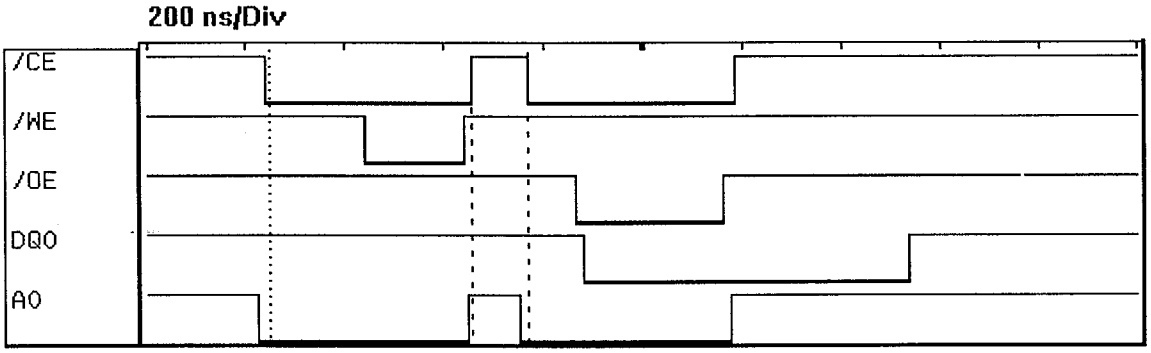

Fig. 4.4. Read Cycle of AMD Flash device during functional test.

5. TOTAL IONISING DOSE EXPERIMENTAL RESULTS

5.1. TID IRRADIATION TEST SEQUENCE

During irradiation all the devices were functionally tested 3 times per hour automatically in the exposure chamber, and the results were stored on a hard disk of the measuring computer. The memory test started with the write of a CB (checkerboard) pattern to the memory device. The erasure time was approx. 35 s and write time of a device was approx. 5 s. Thereafter the memory contents of the device was read and it was compared to the original pattern. In-situ in the irradiation chamber the memory devices were only read. Prior to parametric tests, the devices were systematically erased and rewritten.

If errors were encountered, the corrupted data was immediately reread. Due to the limitation of the measuring computer, the maximum number of recorded corrupted bytes was set to 100. TTL levels were applied in control, address and data signals. 5 V bias was applied to devices s/n 06-08 and 3.3 V bias was applied to devices s/n 24-26.

In the time between the irradiation, the parameters were measured (after erasure and rewritting of CB pattern) remotely at the end of each step within two hours with the VTT parametric tester in another room.. Except the measurement, the devices were unbiased during this time. The resolution of the voltage measurements was better than 1 mV.

The irradiation was accomplished in seven steps. The average dose rates were 420 rad(Si)/h and 410 rad(Si)/h for 5 V and 3.3 V devices, correspondingly. The dose rates and cumulative doses with durations of each irradiation are given in table 5.1.

Table 5.1. Dose rates, durations, and cumulative doses for 5 V and 3.3 V AMD Flash.

Step	Dose rate 5 V rad(Si)/h	Dose rate 3.3 V rad(Si)/h	Duration h	Total Dose 5 V krad(Si)	Total Dose 3.3 V krad(Si)
1	262	258.1	20.00	5.2	5.1
2	327.5	317.3	19.00	11.5	11.2
3	471.6	458.1	8.00	15.2	14.9
4	471.6	458.1	12.00	20.9	20.4
5	471.6	458.1	19.17	29.9	29.1
6	471.6	458.1	7.18	33.3	32.4
7	471.6	458.1	60.00	61.6	59.9

After the last irradiation step and parametric measurement, the devices were put into a heat chamber for an annealing period of 168 h at 85°C. The devices were biased continously and functionally tested 3

times per hour. The functional testing now included erasure operation. Otherwise the test set-up for the AMD Flash devices was the same one as during irradiation.

5.1.1. Problems encountered/Discussion

No specific problem was encountered during irradiations.

5.2. TID TEST RESULTS

Functional test

The following table summarises the failure doses of TID test:

S/N	V_{CC} V	Dose at failure krad(Si)	Annealing	Remarks
06	**5**	29.9	No functional recovery	Erasure failure
07	**5**	29.9	No functional recovery	Erasure failure
08	**5**	29.9	No functional recovery	Erasure failure
24	**3.3**	20.4	No functional recovery	Erasure failure
25	**3.3**	14.8	No functional recovery	Erasure failure
26	**3.3**	20.4	No functional recovery	Erasure failure

The devices failed due to the erasure failure that occured during parametric test. No read errors were encountered during irradiation.

Functional test conclusion

The results of these experiments demonstrate that on the average 8 Mbit Flash AM29F800B-120SC from AMD, when biased at 5 V, is less sensitive to ionising radiation than AM29LV800B-120SC biased at 3.3 V in terms of the erasure failure.

Parametric test

The following table summarises the average dose levels for both bias at which sensitive parameters have drifted **20%**:

Symbol	Parameter	Dose Level/krad(Si)	
		V_{CC} = 5 V	V_{CC} = 3.3 V
I_{CCSB}	Standby Supply Current	35	>60
I_{CCOP}	Operating Supply Current	30	>60
V_{OL}	Output Voltage Low Level	35	35
V_{OH}	Output Voltage High Level	25	25
T_{ACS}	Chip Select Access Time	30	20

Dramatic changes in supply currents and also in 3.3 V voltage parameters were measured when the devices had failed due to the erasure failure. Due to the loss of functionality the parameters do not describe the proper behaviour of the devices. No device recovered in the high temperature annealing.

Parametric test results are given as graphs in appendix 2.

Parametric test conclusion

The results of these experiments indicate that there in no clear difference in the radiation sensitivity of 8 Mbit Flash AM29F800B-120SC AMD biased at 5 V and AM29LV800B-120SC biased at 3.3 V.

6. CONCLUSION

Ionising dose tests were performed on the 8 Mbit AM29F800B-120SC and AM29LV800B-120SC Flash from AMD with 3.3 Vand 5 V bias.

The erasure failure makes the comparison of parametric performance of the devices difficult. In terms of erasure failure, the AM29F800B is less radiation sensitive compared to AM29LV800B: the failure dose of 5 V device was twice that of the 3.3 V device.

Further tests need to be done to reveal if there is difference in read errors.

APPENDIX 1. Parametric test results for AMD Flash devices.

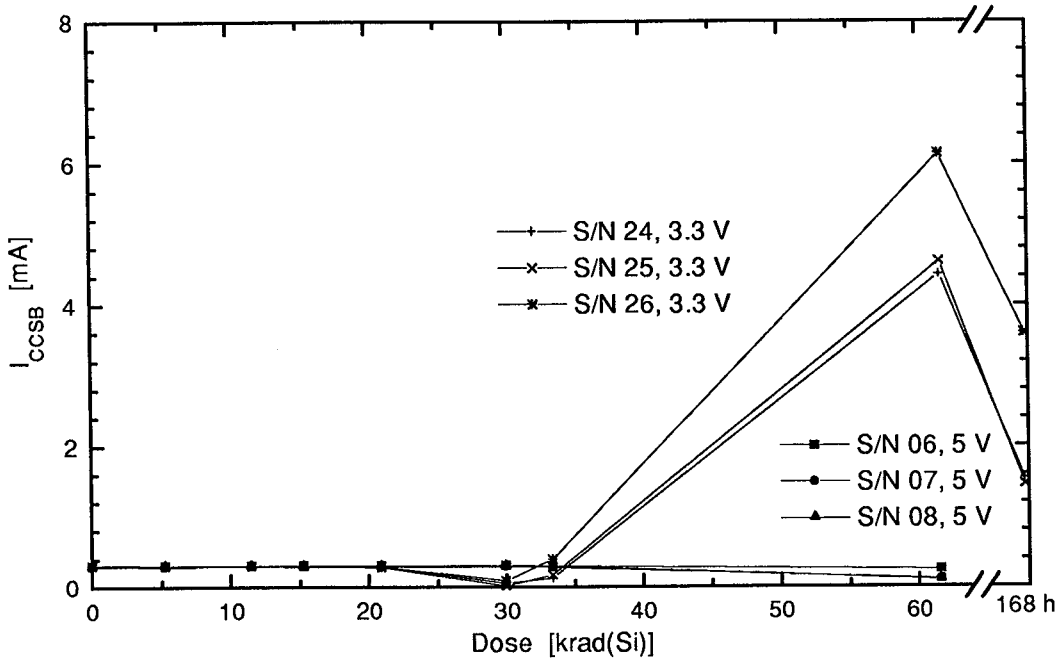

Fig. 1. Standby supply current versus dose and after annealing for AMD Flash devices.

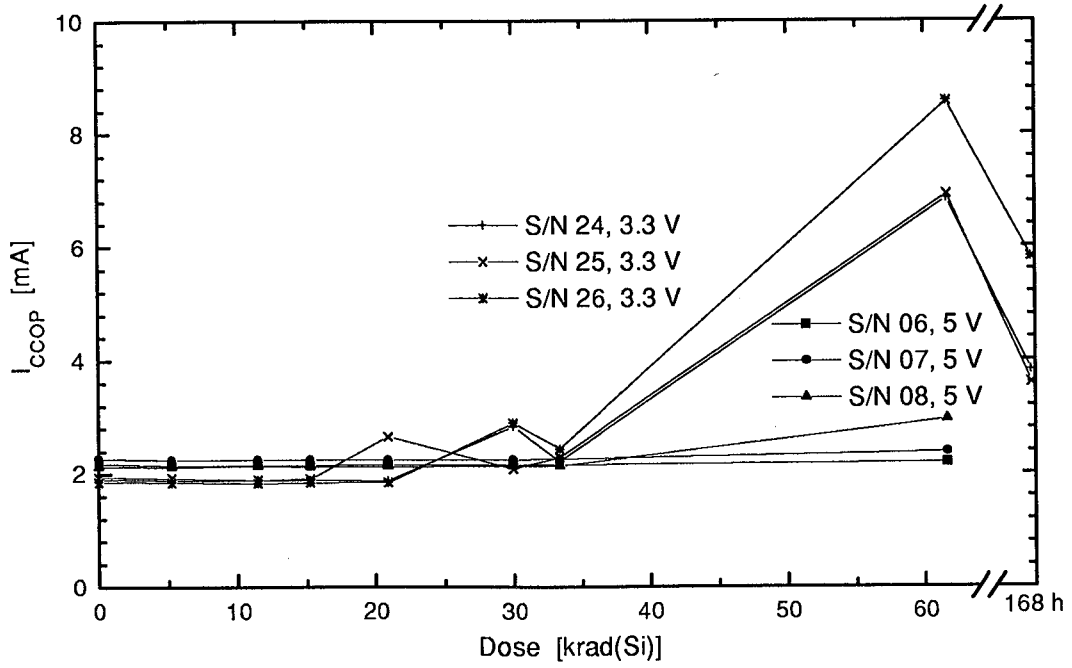

Fig. 2. Operating supply current versus dose and after annealing for AMD Flash devices.

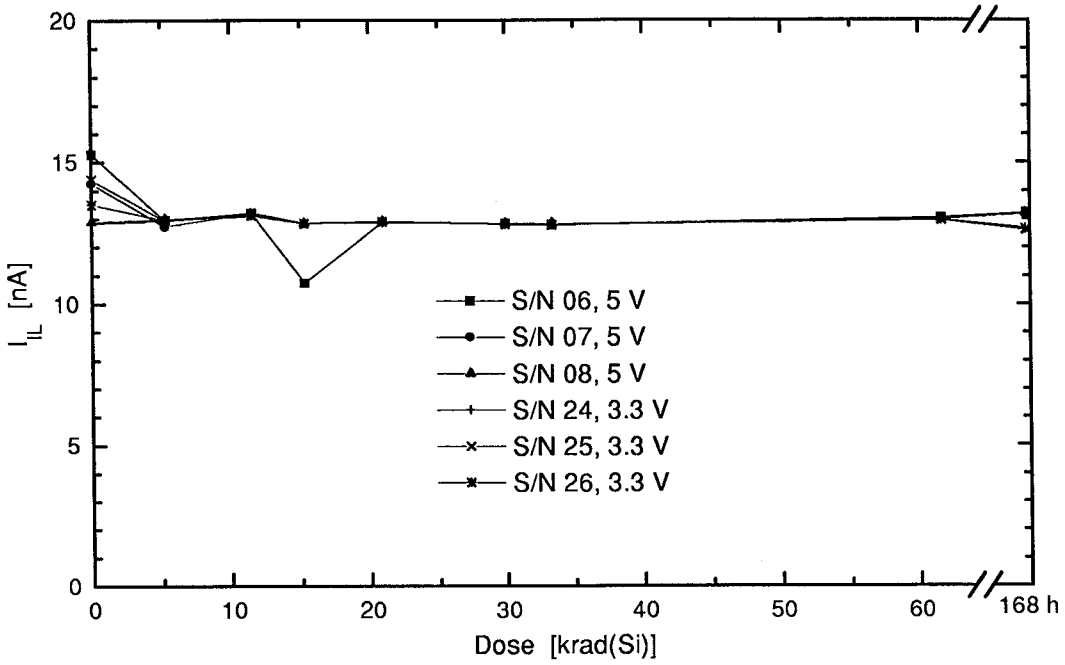

Fig. 3. Input current low level versus dose and after annealing for AMD Flash devices.

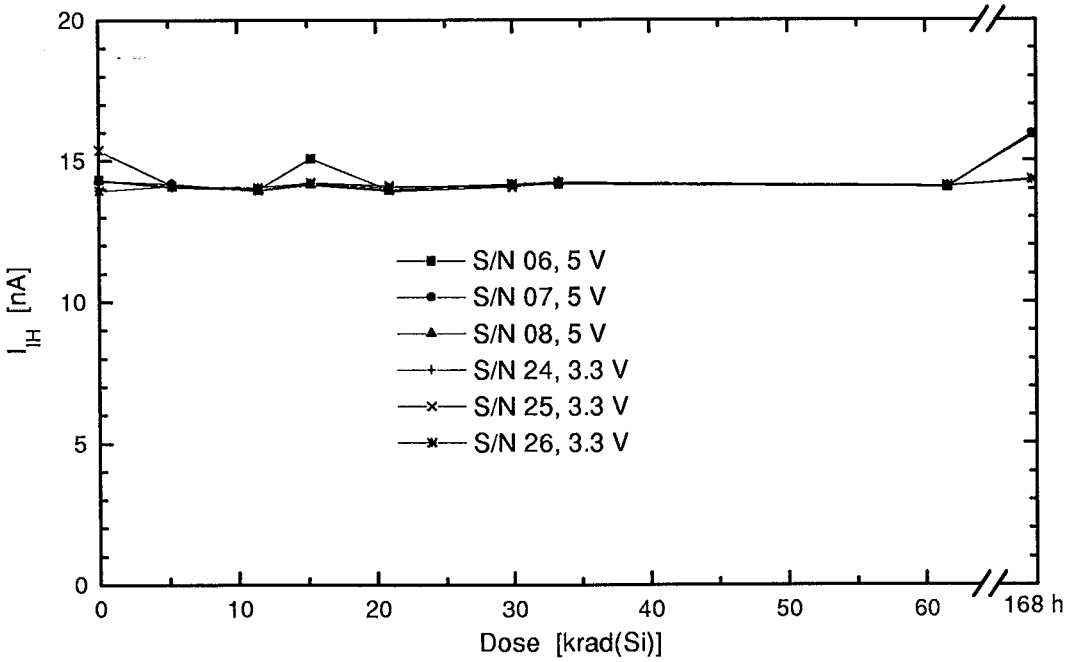

Fig. 4. Input current high level versus dose and after annealing for AMD Flash devices.

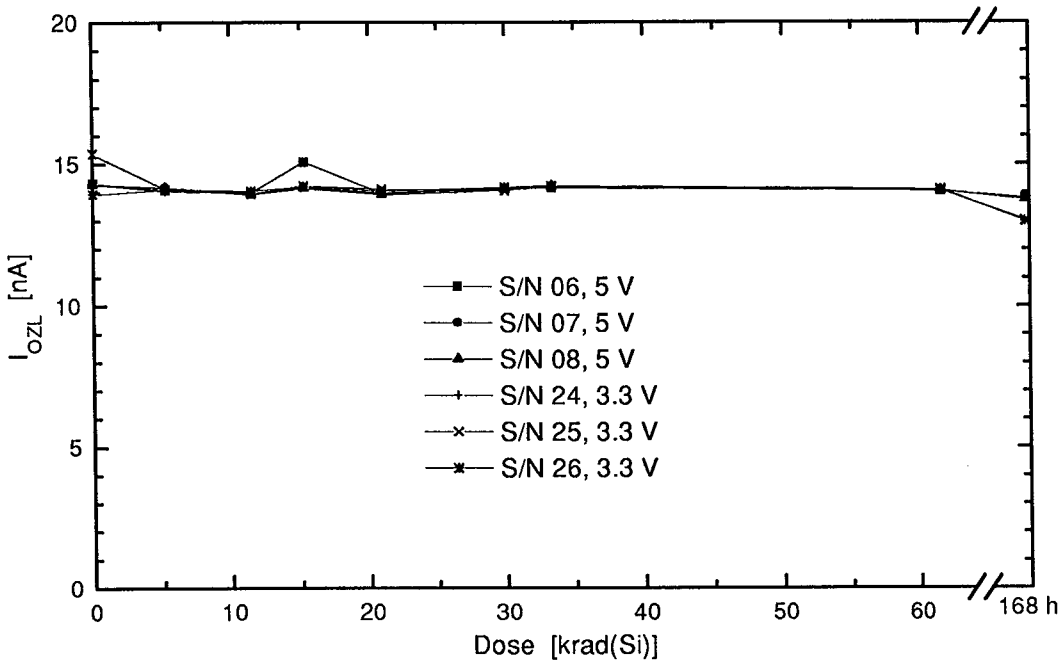

Fig. 5. Output leakage current third state low level applied versus dose and after annealing for AMD Flash devices.

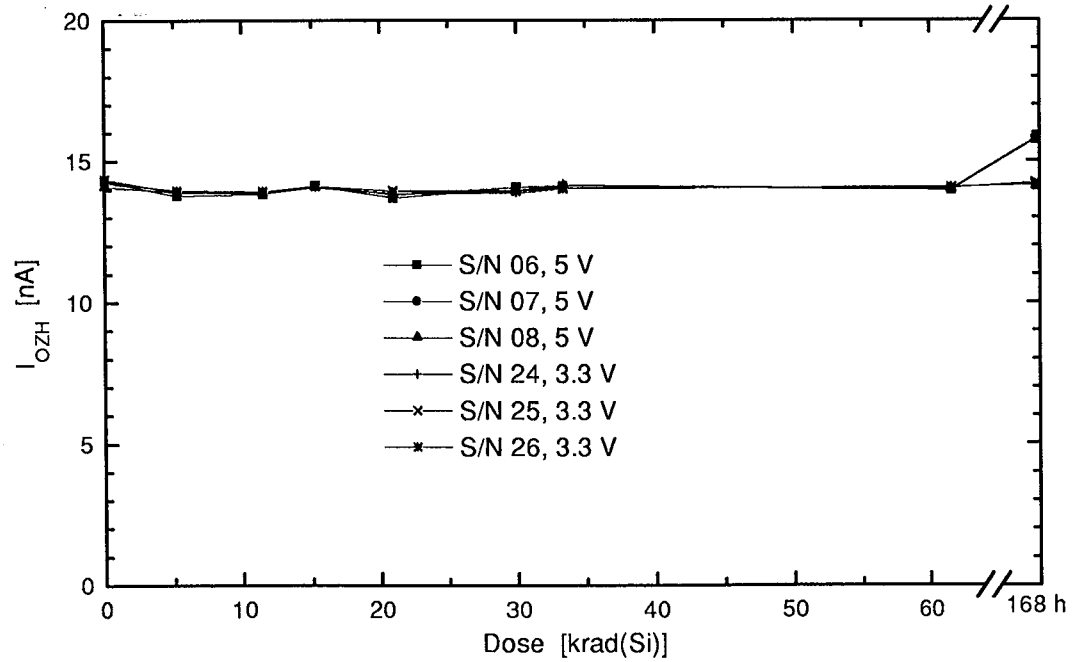

Fig. 6. Output leakage current third state high level applied versus dose and after annealing for AMD Flash devices.

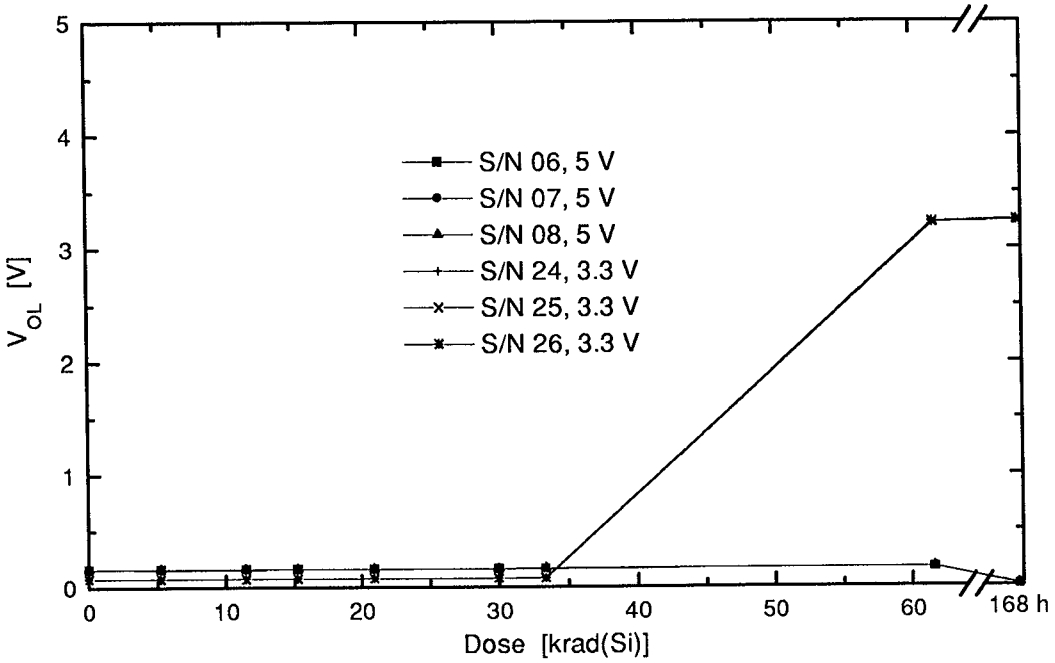

Fig. 7. Output voltage low level versus dose and after annealing for AMD Flash devices.

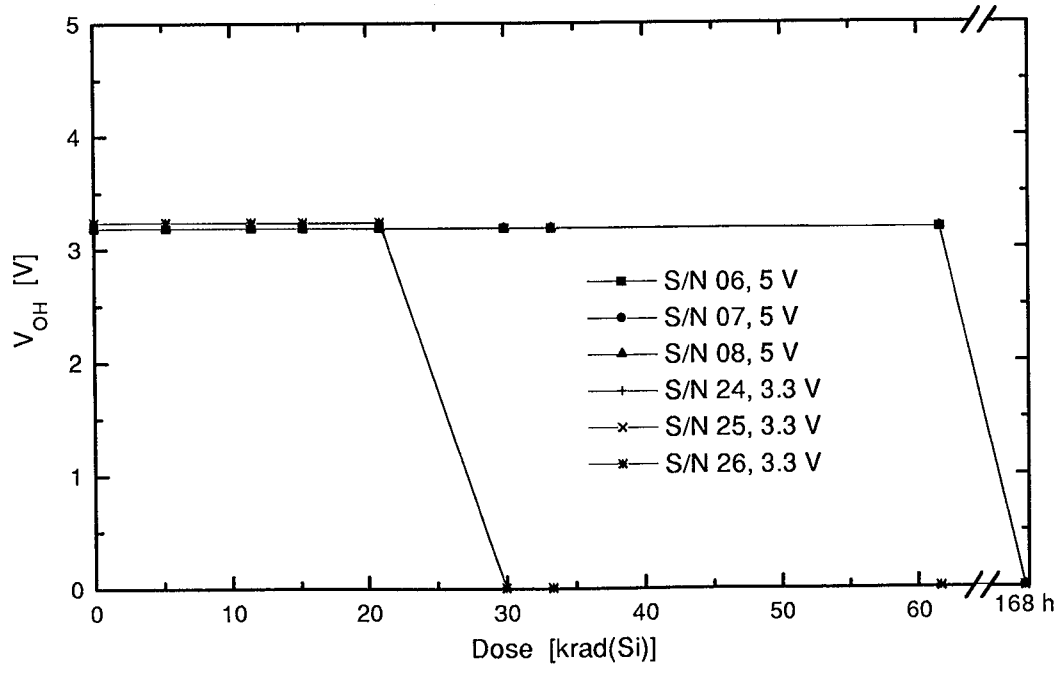

Fig. 8. Output voltage high level versus dose and after annealing for AMD Flash devices.

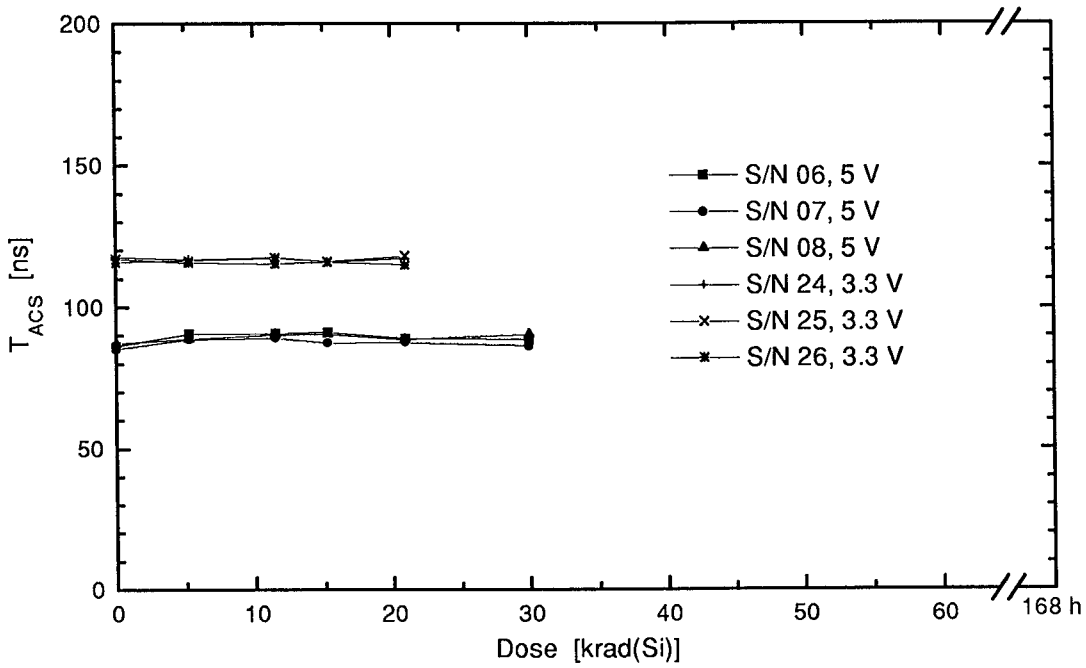

Fig. 9. Chip select access time versus dose and after annealing for AMD Flash devices.