| MATRA MARCONI SPACE | VTT AUTOMATION | Ref :AUT/PRO/938/97<br>Issue :01 Rev. :<br>Date :20/10/97<br>Page :i |
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# EUROPEAN SPACE AGENCY CONTRACT REPORT

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Title

# TC551001BFL-70L, 1 MBIT SRAM FROM TOSHIBA

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## TOTAL IONISING DOSE CHARACTERIZATION TEST REPORT

**ESA/ESTEC Contract No. 11755/95/NL/NB-WO1/CO1**

| | Name and Function | Date | Signature |
|---|---|---|---|
| **Prepared by :** | SALMINEN A.<br>Project manager | 20/10/97 | A. Salmin |
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| **Approved by :** | POIVEY Christian | 28/11/97 | |
| **Authorized by :** | HARBOE SØRENSEN R.<br>ESTEC Technical Officer | | |
| **Application authorized by :** | | | |

| Document type | Nb WBS | Summary: Low voltage memories were tested under total ionising dose irradiation to study the effect of supply voltage on the radiation sensitivity. This report presents the results obtained on 1 Mbit Toshiba SRAMs. |
|---|---|---|

# SUMMARY OF RESULTS

## Test sample characteristics

| | | | |
|---|---|---|---|
| **Part Name :** | TC551001BFL-70L | **Function :** | 128K x 8 SRAM |
| **Technology :** | CMOS, 0.5 µm | **Package :** | 32 pin SOP |
| **Manufacturer :** | Toshiba | **Location :** | Germany |
| **Sample size :** | 3 (5 V), 3 (3.3 V) | **Date Code :** | 9624 |

## TID test results

### Functional test

The following table summarises the failure doses at the first error and at the 100th error:

| S/N | $V_{CC}$ V | Dose at 1st error krad(Si) | Error mode | Dose at 100 error krad(Si) | % of 0→1 |
|---|---|---|---|---|---|
| 00 | **5** | 36.6 | 1→0 | 56.1 | 60 |
| 01 | **5** | 28.2 | 0→1 | 45.4 | 34 |
| 02 | **5** | 33.9 | 1→0 | 55.1 | 31 |
| 18 | **3.3** | 39.3 | 1→0 | 54.0 | 60 |
| 19 | **3.3** | 39.5 | 1→0 | 56.1 | 40 |
| 20 | **3.3** | 38.9 | 0→1 | 58.3 | 42 |

In four out of six devices the initial error mode was the transition 1→0. The transition 1→0 dominates in four out of six devices at 100 errors. All the errors detected were read errors. The error growth rate was nearly exponential as a function of dose. No devices recovered functionally in the high temperature annealing of 168 h at 85°C.

### Functional test conclusion

The results of these experiments demonstrate that on the average 1 Mbit SRAM TC551001BFL-70L (70ns) from Toshiba, when biased at 3.3 V, is less sensitive to ionising radiation than in the 5 V biasing mode in terms of functional performance.

## Parametric test

The following table summarises the average dose levels for both bias at which sensitive parameters have drifted **20%**:

| **Parameter** | **Dose Level** $V_{CC}$ **= 5 V** | **Dose Level** $V_{CC}$ **= 3.3 V** |
|---|---|---|
| Standby supply current | 35 krad(Si) | >60 krad(Si) |
| Operating supply current | 35 krad(Si) | >60 krad(Si) |

Both drifted parameters at 5 V recovered after annealing: compared to the preirradiated value, the standby supply current increased by a factor of 23 and the operating supply current increased by a factor of 2.

## Parametric test conclusion

The results of the parametric tests indicate that 1 Mbit SRAM TC551001BFL-70L (70ns) from Toshiba at 5 V is more sensitive to ionising radiation than at 3.3 V bias.

# DOCUMENT CHANGE LOG

| Issue/ Revision | Date | Modification Nb | Modified pages | Observations |
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| 1 | 20/10/97 | | | Original Edition |

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## 1. INTRODUCTION

The aim of this work is to investigate radiation effects in low voltage technologies. The study is focused on memory devices, which require lower voltage to achieve higher integration. Parts selected consists of SRAMs (1 Mbit, 2 types), DRAMs (16 Mbit, 2 types), and FLASH memories (8 Mbit, 2 types).

The object of this document is to describe the irradiations performed on the Toshiba 1 Mbit TC551001BFL-70L (70ns), in order to measure the influence of two different supply voltage levels on the total ionising dose sensitivity.

Irradiations were performed in March 1997 ($10^{th}$-$17^{th}$) according to the procedures referenced in the following paragraph.

This work was performed in the frame of the WO1/CO1 for ESTEC Contract n°11755/95/NL/NB.

## 2. REFERENCE DOCUMENTS

[1] ESA/SCC 22900-4 ESA Basic Specification for Total Dose Steady-State Irradiation

[2] Toshiba Manufacturer Data Sheet

[3] Description of the VTT memory tester, AUT/PRO/76/96 (in Finnish)

# 3. PART DETAILS

## 3.1. DEVICE IDENTIFICATION

### 3.1.1. References

| | | |
|---|---|---|
| Type | : | TC551001BFL-70L |
| Manufacturer | : | Toshiba |
| Place | : | Germany |
| Packaging | : | 32 pin SOP |

### 3.1.2. Function

128K x 8 SRAM (70 ns)

### 3.1.3. Technology

CMOS, 0.5 µm, 4T+2 resistors (See next page for further details)

### 3.1.4. Part Procurement

| | | |
|---|---|---|
| Origin | : | VTT Automation, Finland |
| Level | : | Standard Level |
| Temperature range | : | -25°C, +85°C (Industrial) |
| Date code | : | 9624 |
| Screening | : | / |
| Sample size | : | 3 (biased at 5 V), 3 (biased at 3.3 V) |
| Manufacturer Marking | : | TC551001BFL-70L Germany 9624TBK (Package) |
| Detailed specifications | : | Manufacturer Data sheet |

### 3.1.5. Previous TID details/history

No radiation data on this device

### 3.2. TECHNICAL INFORMATION

The 1 Mbit TC551001BFL-70L SRAM from Toshiba is a device with wide supply voltage range. The device can be operated at 3.3V or at 5V.

The functionality and the parametric integrity of the devices were examined prior to irradiation. No screening nor burn-in were carried out during this study.

**General information**

| | |
|---|---|
| **Name** | Toshiba TC551001BFL-70L |
| **Package Marking** | Toshiba TC551001BFL-70L<br>Germany 9624TBK |
| **Access time/ns at 5V** | 70 |
| **Temperature range/°C** | -25, +85 |
| **Organisation** | 128K x 8 |
| **Supply Voltage/V** | 2.7-5.5 |

**Technology**

| | |
|---|---|
| **Name** | Toshiba TC551001BFL-70L |
| **CMOS** | yes |
| **Mask** | B |
| **Epitaxial layer** | * |
| **Design rules** | 0.5 µm |
| **Die size** | 5.07 mm x 8.69 mm |
| **Cell type** | 4T + 2 resistors |
| **Cell size** | 3.61 µm x 5.7 µm |

* The missing information was unsuccessfully required from the manufacturer.

# 4. TEST DESCRIPTION

## 4.1. IRRADIATION FACILITY

**Name** MMS Cobalt 60-source, model Shepherd 484

**Location** Matra Marconi Space France
37, avenue Louis Bréguet
78146 VELIZY-VILLACOUBLAY Cedex
France

**Activity** < 8.9 curies.

**Calibration** 10/03/97.

## 4.2. TID TEST SET-UP

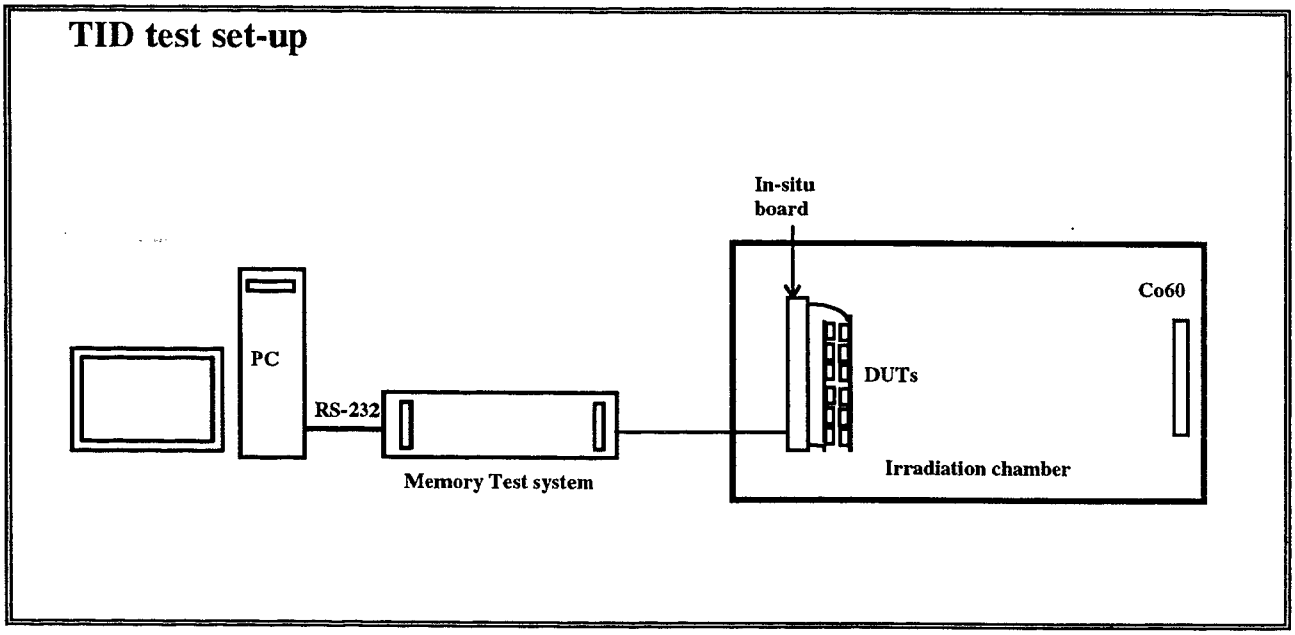


**Fig. 4.1. Description of the TID test set-up.**

The DUTs were soldered on small PCB's with pin headers. They were mounted on the two large PCB's that were biased at 5 V and 3.3 V. The distance between 5 V and 3.3 V devices were 2 mm from package to package. The difference in dose rates was taken into account when computing the doses received by the devices.

To be functionally tested in the irradiation exposure chamber, each DUT was selected by a chip select logic in the In-situ board. The supply voltage was provided by the memory tester. A complete description of the memory tester is given in [3].

The test flow chart is given in fig. 4.2.

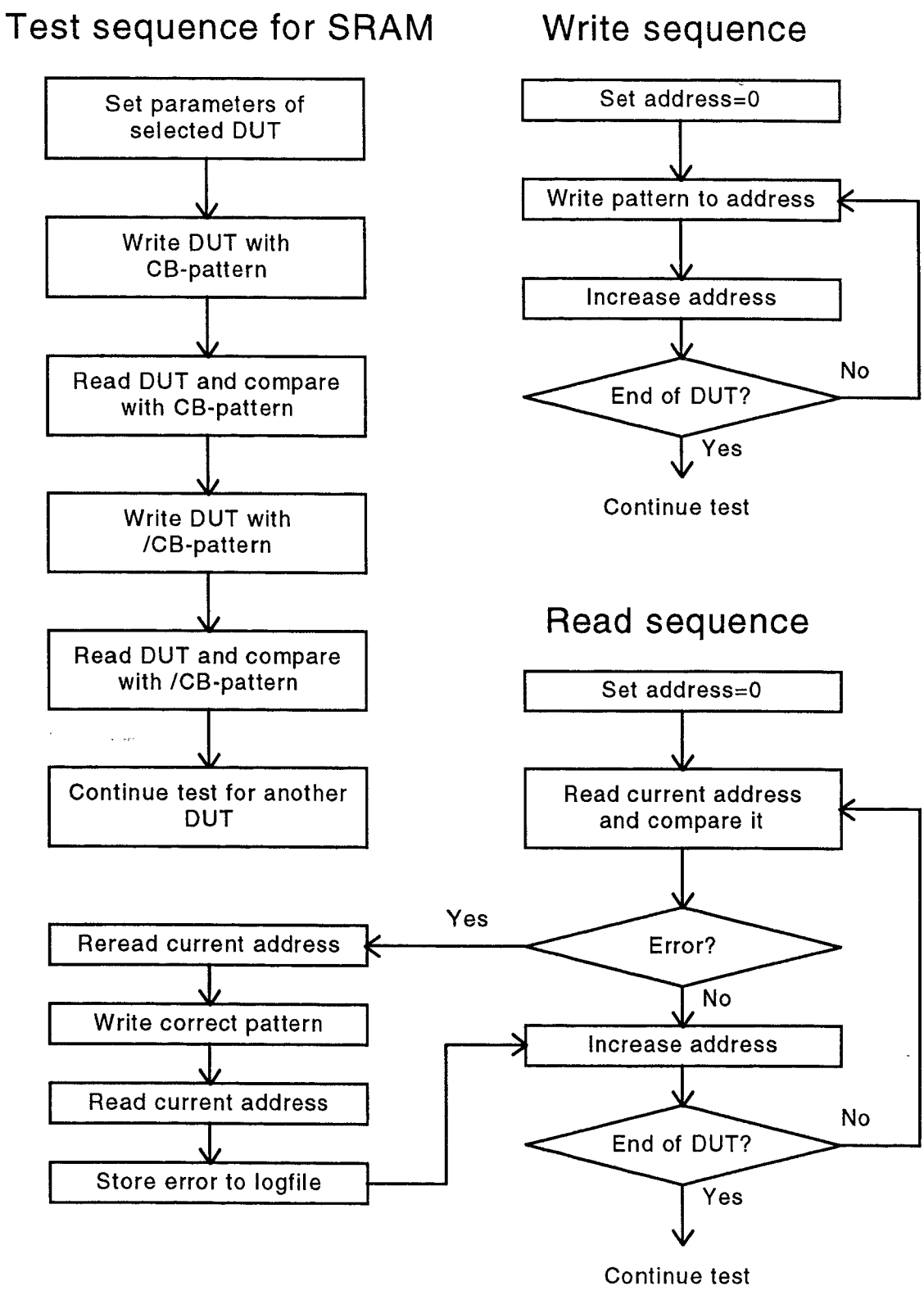


**Fig. 4.2. The test flow chart of an individual device with write and read sequencies.**

The write and read cycles during functional test were as follows:

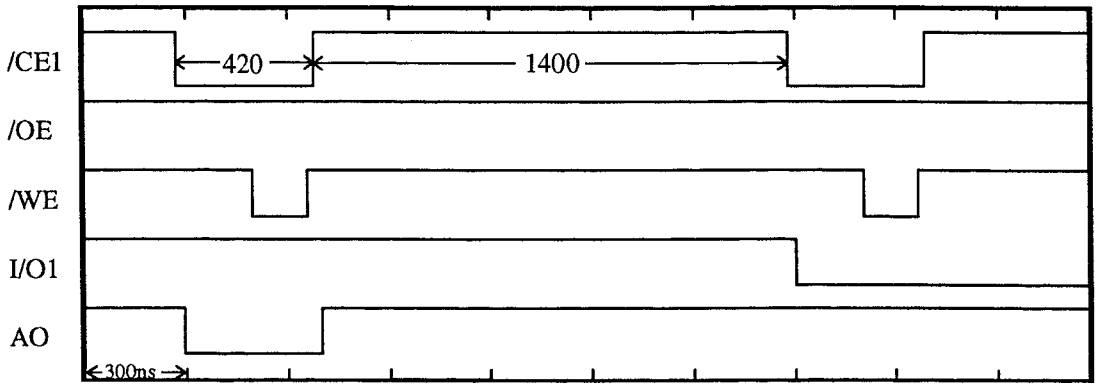


**Fig. 4.3. Write Cycle of Toshiba SRAM during functional test.**

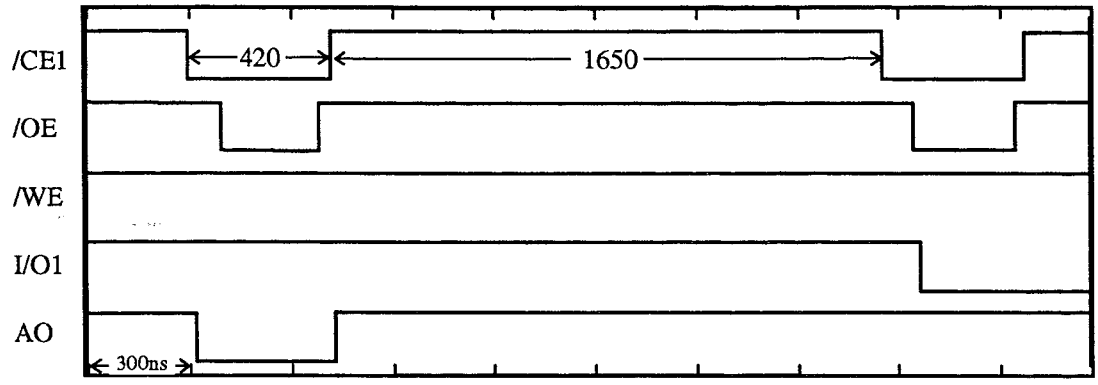


**Fig. 4.4. Read Cycle of Toshiba SRAM during functional test.**

# 5. TOTAL IONISING DOSE EXPERIMENTAL RESULTS

## 5.1. TID IRRADIATION TEST SEQUENCE

During irradiations all the devices were functionally tested 3 times per hour automatically in the exposure chamber, and the results were stored on a hard disk of the measuring computer. The memory test started with write of a CB (checkerboard) pattern to the memory device. The write time of a single pattern was approx. 0.24 s. Thereafter the memory contents of the device was read and it was compared to the original pattern. After this the memory was tested with a complementary CB pattern in an identical way. During the irradiation, the memory contents was the complementary CB pattern. Therefore, this represents the worst case testing.

If errors were encountered, the corrupted data was immediately reread and rewritten with the original pattern. The write operation was verified with another read. In this way peripheral circuitry errors, memory cell errors, write errors and stuck bits can be indicated. Due to the limitation of the measuring computer, the maximum number of recorded corrupted bytes was set to 100. TTL levels were applied in control, address and data signals. 5 V bias was applied to devices s/n 00-02 and 3.3 V bias was applied to devices s/n 18-20. Before the seventh irradiation step the time between write and read of both patterns was increased to 4 s to enhance the detection of corrupted memory location.

In the time between the irradiations, the parameters were measured remotely at the end of each step within two hours with the VTT parametric tester in another room. Except the measurement, the devices were unbiased during this time. The resolution of the voltage measurements were better than 1 mV.

The irradiation was accomplished in seven steps. The average dose rates were 420 rad(Si)/h and 410 rad(Si)/h for 5 V and 3.3 V devices, correspondingly. The dose rates and cumulative doses with durations of each irradiation step are given in table 5.1.

**Table 5.1. Dose rates, durations and cumulative doses for 5 V and 3.3 V Toshiba SRAMs.**

| Step | Dose rate 5 V rad(Si)/h | Dose rate 3.3 V rad(Si)/h | Duration h | Total Dose 5 V krad(Si) | Total Dose 3.3 V krad(Si) |
|---|---|---|---|---|---|
| 1 | 262.0 | 258.1 | 20.00 | 5.2 | 5.1 |
| 2 | 327.5 | 317.3 | 19.00 | 11.5 | 11.2 |
| 3 | 471.6 | 458.1 | 8.00 | 15.3 | 14.8 |
| 4 | 471.6 | 458.1 | 12.00 | 20.9 | 20.4 |
| 5 | 471.6 | 458.1 | 19.17 | 29.9 | 29.1 |
| 6 | 471.6 | 458.1 | 7.18 | 33.3 | 32.4 |
| 7 | 471.6 | 458.1 | 60.00 | 61.6 | 59.9 |

After the last irradiation step and parametric measurement, the devices were put into a heat chamber for an annealing period of 168 h at 85°C. The devices were functionally tested 3 times per hour. The test set-up for the Sony SRAMs was the same one as during irradiation.

### 5.1.1. Problems encountered/Discussion

No specific problem was encountered during irradiations.

## 5.2. TID TEST RESULTS

**Functional test**

The table 5.2 summarises the failure doses in the functional test:

**Table 5.2. Failure doses at first and 100th errors with error modes.**

| S/N | $V_{CC}$ V | Dose at 1st error krad(Si) | Error mode | Dose at 100 error krad(Si) | % of 0→1 | Annealing | Remarks |
|---|---|---|---|---|---|---|---|
| 00 | 5 | 36.6 | 1→0 | 56.1 | 60 | No functional recovery | Read errors |
| 01 | 5 | 28.2 | 0→1 | 45.4 | 34 | No functional recovery | Read errors |
| 02 | 5 | 33.9 | 1→0 | 55.1 | 31 | No functional recovery | Read errors |
| Average | | 32.9 | | 52.2 | 42 | | |
| 18 | 3.3 | 39.3 | 1→0 | 54.0 | 60 | No functional recovery | Read errors |
| 19 | 3.3 | 39.5 | 1→0 | 56.1 | 40 | No functional recovery | Read errors |
| 20 | 3.3 | 38.9 | 0→1 | 58.3 | 42 | No functional recovery | Read errors |
| Average | | 39.3 | | 56.1 | 47 | | |

The results of these experiments demonstrate that on the average 1 Mbit SRAM TC551001BFL-70L (70ns) from Toshiba, when biased at 3.3V, is less sensitive to ionising radiation than in the 5 V biasing mode in terms of the first error and 100 errors detected. The failure dose of devices biased at 3.3 V is 6.4 krad(Si) larger than devices biased at 5 V. The failure dose at 100 errors is 3.9 krad(Si) higher for devices biased at 3.3 V.

In four out of six devices the error mode was the transition 1→0 at the first errors.At 100 errors, the error mode was the transition 1→0 in four out of six devices. All the errors were read errors and up to the highest doses there were no write errors in any device. The error growth rate was nearly exponential as a function of dose. No devices recovered functionally in the high temperature annealing of 168 h at 85°C.

Detailed functional test results are given in appendices 1 and 2.

**Functional test conclusion**

The results of these experiments demonstrate that on the average 1 Mbit SRAM TC551001BFL-70L (70ns) from Toshiba, when biased at 3.3V, is less sensitive to ionising radiation than in the 5 V biasing mode.

**Parametric test**

The table 5.3 summarises the average dose levels at which parameters have drifted 20% and the average relative recovered values after 168 h at 85°C annealing for both bias. The average relative recovery indicates the recovered value after annealing divided by the preirradiated value.

**Table 5.3. Average dose levels at 20% drift and relative recovery after annealing.**

| Symbol | Parameter | Dose Level/krad(Si) | | Parametric recovery | |
|---|---|---|---|---|---|
| | | $V_{CC}$ = 5 V | $V_{CC}$ = 3.3 V | $V_{CC}$ = 5 V | $V_{CC}$ = 3.3 V |
| $I_{CCSB}$ | Standby Supply Current | 35 | >60 | 23 | 0.9 |
| $I_{CCOP}$ | Operating Supply Current | 35 | >60 | 2.0 | 1.1 |
| $I_{IL}$ | Input Current Low Level | >60 | >60 | 0.9 | 0.9 |
| $I_{IH}$ | Input Current High Level | >60 | >60 | 1.2 | 1.0 |
| $I_{OZL}$ | Output Leakage Current High Impedance Low level Applied | >60 | >60 | 0.9 | 0.9 |
| $I_{OZH}$ | Output Leakage Current High Impedance High Level Applied | >60 | >60 | 1.0 | 1.0 |
| $V_{OL}$ | Output Voltage Low Level | >60 | >60 | 1.0 | 1.0 |
| $V_{OH}$ | Output Voltage High Level | >60 | >60 | 1.0 | 1.0 |
| $T_{AOE}$ | Output Enable Access Time | >60 | >60 | 1.0 | 1.0 |
| $T_{ACS}$ | Chip Select Access Time | >60 | >60 | 1.0 | 1.0 |

Up to 30 krad(Si) all the parameters were very stable. At 60 krad(Si) dose, most parameters were insensitive to total dose. Only $I_{CCSB}$ and $I_{CCOP}$ of 5 V devices show strong sensitivity to dose. Devices biased at 3.3 V are very insensitive to dose. After annealing, all the sensitive parameters recovered closer to the preirradiated value. Parametric test result are given as graphs in appendix 3.

**Parametric test conclusion**

The results of the parametric tests indicate that 1 Mbit SRAM TC551001BFL-70L (70ns) from Toshiba, when biased at 5 V, is more sensitive to ionising radiation than in the 3.3 V biasing mode in

terms of the parametric sensitivity. Except $I_{CCSB}$ and $I_{CCOP}$ of the 5 V devices, the parameters are almost insensitive to total dose.

## 6. CONCLUSION

Ionising dose tests were performed on the 1 Mbit SRAM TC551001BFL-70L from Toshiba, with 3.3 V and 5 V bias. The dose tolerance of the tested devices is good.

The effect of supply voltage tends to modify the TID tolerance of the devices: the sensitivity to ionising radiation is lower at 3.3 V bias than at 5 V bias in terms of functional performance and parametric stability.

## APPENDIX 1. Functional test results for 5 V Toshiba SRAM devices.

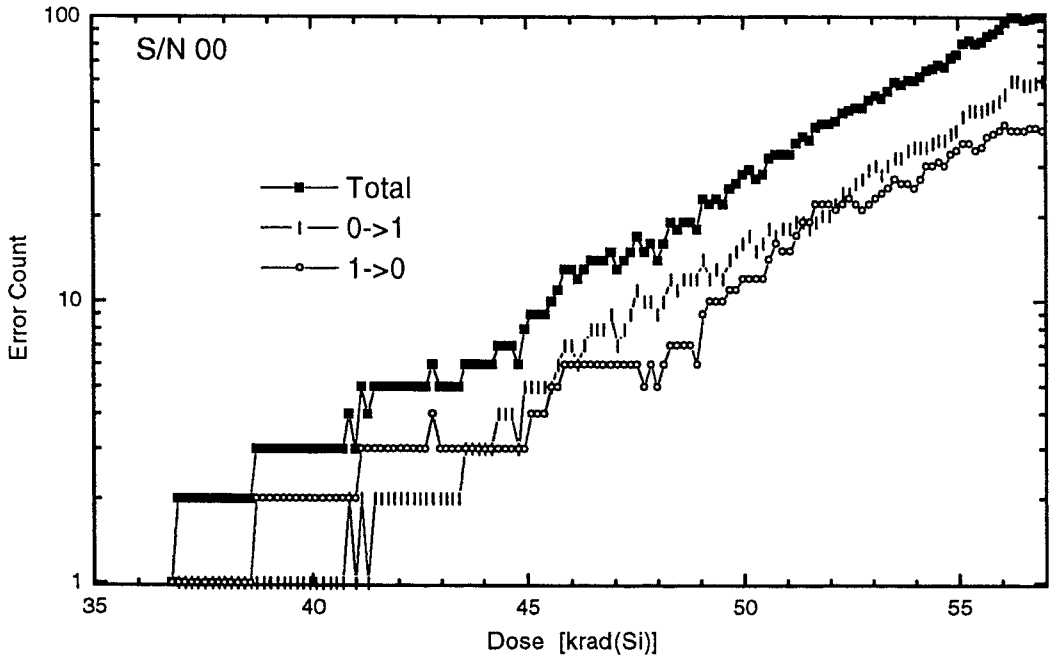


Fig. 1. Error count with modes 0→1 and 1→0 versus dose in 5 V Toshiba SRAM s/n 00.

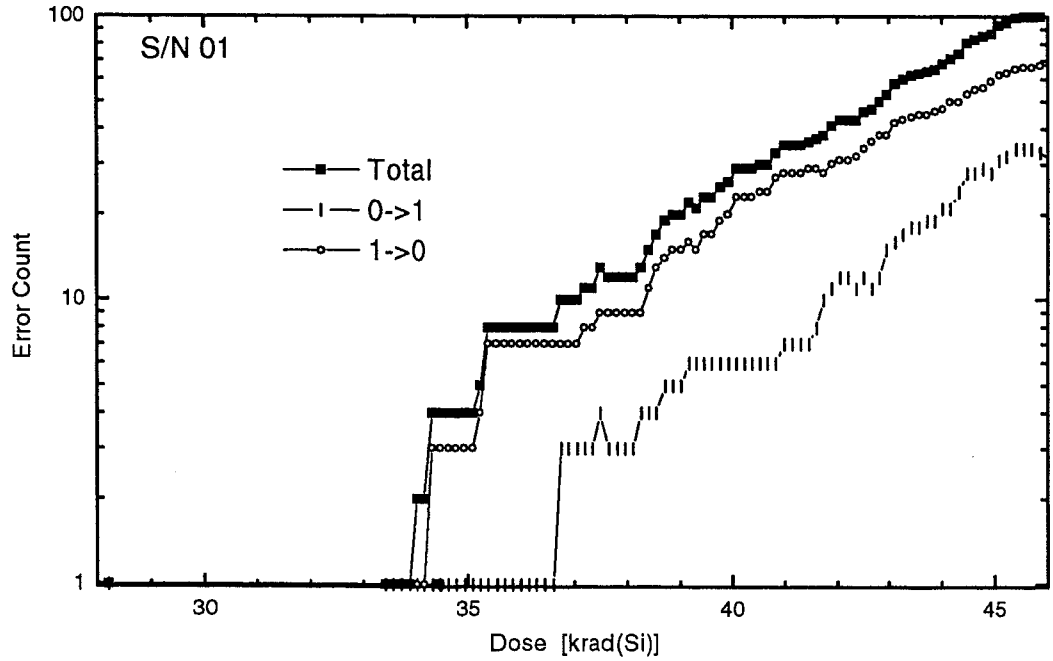


Fig. 2. Error count with modes 0→1 and 1→0 versus dose in 5 V Toshiba SRAM s/n 01.

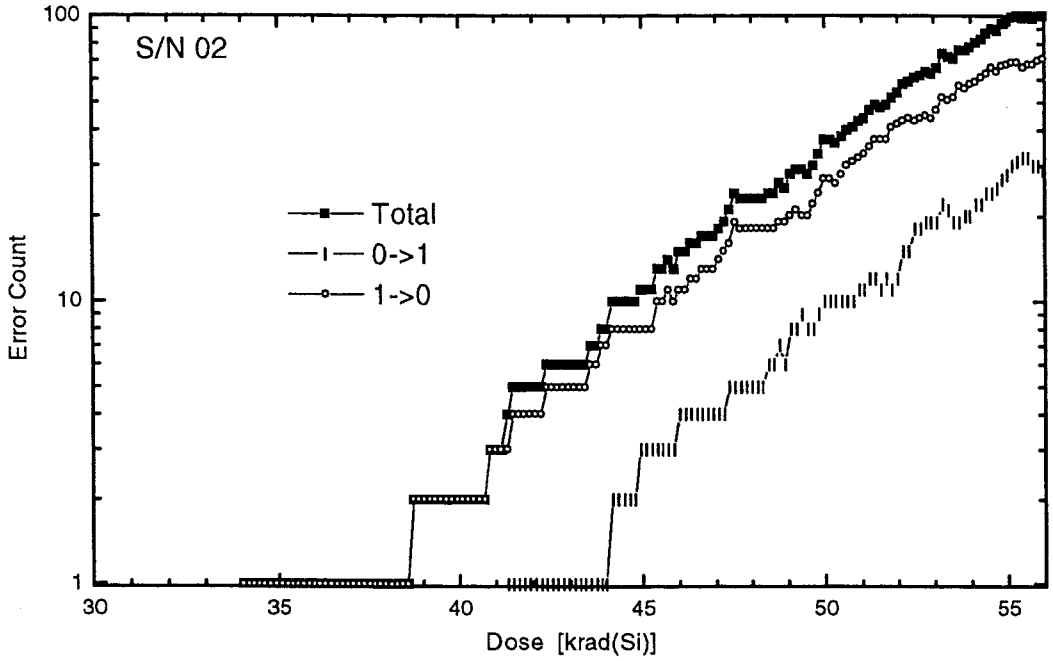


Fig. 3. Error count with modes 0→1 and 1→0 versus dose in 5 V Toshiba SRAM s/n 02.

## APPENDIX 2. Functional test results for 3.3 V Toshiba SRAM devices.

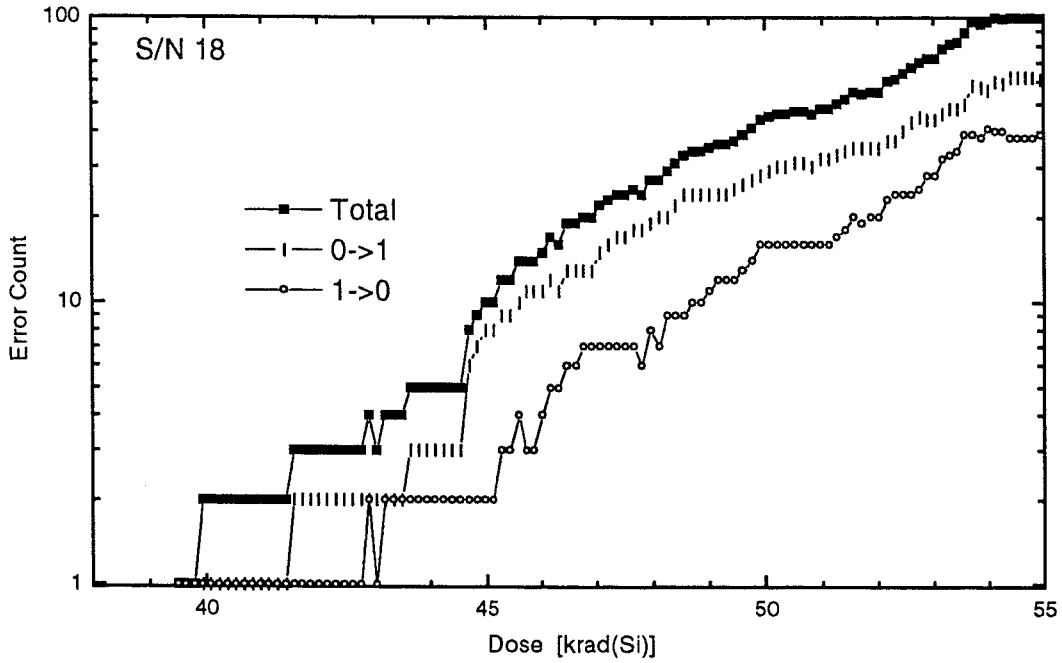


Fig. 1. Error count with modes 0→1 and 1→0 versus dose in 3.3 V Toshiba SRAM s/n 18.

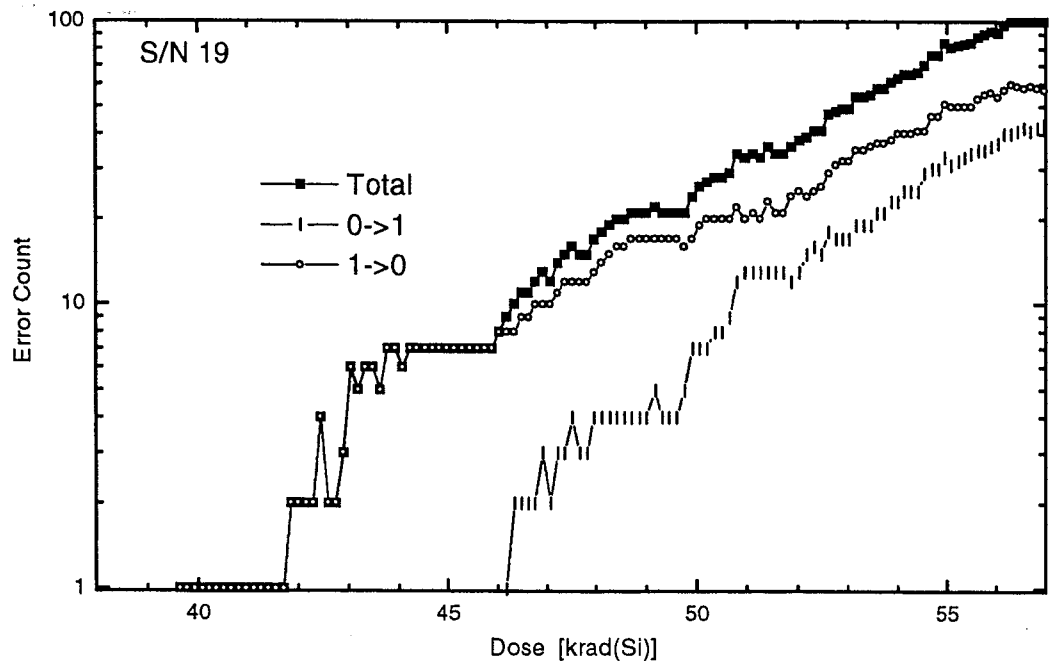


Fig. 2. Error count with modes 0→1 and 1→0 versus dose in 3.3 V Toshiba SRAM s/n 19.

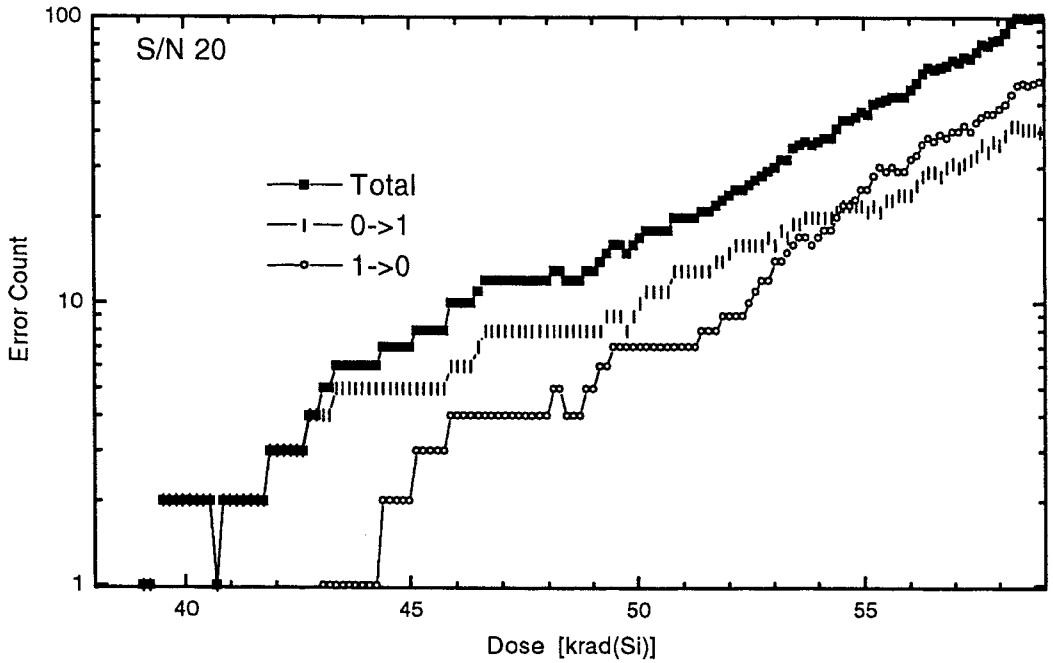


Fig. 3. Error count with modes 0→1 and 1→0 versus dose in 3.3 V Toshiba SRAM s/n 20.

## APPENDIX 3. Parametric test results for 5 V and 3.3 V Toshiba SRAM devices.

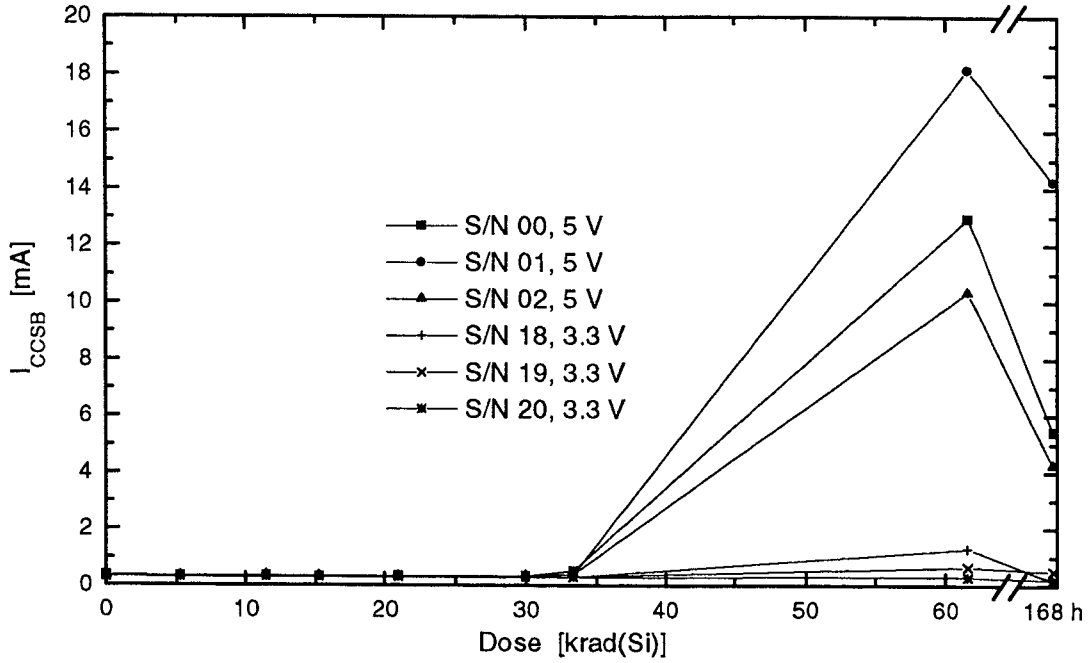


Fig. 1. Standby supply current versus dose and after annealing for Toshiba SRAM devices.

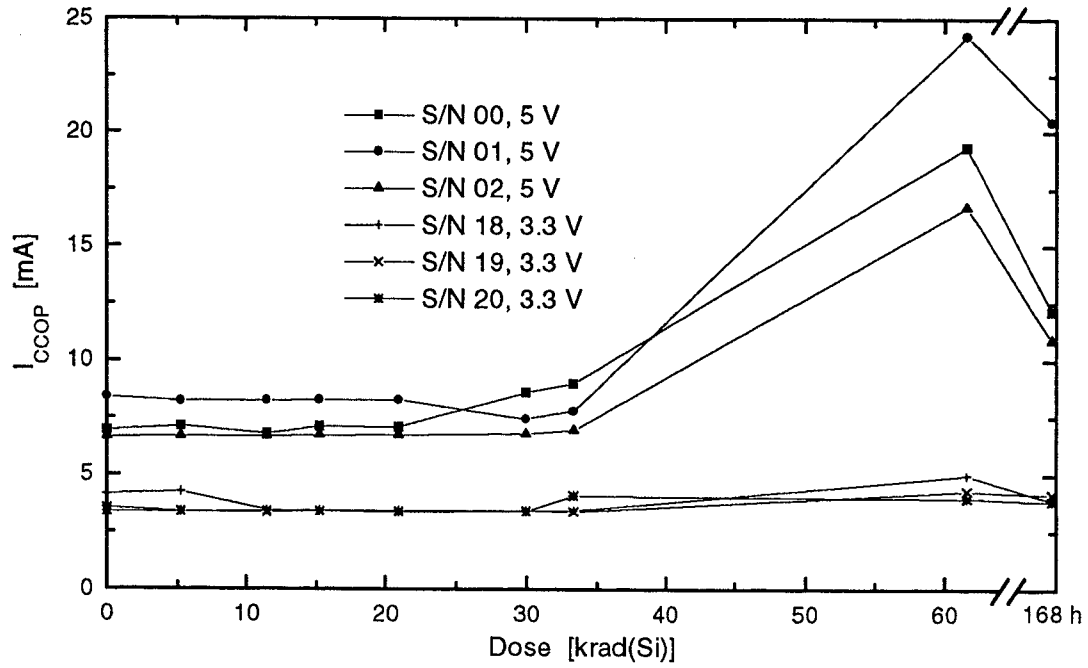


Fig. 2. Operating supply current versus dose and after annealing for Toshiba SRAM devices.

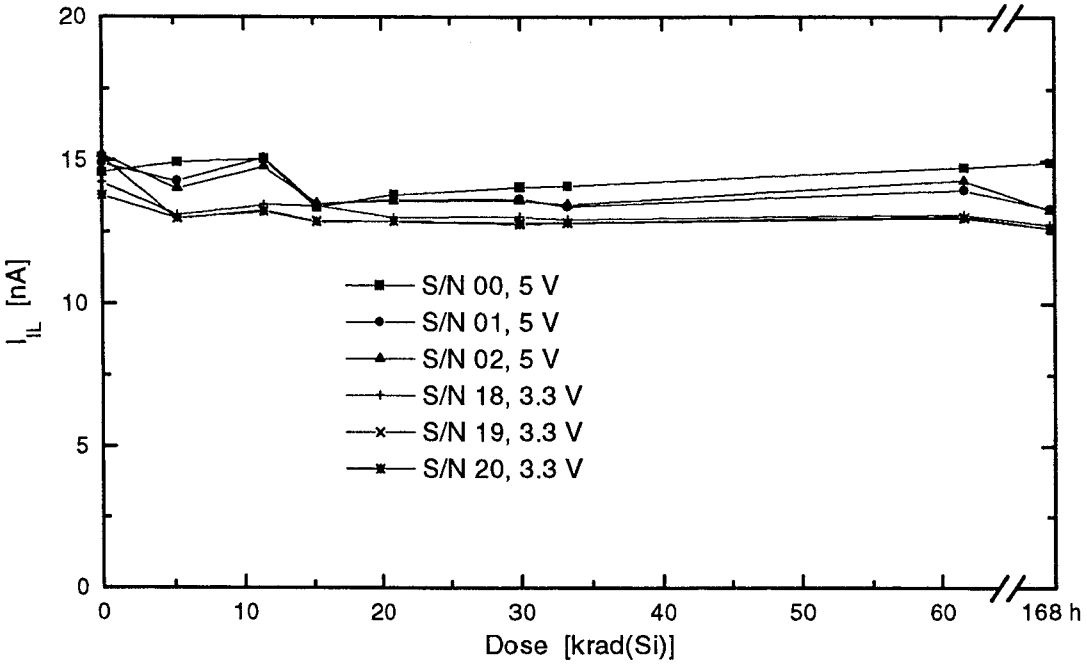


Fig. 3. Input current low level versus dose and after annealing for Toshiba SRAM devices.

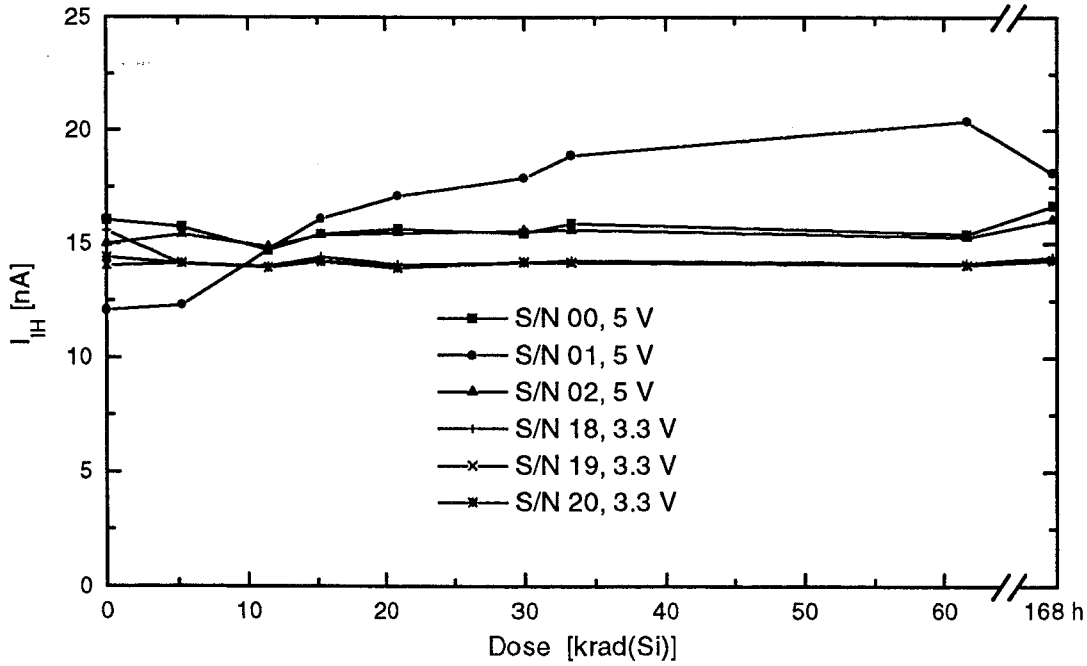


Fig. 4. Input current high level versus dose and after annealing for Toshiba SRAM devices.

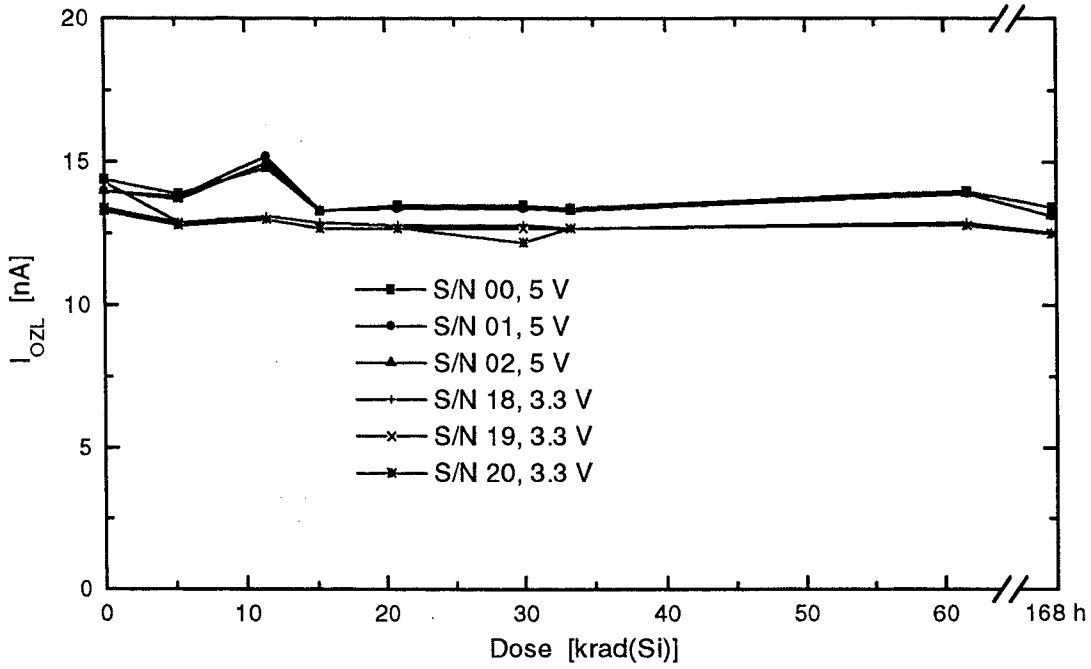


Fig. 5. Output leakage current high impedance low level applied versus dose and after annealing for Toshiba SRAM devices.

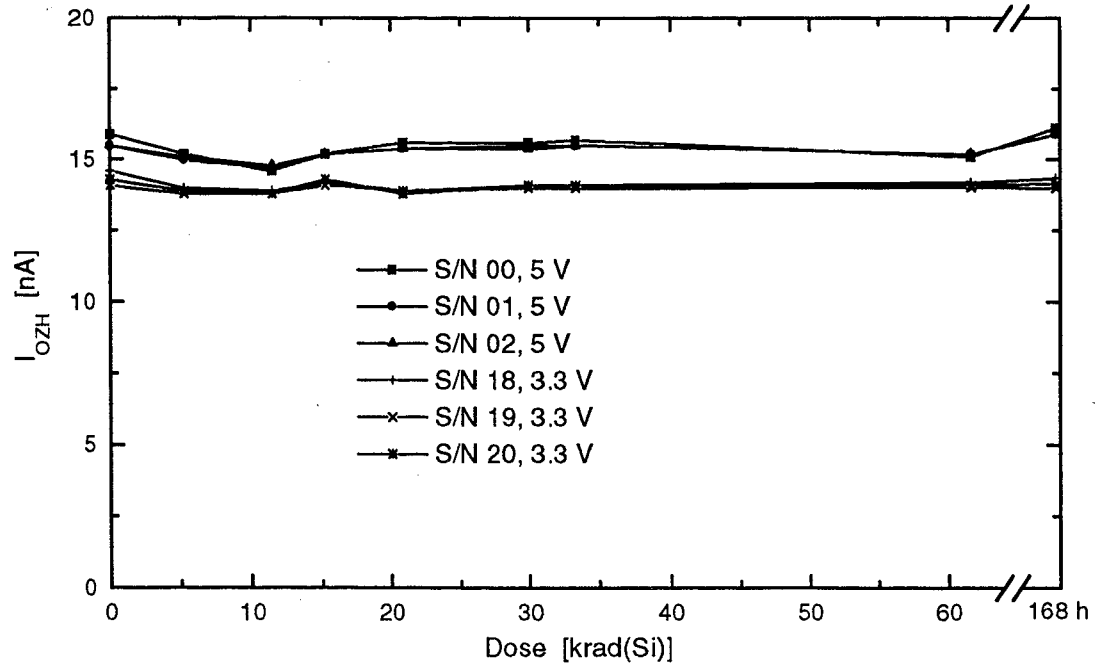


Fig. 6. Output leakage current high impedance high level applied versus dose and after annealing for Toshiba SRAM devices.

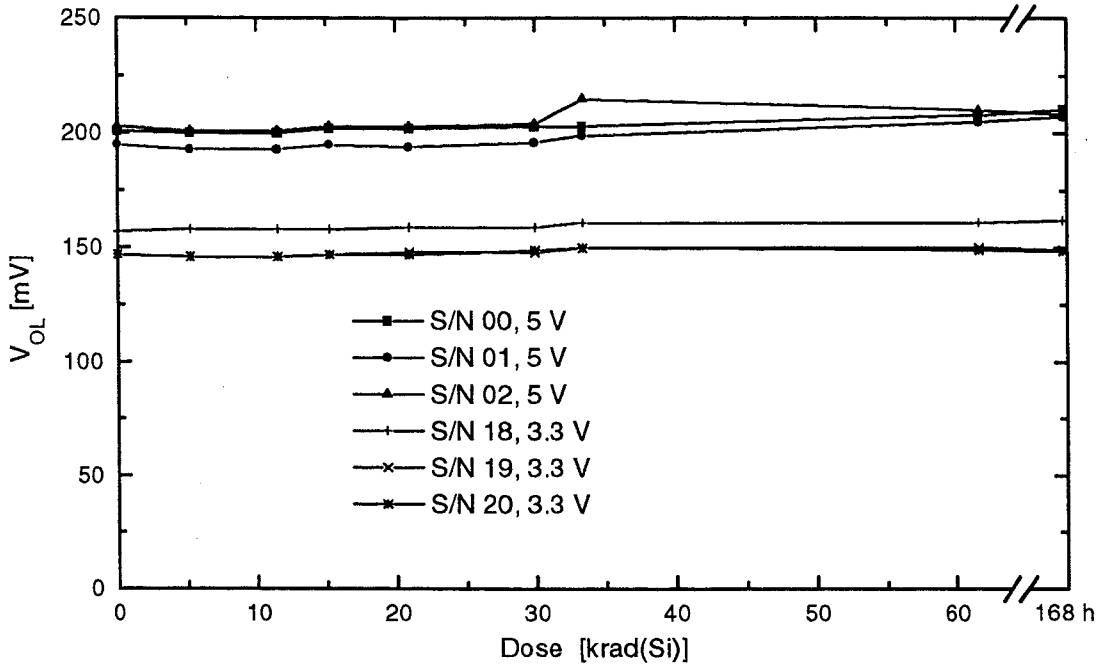


Fig. 7. Output voltage low level versus dose and after annealing for Toshiba SRAM devices.

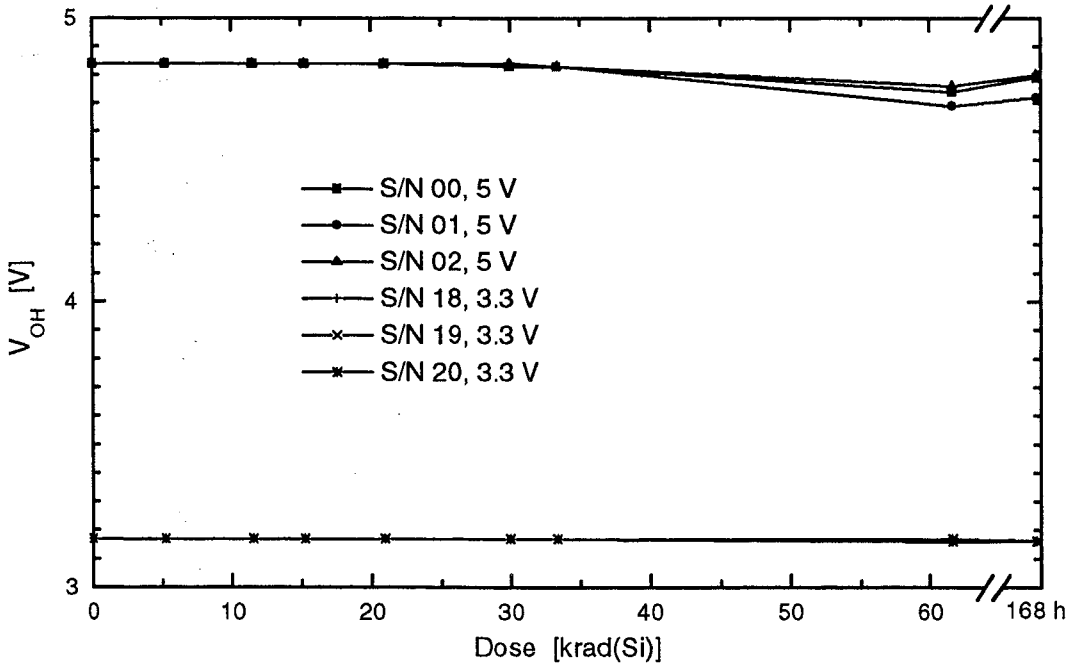


Fig. 8. Output voltage high level versus dose and after annealing for Toshiba SRAM devices.

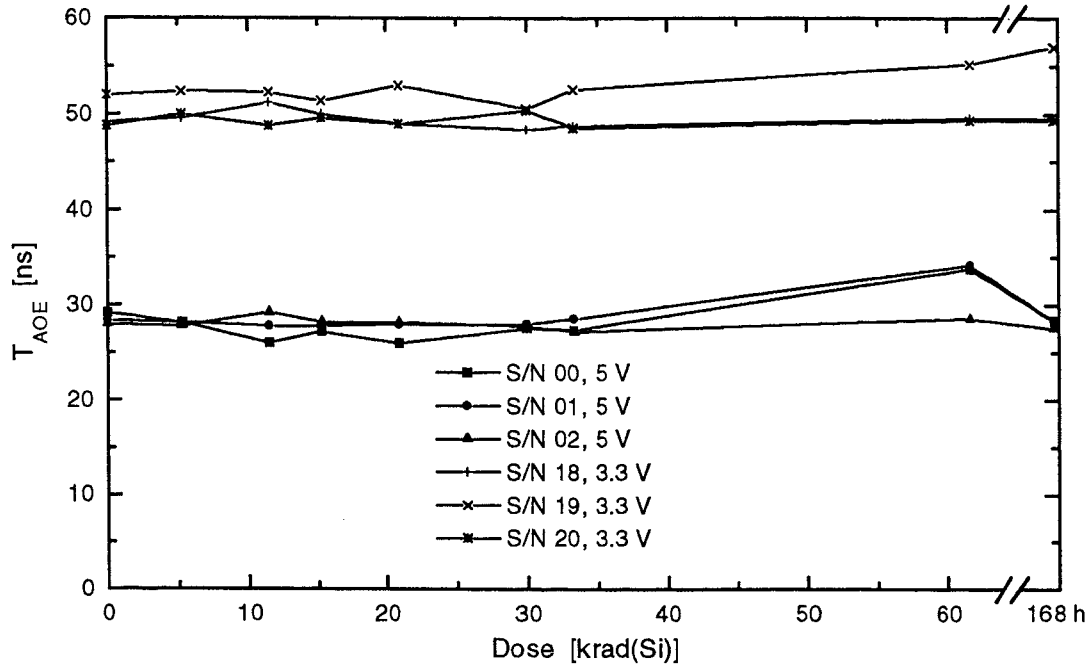


Fig. 9. Output enable access time versus dose and after annealing for Toshiba SRAM devices.

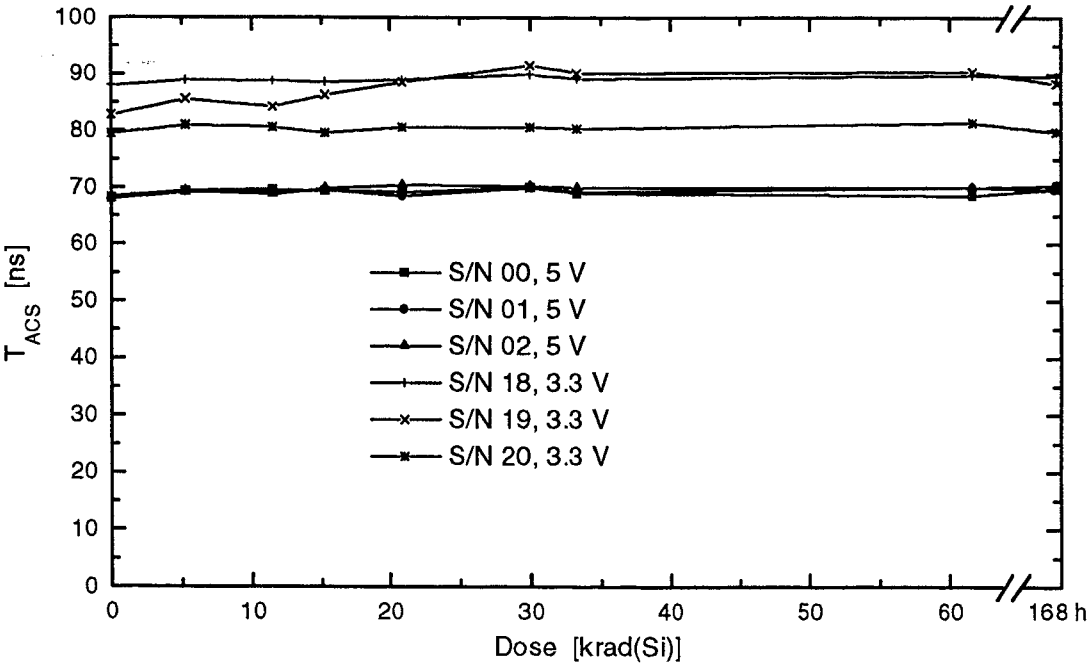


Fig. 10. Chip select access time versus dose and after annealing for Toshiba SRAM devices.