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EUROPEAN SPACE AGENCY
CONTRACT REPORT

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Title

LUNA ES/3, 16 MBIT DRAM FROM IBM

TOTAL IONISING DOSE CHARACTERIZATION TEST REPORT

ESA/ESTEC Contract No. 11755/95/NL/NB-WO1/CO1

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Document type	Nb WBS	Summary : Low voltage memories were tested under total ionising dose irradiation to study the effect of supply voltage on the radiation sensitivity. This report presents the results obtained on 16 Mbit IBM DRAMs.

SUMMARY OF RESULTS

Test sample characteristics :

Part Name :	Luna ES/3	**Function :**	4 M x 4 DRAM
Technology :	CMOS	**Package :**	MMS package
Manufacturer :	IBM	**Location :**	USA
Sample size :	3 (5 V), 3 (3.3 V)	**Date Code :**	-

TID test results

Functional test

5 V bias: device s/n 13 failed at 60.5 krad(Si). No other failures up to the maximum dose 63.4 krad(Si).

3.3 V bias: no failures up to the maximum dose 58.6 krad(Si).

After a non-biased period of 30 min, all the devices failed functionally in the CB-test that was performed prior to the parametric measurements.

Additional functional results:

The functional failure of s/n 13 was a multiple one: both 05 and 0A have changed permanently to 00.

One 5 V and one 3.3 V device recovered in the high temperature annealing of 168 h at 85°C in terms of CB-test.

Functional test conclusion

The dose sensitivity of the 5 V and 3.3 V device is similar. The comparison of 5 V and 3.3 V devices is difficult because the failure dose of the device biased at 5 V is larger than the maximum dose of devices biased at 3.3 V and because the doses received are different. Irradiation to a higher dose is needed to indicate the difference in bias sensitivity.

Parametric test

The following table summarises the average dose levels for both bias at which sensitive parameters have drifted **20%** and the average relative recovery after annealing:

Symbol	Parameter	Dose Level/krad(Si)		Relative Recovery	
		V_{CC} = 5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	V_{CC} = 3.3 V
I_{CCSB}	Standby Supply Current	15	25	350	28
I_{CCOP}	Operating Supply Current	25	30	90	30
I_{IL}	Input Current Low Level	40	50	1.1	1.1
I_{IH}	Input Current High Level	40	>60	1.0	1.0
I_{OZL}	Output Leakage Current High Impedance Low level Applied	10	10	0.9	0.9
I_{OZH}	Output Leakage Current High Impedance High Level Applied	10	15	340	100
V_{OL}	Output Voltage Low Level	10	15	20	20
V_{OH}	Output Voltage High Level	>60	>60	1.0	1.0
T_{AOE}	Output Enable Access Time	35	40	-	-
T_{ACS}	CAS Access Time	35	35	-	-

Parametric test conclusion

Parametric data show that the effect of supply voltage tends to modify the TID sensitivity of the devices: the sensitivity is lower at 3.3 V than at 5 V in terms parametric drifts. The parametric recovery after annealing is more efficient in 3.3 V devices than in 5 V devices.

DOCUMENT CHANGE LOG

Issue/ Revision	Date	Modification Nb	Modified pages	Observations
1	20/10/97			Original Edition

PAGE ISSUE RECORD

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TABLE OF CONTENTS

1. INTRODUCTION

The aim of this work is to investigate radiation effects in low voltage technologies. The study is focused on memory devices, which require lower voltage to achieve higher integration. Parts selected consists of SRAMs (1 Mbit, 2 types), DRAMs (16 Mbit, 2 types), and FLASH memories (8 Mbit, 2 types).

The object of this document is to describe the irradiation performed on the IBM 16 Mbit Luna ES/3, in order to measure the influence of two different supply voltage levels on the total ionising dose sensitivity.

Irradiations were performed in March 1997 (10^{th}-17^{th}) according to the procedures referenced in the following paragraph.

This work was performed in the frame of the WO1/CO1 for ESTEC Contract n°11755/95/NL/NB.

2. REFERENCE DOCUMENTS

[1] ESA/SCC 22900-4 ESA Basic Specification for Total Dose Steady-State Irradiation

[2] IBM Manufacturer Data Sheet

[3] Description of the VTT memory tester, AUT/PRO/76/96 (in Finnish)

[4] »Radiation Data Trends on High Integrated Memories for Estec Contract N°11755/95/NL/NB », B. Doucin

3. PART DETAILS

3.1. DEVICE IDENTIFICATION

3.1.1. References

Type	:	Luna ES/3
Manufacturer	:	IBM
Place	:	USA
Packaging	:	MMS package

3.1.2. Function

4 M x 4 DRAM (70 ns)

3.1.3. Technology

CMOS (See next page for further details)

3.1.4. Part Procurement

Origin	:	VTT Automation, Finland
Level	:	Standard Level
Temperature range	:	-25°C, +85°C (Industrial)
Date code	:	-
Screening	:	/
Sample size	:	3 (biased at 5 V), 3 (biased at 3.3 V)
Manufacturer Marking	:	No marking
Detailed specifications	:	Manufacturer Data sheet

3.1.5. Previous TID details/history

No radiation data on this specific device. Other IBM LV 16 Mbit DRAM version (LunaC) exhibited a parametrical and functional tolerance higher than 28 kRad [4].

3.2. TECHNICAL INFORMATION

The 16 Mbit Luna ES/3 DRAM from IBM is a device with wide supply voltage range. The device can be operated at 3.3 V or at 5 V.

The functionality and the parametric integrity of the devices were examined prior to irradiation. No screening nor burn-in were carried out during this study.

General information

Name	IBM Luna ES/3
Package Marking	No
Access time/ns at 5 V	Not measured
Temperature range/°C	Not measured
Organisation	4 M x 4
Supply Voltage/V	3.0-5.5

Technology

Name	IBM Luna ES/3
CMOS	Advanced CMOS
Epitaxial layer	2.1 µm
Design rules	0.5 µm
Die size	6 mm x 14.6 mm
Cell size	1 µm x 2.4 µm

4. TEST DESCRIPTION

4.1. IRRADIATION FACILITY

Name MMS Cobalt 60-source, model Shepherd 484

Location Matra Marconi Space France
37, avenue Louis Bréguet
78146 VELIZY-VILLACOUBLAY Cedex
France

Activity < 8.9 curies.

Calibration 10/03/97.

4.2. TID TEST SET-UP

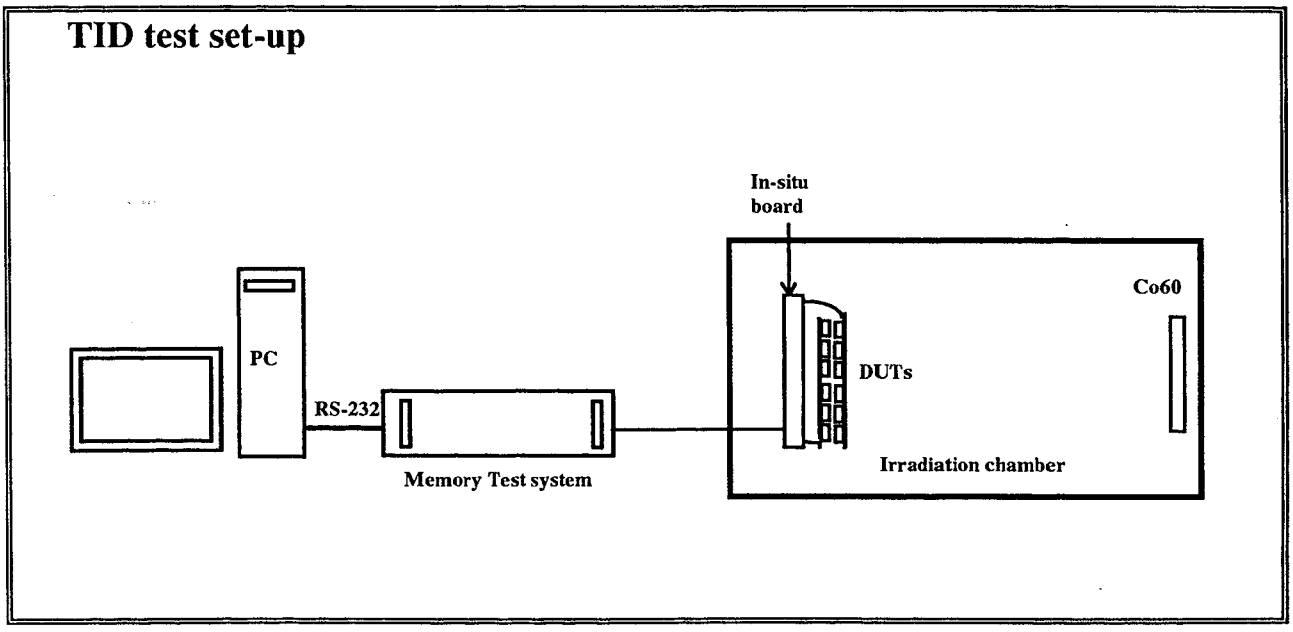

Fig. 4.1. Description of the TID test set-up.

The dies were tested in a MMS package that were mounted on two large PCBs that were biased at 5 V and 3.3 V. The distance between 5 V and 3.3 V devices was 6 mm. The difference in dose rates was taken into account when computing the doses.

The device under test was selected by a chip select logic located in the In-situ board. The supply voltage was provided by the memory tester. A complete description of the memory tester is given in [3].

The test sequence flow chart is given in fig. 4.2.

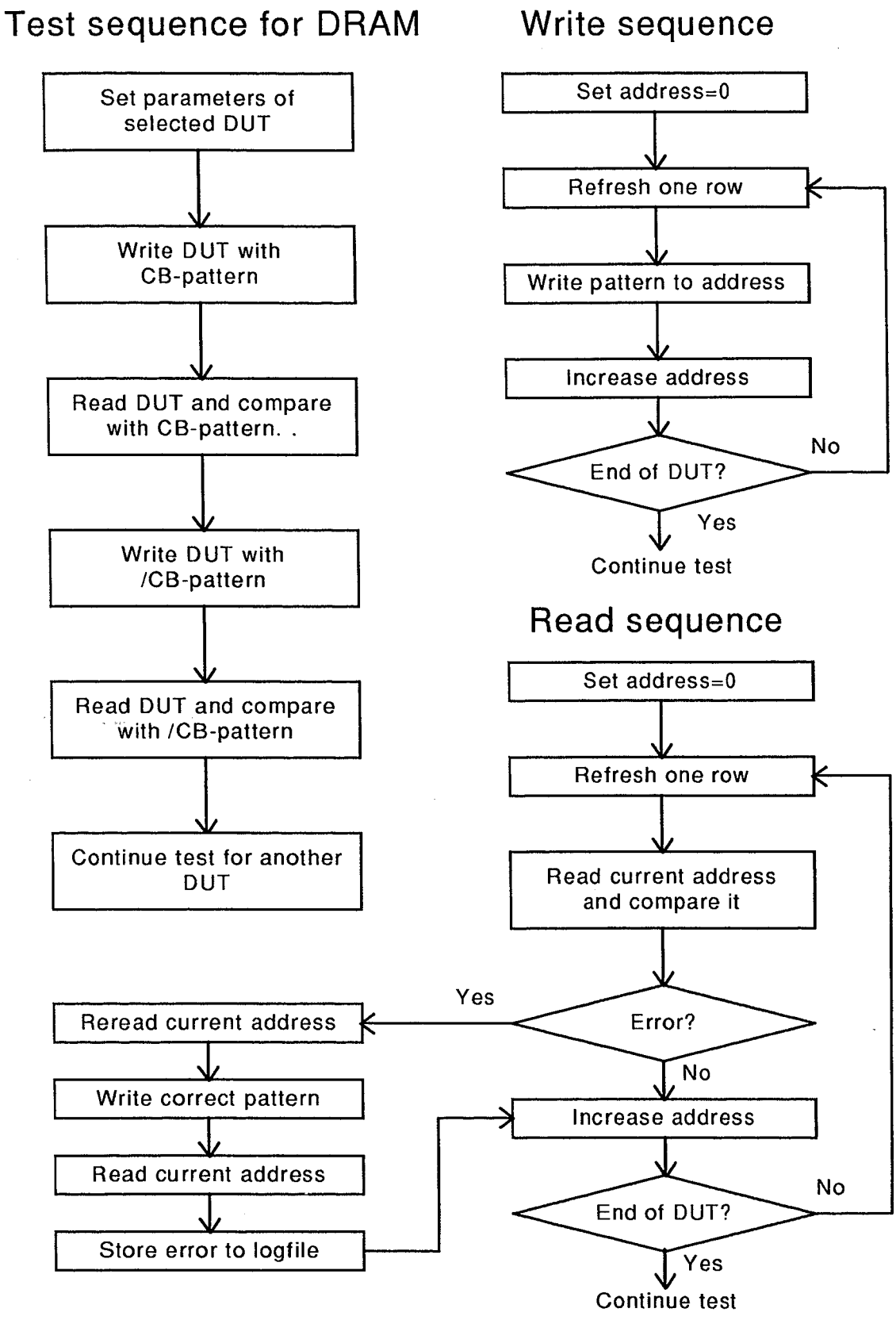

Fig. 4.2. The test flow chart of an individual device with write and read sequencies.

The write and read cycles during functional test were as follows:

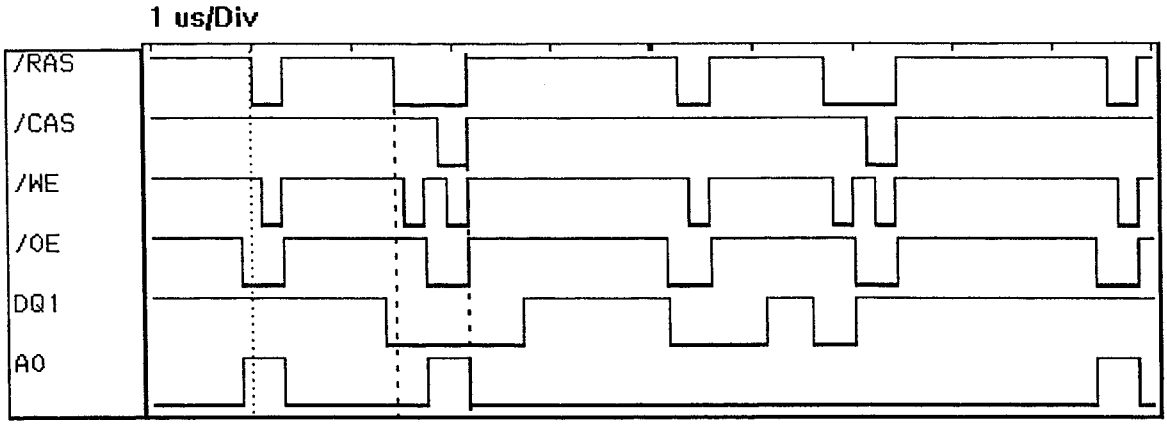

Fig. 4.3. Write Cycle of IBM DRAM during functional test.

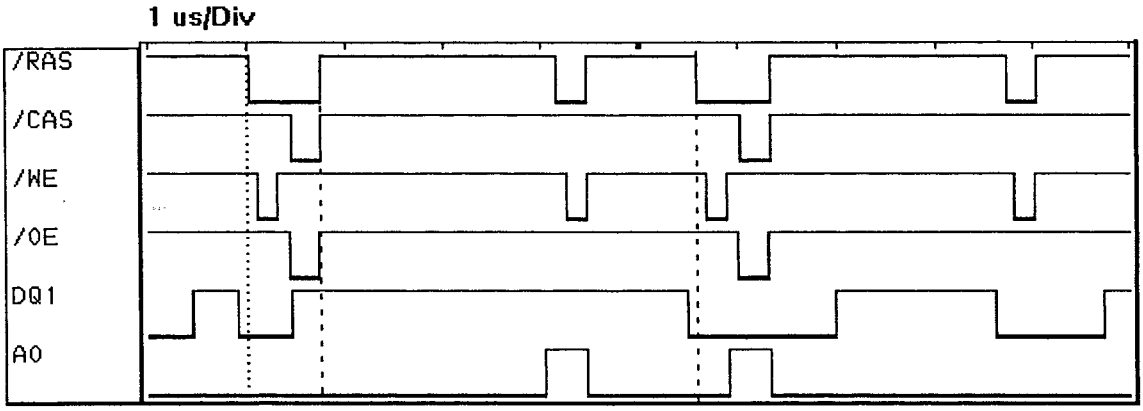

Fig. 4.4. Read Cycle of IBM DRAM during functional test.

5. TOTAL IONISING DOSE EXPERIMENTAL RESULTS

5.1. TID IRRADIATION TEST SEQUENCE

During irradiations all the devices were functionally tested 3 times per hour automatically in the exposure chamber, and the results were stored on a hard disk of the measuring computer. The memory test started with the write of a CB (checkerboard) pattern to the memory device. The write time of the device was approx. 19 s. Thereafter the memory contents of the device was read and it was compared to the original pattern. After this the memory was tested in an identical way with complementary CB pattern. During the irradiation, the memory contents was the complementary CB pattern. Therefore, this represents the worst case testing.

If errors were encountered, the corrupted memory location was immediately reread and rewritten with the original pattern. The write operation was verified with another read. In this way peripheral circuitry errors, memory cell errors, write errors and stuck bits were indicated. During the irradiation the normal DRAM refresh was active. Due to the limitation of the measuring computer, the maximum number of recorded corrupted bytes was set to 100. TTL levels were applied in control, address and data signals. 5 V bias was applied to devices s/n 12-14 and 3.3 V bias was applied to devices s/n 30-32.

In the time between the irradiations, the parameters were measured remotely at the end of each step within two hours with the VTT parametric tester in another room. Except the measurement, the devices were unbiased during this time. The resolution of the voltage measurements was better than 1 mV.

The irradiation was accomplished in seven steps. The average dose rates were 435 rad/h and 405 rad/h for 5 V and 3.3 V devices, correspondingly. The dose rates and cumulative doses with durations of each irradiation step are given in table 5.1.

Table 5.1. Dose rates, durations and cumulative doses for 5 V and 3.3 V IBM DRAMs.

Step	Dose rate 5 V rad(Si)/h	Dose rate 3.3 V rad(Si)/h	Duration h	Total Dose 5 V krad(Si)	Total Dose 3.3 V krad(Si)
1	267.4	251.8	20.00	5.3	5.0
2	333.6	311.2	19.00	11.7	10.9
3	485.1	446.8	8.00	15.6	14.5
4	485.1	446.8	12.00	21.4	19.9
5	485.1	446.8	19.17	30.7	28.5
6	485.1	446.8	7.18	34.2	31.7
7	485.1	446.8	60.00	63.4	58.6

After the last irradiation step and parametric measurement, the devices were put into a heat chamber for an annealing period of 168 h at 85°C. The devices were functionally tested 3 times per hour. The test set-up for the IBM DRAMs was the same one as during irradiation.

5.1.1. Problems encountered/Discussion

No specific problem was encountered during irradiations.

5.2. TID TEST RESULTS

Functional test

The table 5.2 summarises the failure doses in the functional test:

Table 5.2. Failure doses at first and 100th errors with error modes.

S/N	V_{cc} V	Dose at 1st error krad(Si)	Error mode	Dose at 100 errors krad(Si)	% of 0→1	Annealing	Remarks
12	5	>63.4	-	-	-	No functional recovery	Failed in param. test
13	5	60.5	1→0	60.5	100	No functional recovery	Mult. stuck bit error
14	5	>63.4	-	-	-	Functional after 164.1 h	Failed in param. test
30	3.3	>58.6	-	-	-	No functional recovery	Failed in param. test
31	3.3	>58.6	-	-	-	No functional recovery	Failed in param. test
32	3.3	>58.6	-	-	-	Functional after 8.5 h	Failed in param. test

Only one device s/n 13 biased at 5 V failed during the irradiation at 60.5 krad(Si). The failure was complete: the fist one hundred memory locations contained 00 instead of CB-pattern as shown in appendix 1. All the other devices were functional in terms of CB-test until the end of irradiation 63.4 krad(Si) for 5 V bias and 58.6 krad(Si) for 3.3 V bias. However, all devices failed in the parametric test after the last irradiation step.

In the annealing, the 3.3 V device s/n 32 recovered functionally in a 20 times shorter period than the 5 V device s/n 14.

Functional test conclusion

The dose sensitivity of the 5 V and 3.3 V device is similar. The exact comparison of 5 V and 3.3 V devices is difficult because the failure dose of the device biased at 5 V is larger than the maximum dose of devices biased at 3.3 V and because the doses received are different. Irradiation to a higher dose is needed to indicate the difference in bias sensitivity.

Parametric test

The table 5.3 summarises the average dose levels at which parameters have drifted 20% and the average relative recovered values after 168 h at 85°C annealing for both bias. The average relative recovery indicates the recovered value after annealing divided by the preirradiated value.

Table 5.3. Average dose levels at 20% drift and relative recovery after annealing.

Symbol	Parameter	Dose Level/krad(Si)		Relative Recovery	
		V_{CC} = 5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	V_{CC} = 3.3 V
I_{CCSB}	Standby Supply Current	15	25	350	28
I_{CCOP}	Operating Supply Current	25	30	90	30
I_{IL}	Input Current Low Level	40	50	1.1	1.1
I_{IH}	Input Current High Level	40	>60	1.0	1.0
I_{OZL}	Output Leakage Current High Impedance Low level Applied	10	10	0.9	0.9
I_{OZH}	Output Leakage Current High Impedance High Level Applied	10	15	340	100
V_{OL}	Output Voltage Low Level	10	15	20	20
V_{OH}	Output Voltage High Level	>60	>60	1.0	1.0
T_{AOE}	Output Enable Access Time	35	40	-	-
T_{ACS}	CAS Access Time	35	35	-	-

Most of parameters were sensitive to the dose: shifts were evident at 30 krad(Si) dose and dramatic changes occured in several parameters at maximum dose. The parametric changes are considerably larger in 5 V biased devices than in 3.3 V biased ones. The recovery is more efficient in 3.3 V biased devices than in 5 V biased ones.

Parametric test result are given as graphs in appendix 2.

Parametric test conclusion

Parametric data show that the effect of supply voltage tends to modify the TID sensitivity of the devices: the sensitivity is lower at 3.3V than at 5V in terms parametric changes.

6. CONCLUSION

Ionising dose tests were performed on the 16 Mbit DRAM Luna ES/3 from IBM with 3.3 Vand 5 V bias. The dose tolerance of the devices is good.

The comparison of the radiation sensitivity of the IBM devices based on the functional data is difficult because the maximum doses were different and only one device failed during the irradiation. However, the parametric data shows that the effect of supply voltage tends to modify the TID sensitivity of the devices: the radiation sensitivity is lower at 3.3 V than at 5 V in terms parametric drifts.

APPENDIX 1. Functional failures of 5 V IBM DRAM device.

Functional failure of IBM S/N 13:

IBM s/n 13 DRAM 17.3.1997 2:36

82100000,05→00,00,00.

82100001,0A→00,00,00.

82100002,05→00,00,00.

:

82100061,0A→00,00,00.

82100062,05→00,00,00.

82100063,0A→00,00,00.

Explanation

82100000,05→00^1,00^2,00^3.

82100000	memory address with corrupted data
05	original data (CB) in hexadecimal
00^1	corrupted data at first read
00^2	corrupted data at second read
00^3	data after write of original data

APPENDIX 2. Parametric test results for IBM DRAM devices.

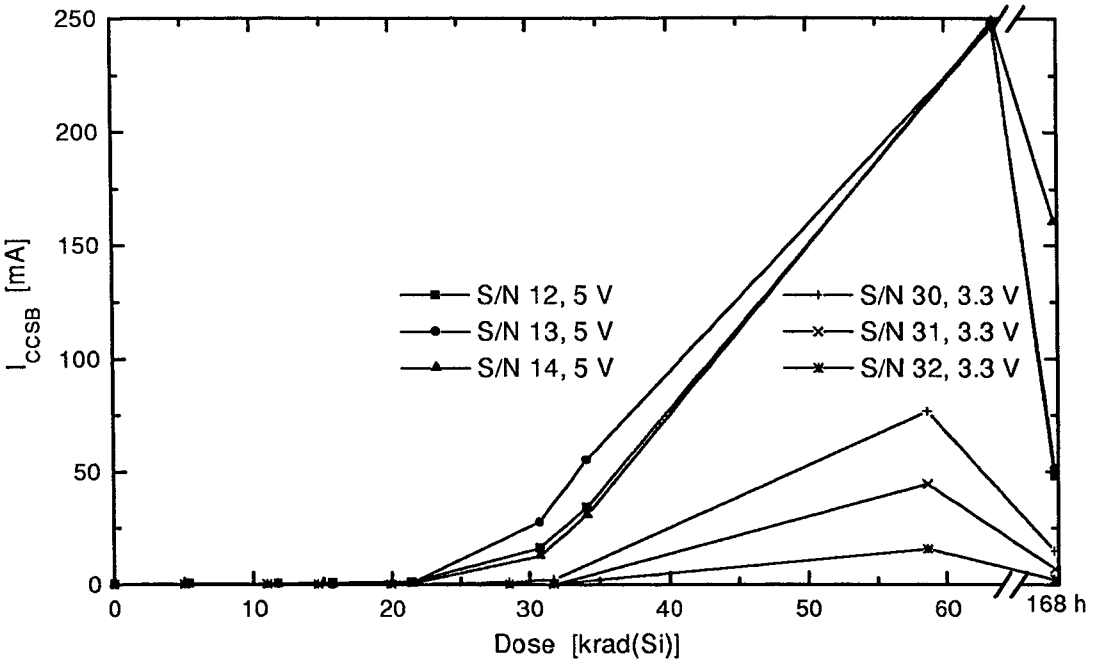

Fig. 1. Standby supply current versus dose and after annealing for IBM DRAMs.

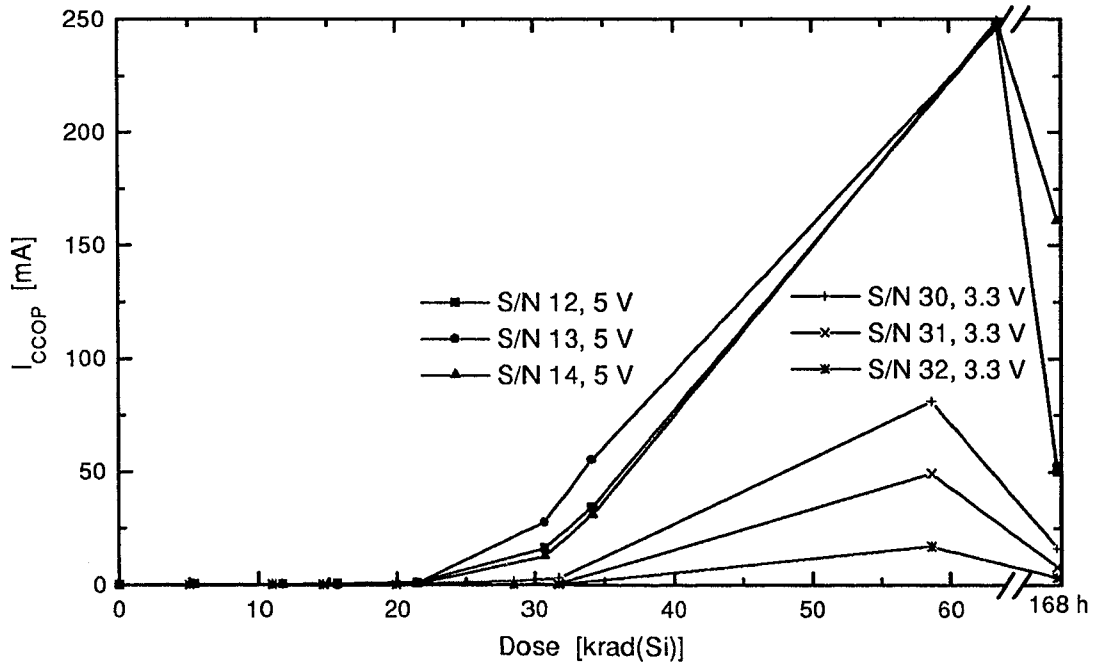

Fig. 2. Operating supply current versus dose and after annealing for IBM DRAMs.

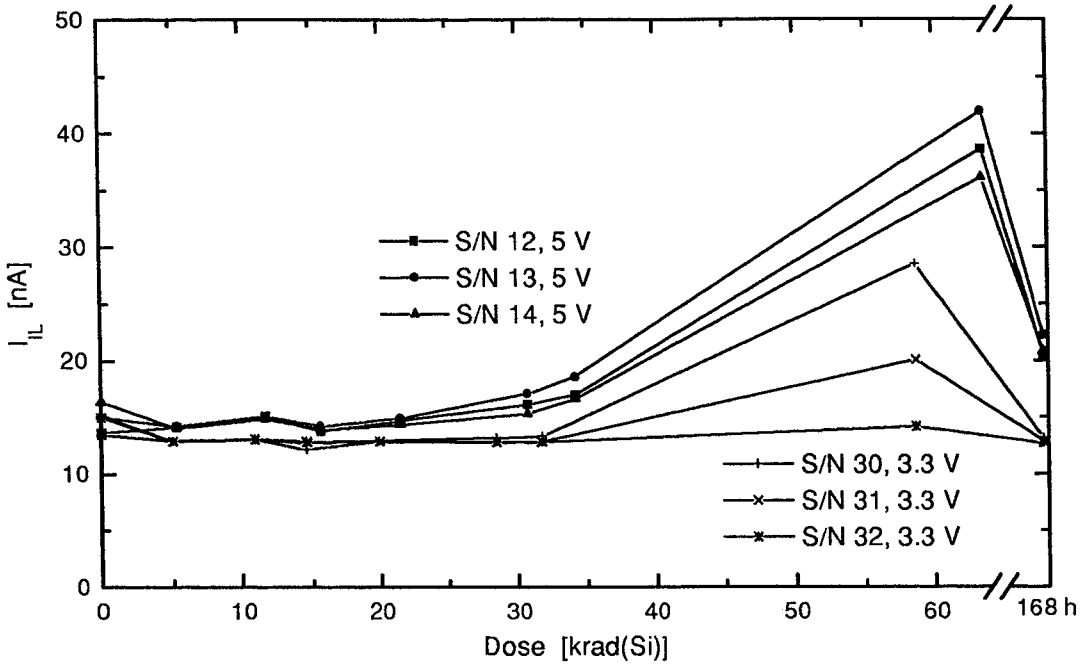

Fig. 3. Input current low level versus dose and after annealing for IBM DRAMs.

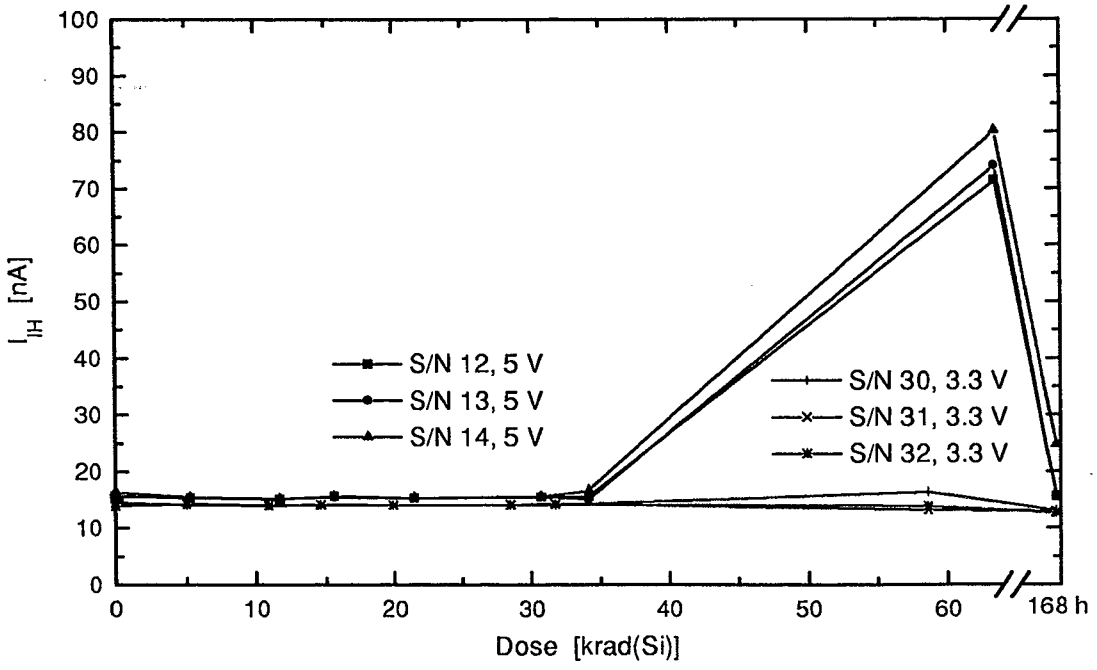

Fig. 4. Input current high level versus dose and after annealing for IBM DRAMs.

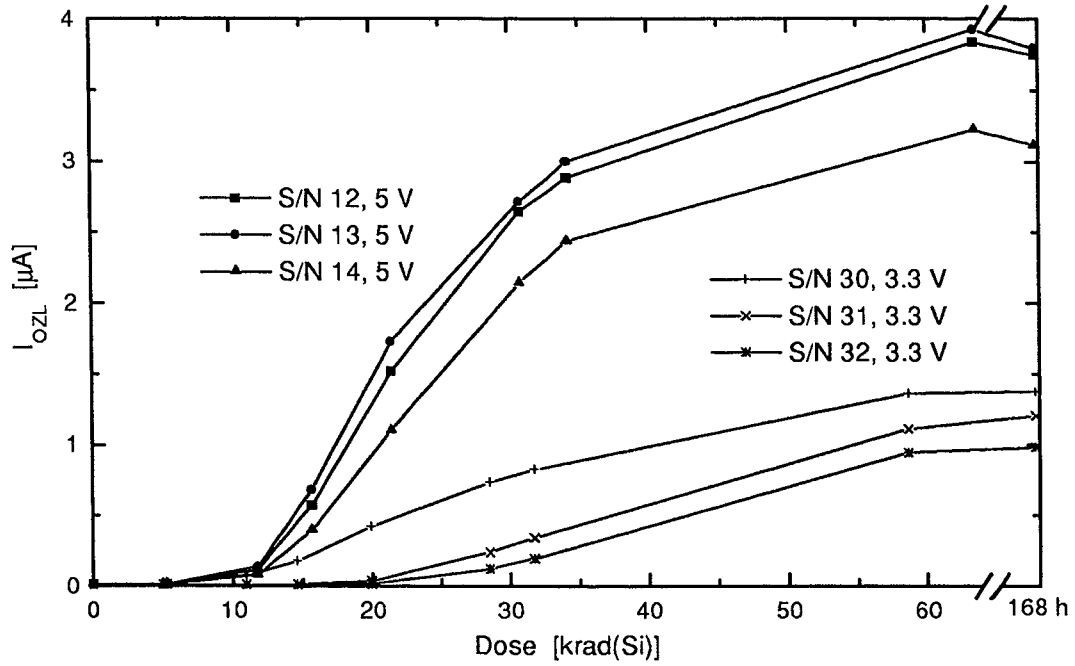

Fig. 5. Output leakage current third state, low level applied versus dose and after annealing for IBM DRAMs.

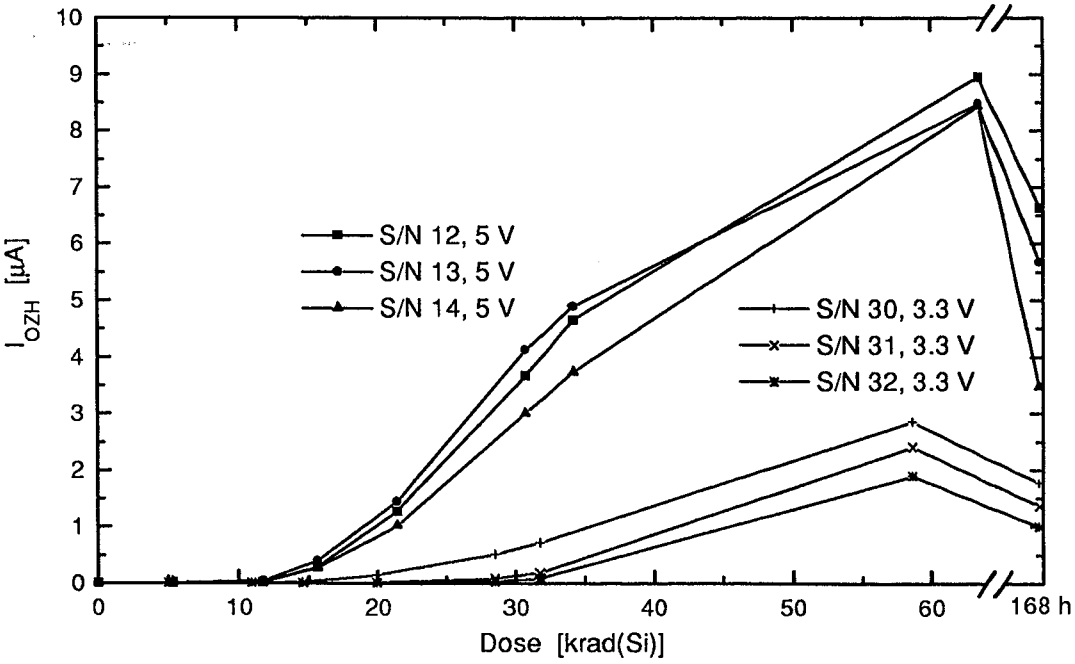

Fig. 6. Output leakage current third state, high level applied versus dose and after annealing for IBM DRAMs.

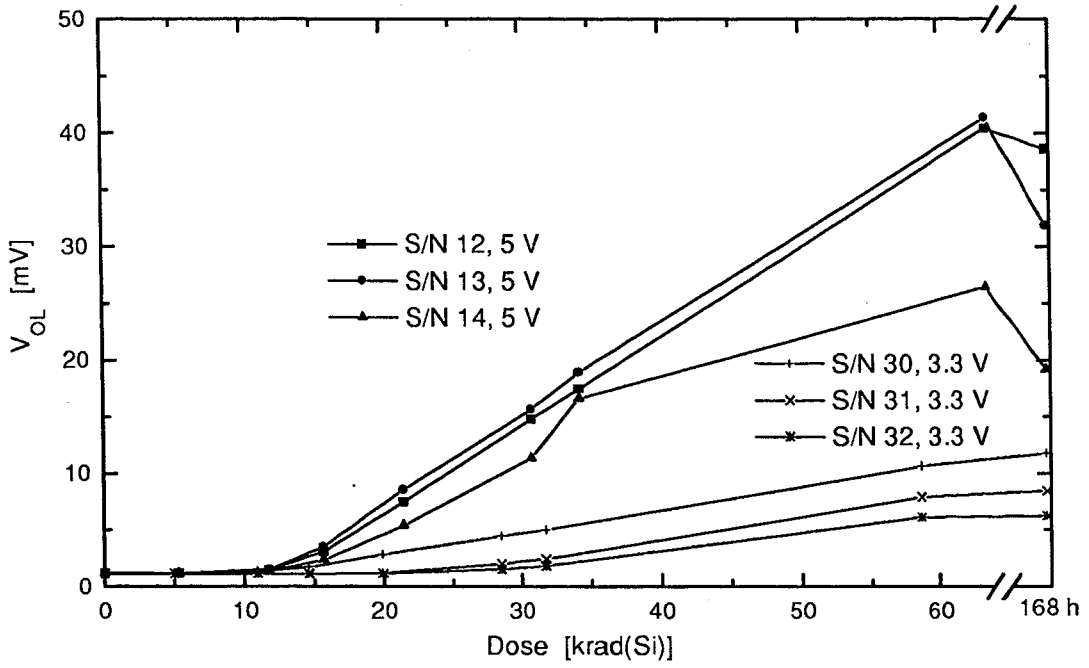

Fig. 7. Output voltage low level versus dose and after annealing for IBM DRAMs.

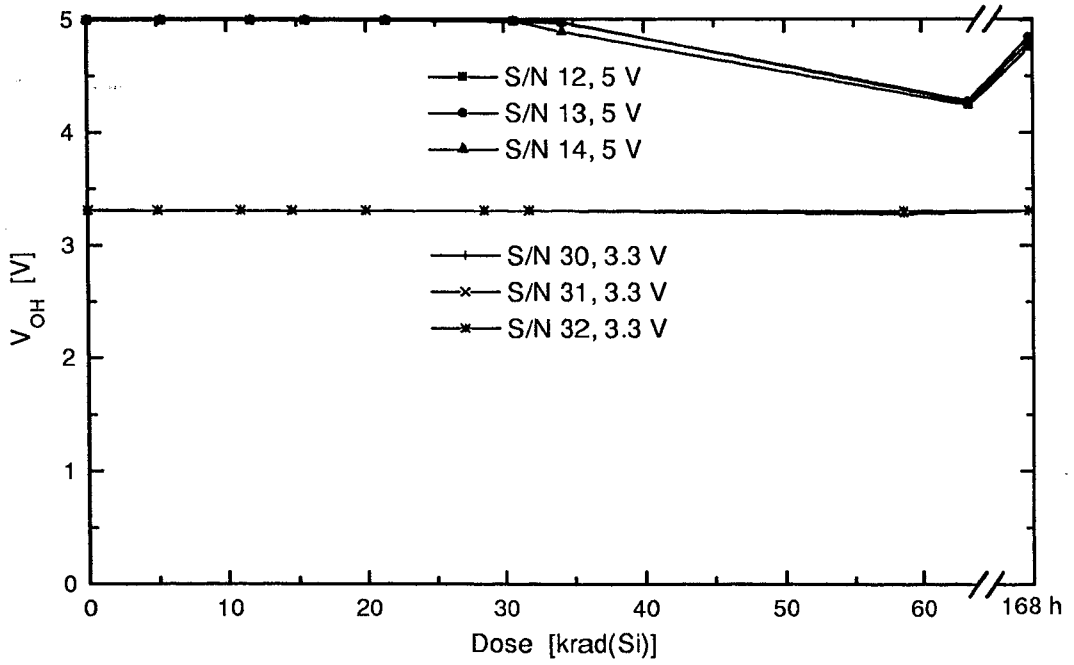

Fig. 8. Output voltage high level versus dose and after annealing for IBM DRAMs.

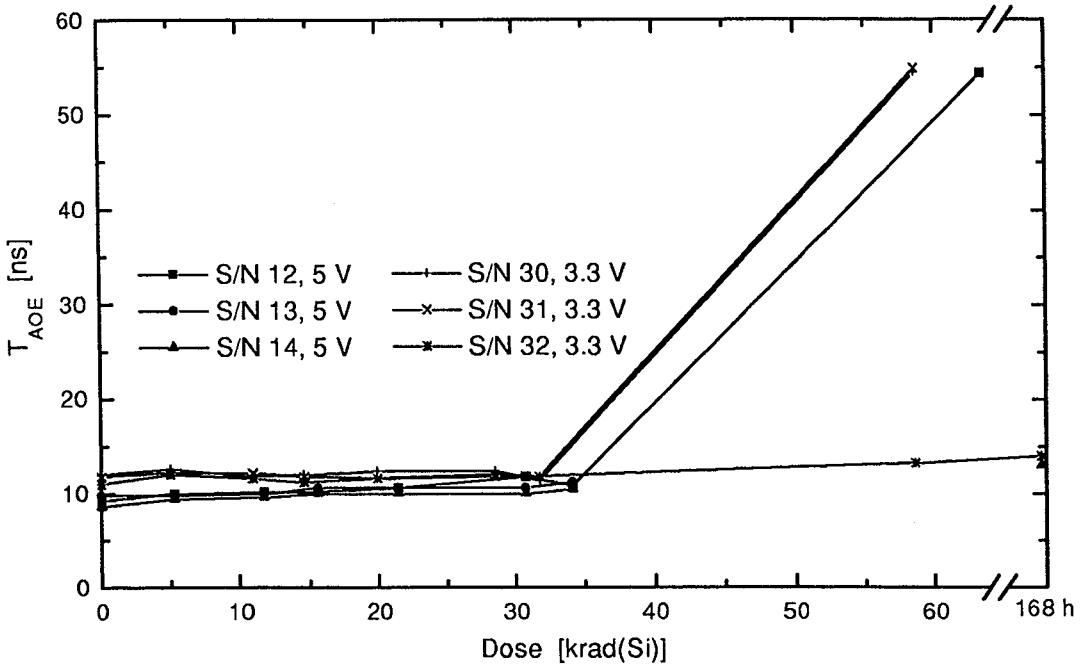

Fig. 9. Output enable access time versus dose and after annealing for IBM DRAMs.

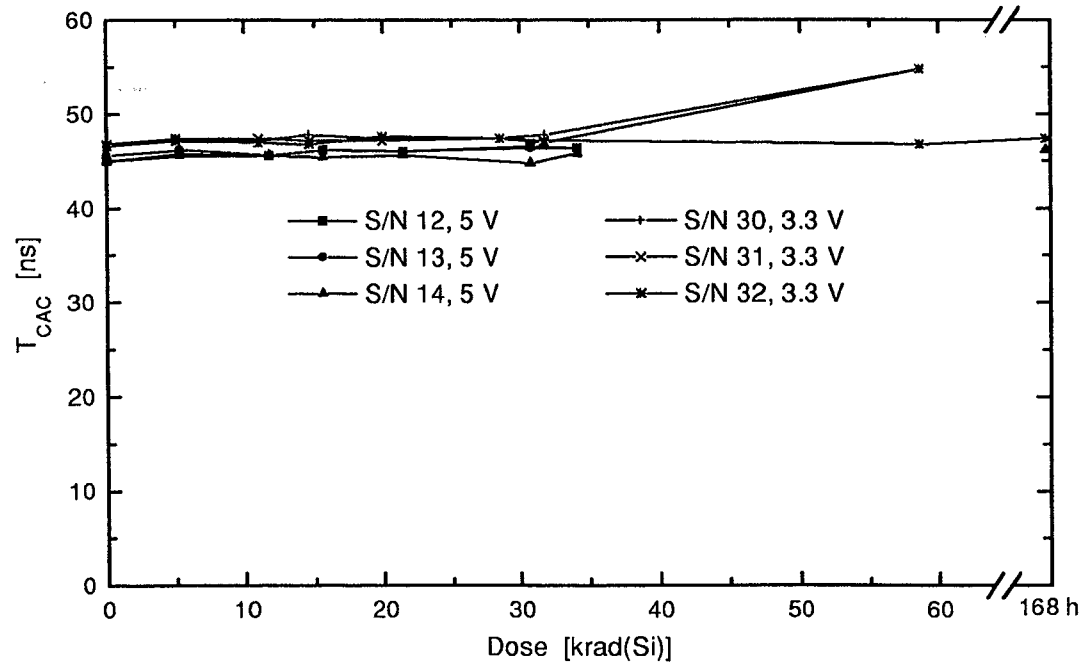

Fig. 10. CAS access time versus dose and after annealing for IBM DRAMs.