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Eddington Demonstration FPA programme

Heavy Ion Single Event Latch-up Test for the RAL CDS/ADC CCD Video Processing ASIC Mk6

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Contents

1 Abstract

These tests were carried out under ESA/ESTEC Contract No. 18470/04/NL/VD dated 14/7/04, covering the radiation tolerance testing (total dose & SEL) of the Mk6 version of the RAL CDS/ADC CCD Video Processing ASIC and the construction and test of a demonstration model Focal Plane Assembly.

A Single Event Latch-up (SEL) Linear Energy Transfer (LET) threshold was found at around 14 MeV/(mg/cm^2), and the SEL LET profile was examined up to 34 MeV/(mg/cm^2). Two devices from a lot of 127 were tested. Included in the report are descriptions of the devices, test set up, test facility, results and conclusions.

2 Introduction

This report presents the results of a heavy ion SEL test program carried out on the Mk6 version of the RAL correlated double sampling ADC ASIC at a 1 MHz sample rate.

The tests were carried out at the European Heavy Ion Facility (HIF) at the Cyclotron, Univesité Catholique de Louvain on 9th November 2004.

3 Reference Documents

[RD1] ESA “Statement of Work Focal Plane Assembly Demonstration Model” (SCI-PT-119)
[RD2] RAL CDS/ADC CCD Video Processing ASIC Design Description Version: 3.4

4 Device Information

4.1 Mk6 ASIC

The Mk6 version of the RAL 16-bit correlated double sampling ADC ASIC was manufactured with a 0.35 μm 'opto' process on 20 μm epitaxial layer silicon, at the Austria Micro Systems (AMS) fab.

4.2 Sample preparation

Three de-lidded Mk6 devices from a lot of 127 were each fitted on separate test boards by the Mullard Space Science Laboratory (MSSL) of University College London. Two devices were used for the SEL tests, one as a spare. Photo 1 shows one of the samples with lid removed.

Designer:	Rutherford Appleton Laboratory (RAL), UK.
Die manufacturer:	Austria Micro Systems
Package facility:	Austin Semiconductor
Package:	84-pin CQFP
Date code:	None
Die marking:	CDS ADC v.6
Die dimensions:	6.75 x 6.75 mm approx.

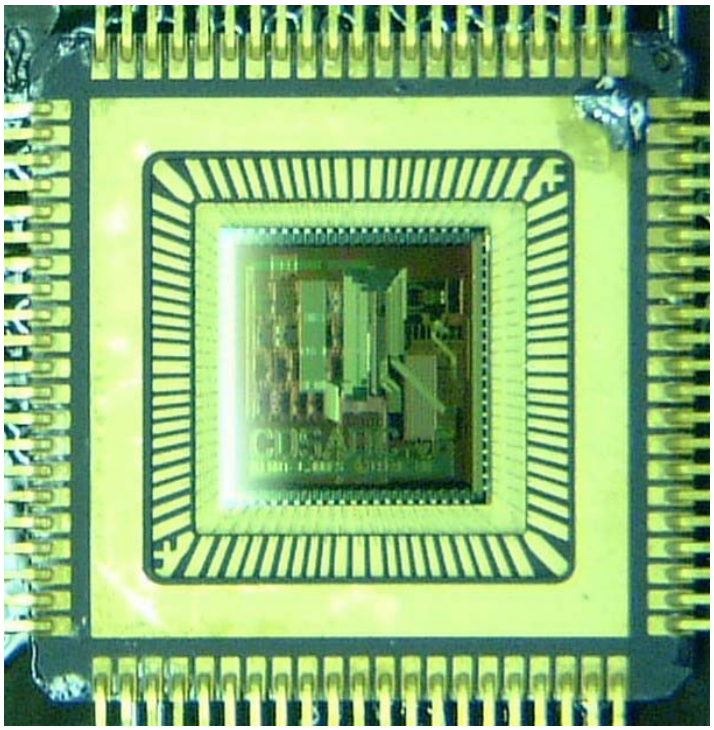

Photo 1. 84-pin CQFP with lid removed showing ASIC die and bond wires

5 Test definition

5.1 Test board

The devices were clocked at 1 MHz with signals generated by an ACTEL proASIC FPGA. The waveform timings were identical to the normal CCD signal digitising mode. A representative analogue CCD signal was also generated as an alternating pixel of approximately 5% and 95% of full-scale video amplitude. The most significant bit was monitored as a check for functional failure. The ADC input offset was set to 0 and the programmable gain amplifier (PGA) gain to 1.

The test boards also included on-board power supply conditioning and control circuitry. Each ASIC had a dedicated +3.3V analogue supply with fold-back current limit set at 235 mA, which is approximately twice the nominal ASIC supply current of 125 mA. The ASIC power conditioning included a current monitor output and reset input for control by the test EGSE (see section 5.2 below). The ACTEL FPGA was powered from a separate external bench supply.

Photo 2 shows the two test boards prior to closure of the HIF test chamber. The CDS/ADC ASICs are positioned, with lids removed, at the bottom of the boards.

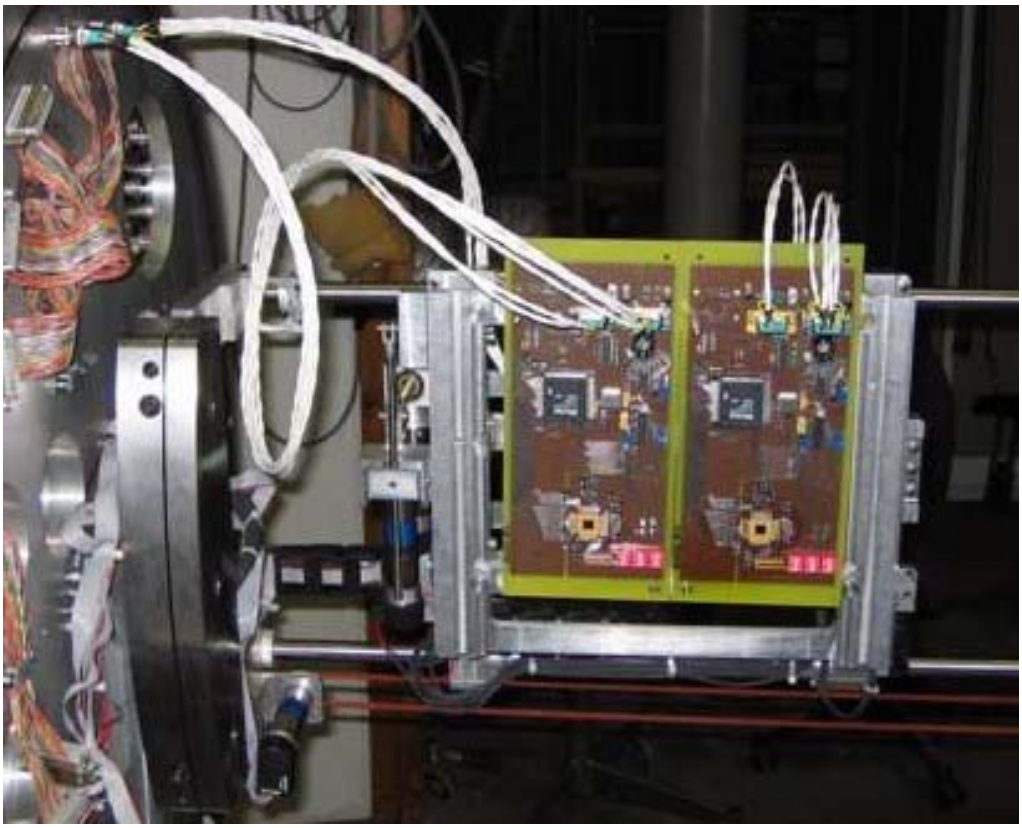

Photo 2. Test boards prior to closure of the HIF test chamber

5.2 EGSE

5.2.1 EGSE Hardware

The EGSE hardware for the HIF test is shown in Figure 1 below. The setup consists of a dual bench power supply, internal and external harnesses, a data acquisition (DAQ) & monitoring system and a manual reset control box. Each ASIC test board is harnessed to a 25 way D-type chamber feed-through allowing testing to be switched between boards by transferring the external harness. Only one board can be tested at a time in this configuration. The dual power supply powers both the ASIC and supporting circuitry during the test. The manual reset box has two functions; the first is a 'Power On Reset', that leaves all devices powered whilst resetting, the second is a current monitor trip that causes the ASIC current limit circuit to power off, simulating an over current condition. The DAQ and monitoring system consists of a laptop PC with USB personal measurement device (PMD) attached. The PMD is an 8 channel, 12-bit resolution, 50ks/s, +/-10 V input ADC.

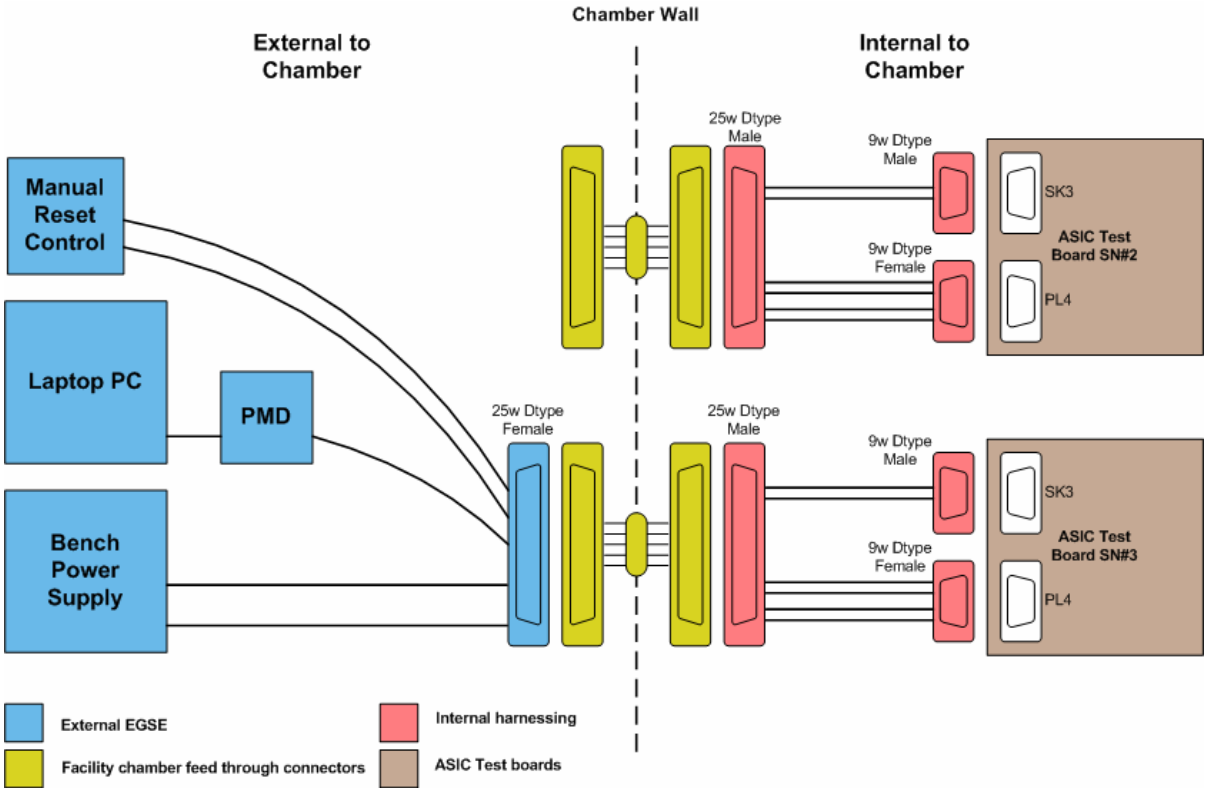

Figure 1. ASIC EGSE test configuration

5.2.2 EGSE Software

The software for the ASIC HIF test was written using Labview 7.1 from National Instruments running under Windows XP. The software serves the following purposes: monitoring the ASIC supply current and the MSB (D15) of the ASIC digital output,

counting SELs and unrecoverable SELs, and alerting the operator to unrecoverable SEL conditions. A screen shot of the ASIC monitor & data logger program is shown below in Figure 2.

The D15 output is passed through a 100μs low pass filter to produce an average value. In the event of the ASIC failing to function as an ADC, the mean level of D15 will deviate from its mid range value of 1.65V. The ASIC supply current monitor and filtered D15 are sampled by the PMD at 200Hz. The ASIC current limiting circuit limits at 235mA for 50ms and then shuts off the current for a further 500ms before powering back on. The sample rate of 200Hz is used to ensure adequate acquisition of the 50ms high current state indicating the ASIC is in latch up.

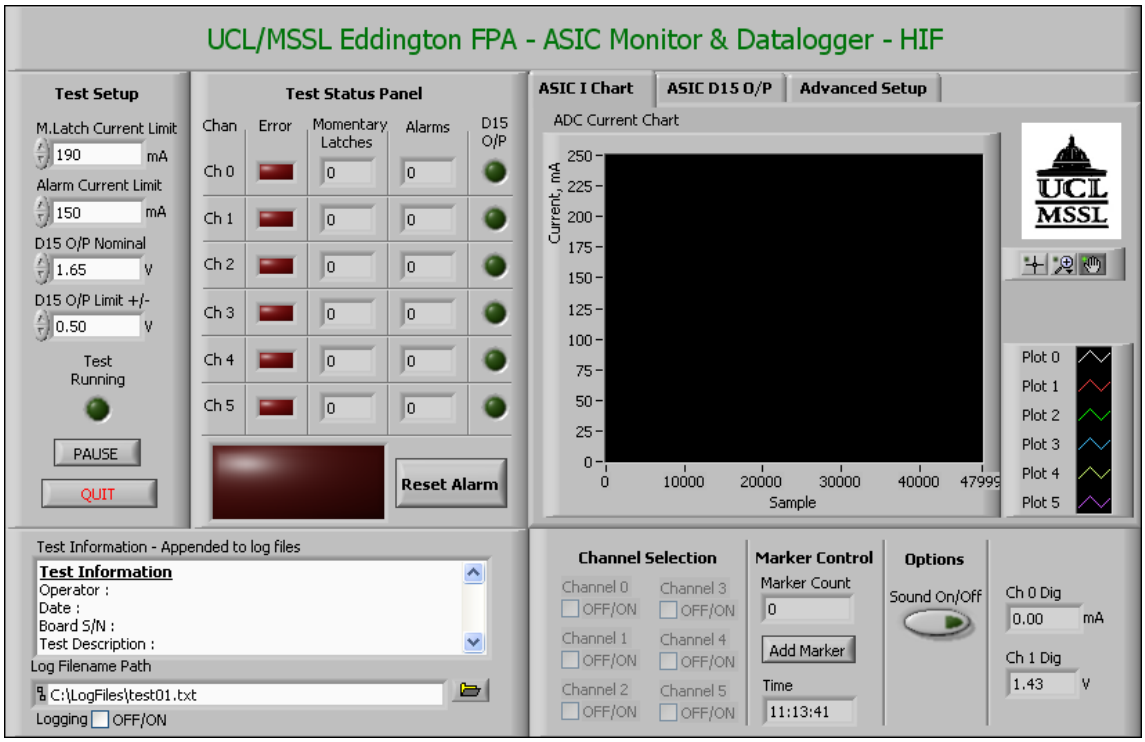

Figure 2. Screen shot of EGSE ASIC monitor & data logger

The ASIC current monitor is primarily used to detect latch up. If the user selectable current threshold 'Latch Current Limit' is passed a SEL is deemed to have occurred. If the user selectable threshold 'Alarm current limit' is passed for >500ms the user is alerted that the device is consuming an increased current and not tripping the onboard limiter. This functionality is included to try to reduce power dissipation from a SEL that does not cause a current trip. If D15 deviates from the user selectable norm by +/- a selectable limit the alarm is also triggered indicating the ASIC has stop functioning as an ADC. A setting of +/-0.2V was used for the test. Logging of all data acquired is written to disk for further analysis.

5.3 Test conditions

The tests were performed at room temperature, under vacuum.

6 Heavy ion test facility

Heavy ion tests were performed at the CYClotron of LOuvain la NEuve (CYCLONE), Belgium using Ne^{4+}, Ar^{8+} and Kr^{17+} ions at the Heavy Ion Facility (HIF). Details of these ions from "cocktail #1" are summarised in Table 1. In order to increase the effective LET range per ion type various angles of incidence were also used.

Ion Cocktail M/Q=4.94	Energy MeV	Range µm Si	LET MeV(mg/cm²)
$^{20}Ne^{4+}$	78	45	5.85
$^{40}Ar^{8+}$	150	42	14.1
$^{84}Kr^{17+}$	316	43	34.0
UCL – Ion Cocktail #1 produced for ESA			

Table 1. Ions used for the ASIC SEL characterization.

Start Time	Run No.	DUT Board	s/n	Ion-Tilt	LET-MeV (mg/cm^2)	Flux p/s/cm^2	Fluence p/cm^2	Dose rad(Si)	Time sec.	Results SEL
04:55	1	Board 2	2	Ne-0	5.85	5.00E+03	1.00E+06	94	237	0
05:00	2	Board 2	2	Ne-45	8.27	3.50E+03	1.00E+06	132	296	0
05:06	3	Board 2	2	Ne-60	11.70	2.50E+03	1.00E+06	187	416	0
05:32	4	Board 2	2	Kr-0	34.00	1.00E+03	6.00E+05	328	323	85
05:45	5	Board 2	2	Ar-0	14.10	5.00E+03	1.00E+06	226	203	0
05:50	6	Board 2	2	Ar-45	19.90	3.50E+03	1.00E+06	320	294	16
05:55	7	Board 2	2	Ar-60	28.20	2.50E+03	1.00E+06	452	399	74
06:04	8	Board 2	2	Ar-35	17.20	4.00E+03	1.00E+06	276	253	6
06:09	9	Board 2	2	Ar-30	16.30	4.00E+03	1.00E+06	261	253	4
06:14	10	Board 2	2	Ar-25	15.60	4.00E+03	1.00E+06	250	215	4
06:19	11	Board 2	2	Ar-20	15.00	4.50E+03	1.00E+06	240	228	0
06:25	12	Board 3	3	Ar-0	14.10	5.00E+03	1.00E+06	226	200	1
06:30	13	Board 3	3	Ar-45	19.90	3.50E+03	1.00E+06	320	309	16
06:37	14	Board 3	3	Ar-60	28.20	2.50E+03	1.00E+06	452	386	63
06:48	15	Board 3	3	Ar-25	15.60	4.00E+03	1.00E+06	250	266	3

Table 2. Detailed results per run.

7 Results

Test run data and information together with SEL results for both devices are given in Table 2 above. As can be seen, s/n 2 showed a SEL LET threshold of 15.6 MeV/(mg/cm^2) a value slightly higher then the value recorded for s/n 3 of 14.1 MeV/(mg/cm^2). The accumulated total dose recorded for s/n 2 was 2.8 krad(Si) while s/n 3 received 1.5 krad(Si). Further SEL results for both devices are plotted in Figure 3. The latch-up behavior can be concluded to be very consistent for the two parts with a SEL threshold of about a LET of 14.1 MeV/(mg/cm^2).

For each incidence of an SEL shown in Table 2, the on-board power supply conditioning and control circuitry succesfully switched off the power to the ASIC and then recovered the current to its nominal level of 125 mA. The EGSE was set to count current levels exceeding 150 mA, i.e. 25 mA above the nominal 125 mA. No human intervention was required to switch off the power at the bench supplies.

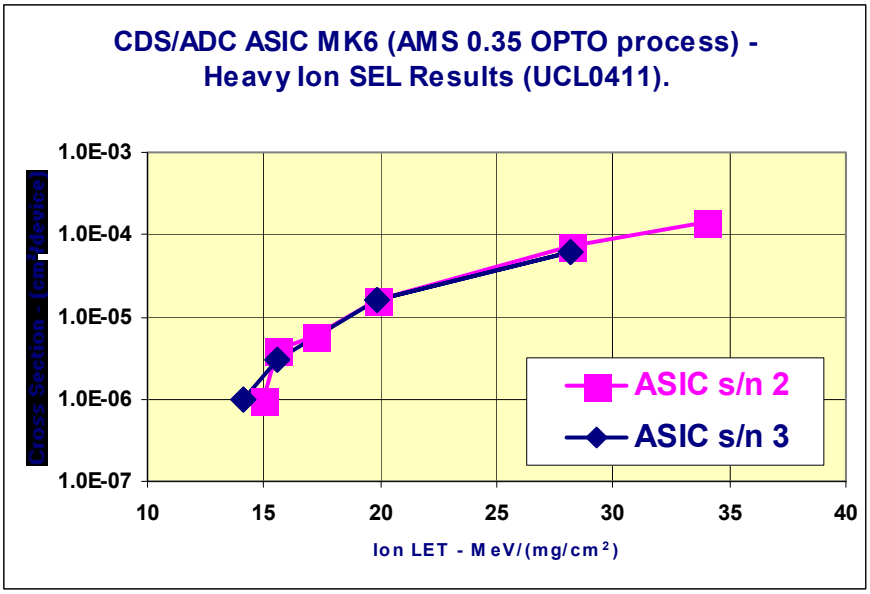

Figure 3. Latch-up sensitivity versus ion LET.

8 Conclusion

Two Mk6 CDS/ADC CCD Video Processing ASIC devices were heavy ion SEL tested at the European Heavy Ion Facility at the Cyclotron, Université Catholique de Louvain on 9th November 2004. An interesting set of results were obtained. Both devices showed identical latch-up behavior with a SEL LET threshold around 14 MeV/(mg/cm^2). The devices were manufactured with a 0.35 μm 'opto' process on 20 μm epitaxial layer silicon, from Austria Micro Systems (AMS).

9 Acknowledgements

MSSL wishes to thank the European Space Agency, particularly Reno Harboe-Sorensen, and the team at the Heavy Ion Facility at Louvain, for their constructive support in the planning and operation of the tests.