# Application-Like Radiation Test of XTMR and FTMR Mitigation Techniquers for Xilinx Virtex-II FPGA

## Final Presentation of ESTEC Contract

## No. 11407/95/NL/MV, CCN-5, COO-7

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# PURPOSE

- Investigate validity of TMR on SRAM based Xilinx FPGA
  - Two TMR Mitigation Methologies
    - FTMR – VHDL code mitigation general for any FPGA/ASIC
    - XTMR – Xilinx specific TMR tool ( in our case implemented by Xilinx)
- Purpose was to Compare the Two Techniques, But

  After first test campaign, it was concluded that FTMR did not mitigate all logics, Xilinx Place & Route tool introduced new nets that were not tripled. The nets were used to control static inputs to basic the FPGA architecture
- All given test data is XTMR

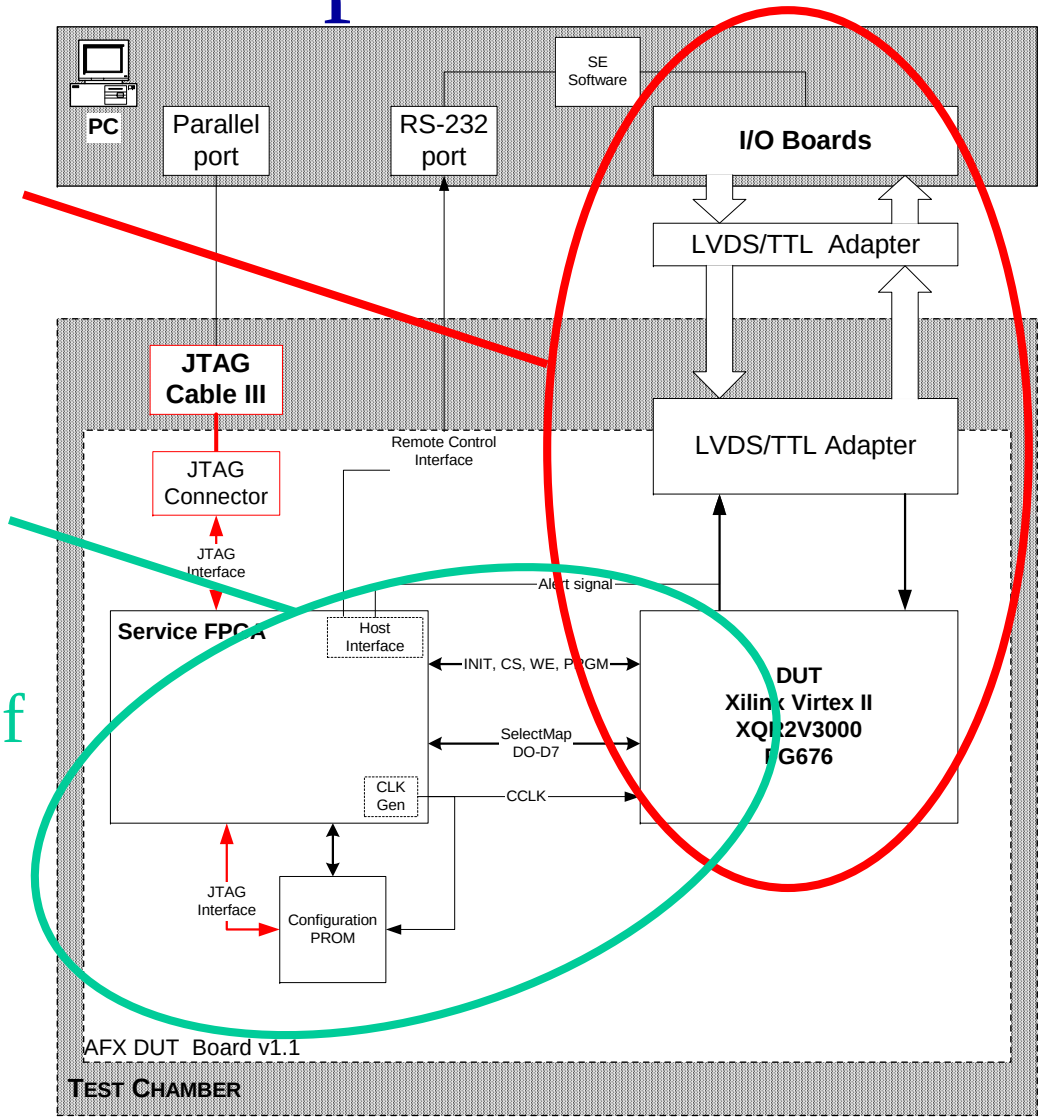
# Upsets and Error detection

- Upsets in Xilinx Virtex-II,
  - SEU in user logic flip-flop, - Mitigated by XTMR???
  - SEU in configuration data ( Functional Errors ) - Mitigated by XTMR???
  - SEU in control registers (SEFI) - No Mitigation

- Error domains
  - *Data Error*, local error corrected with new configuration data
  - *Stuck Error*, local error NOT corrected with new configuration data
  - *SEFI*, device not functional at all.

# Test Setup

- ”DUT-Tester”
  - Records data errors from DUT
- Service FPGA
  - Scrubs configuration data into DUT from PROM
    (10 MHz gives 5 scrubs/second)
  - Monitor some types of SEFIs.
  - Reconfigure (reset) DUT when SEFI is detected



# Tested DUT Designs

## Xilinx TMR Tool ”XTMR”

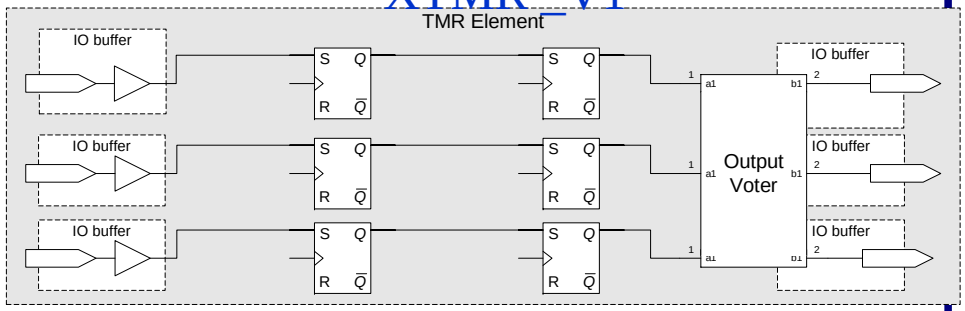
- Design Modules
  - 2x ”FFT”; Fast Fourier Transform (Application like)
    - Complex design with mix of combinatorial and sequential logics
  - 2x PSR; Pseudo Randomizer (Not application like)
    - Mostly sequential logic functional similar to a 60 bits shift register
- 3 Design variants tested
  - Non-TMR
  - XTMR_V1
  - XTMR_V2
- Tripling of routing & logics, inputs & outputs

a,

Non-TMR

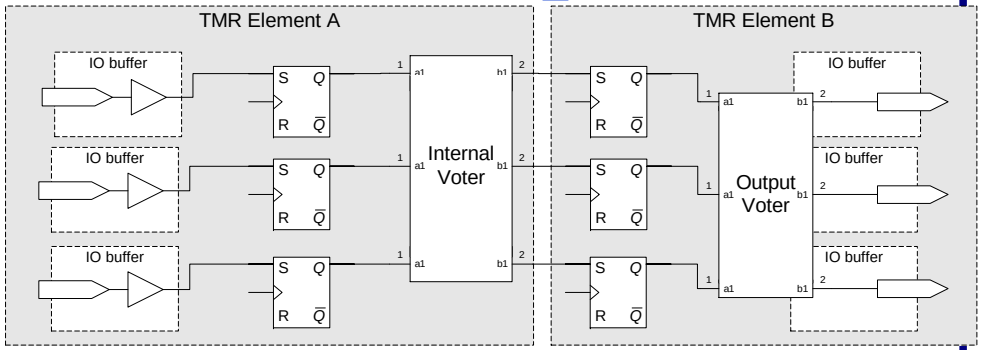

b,

XTMR_V1

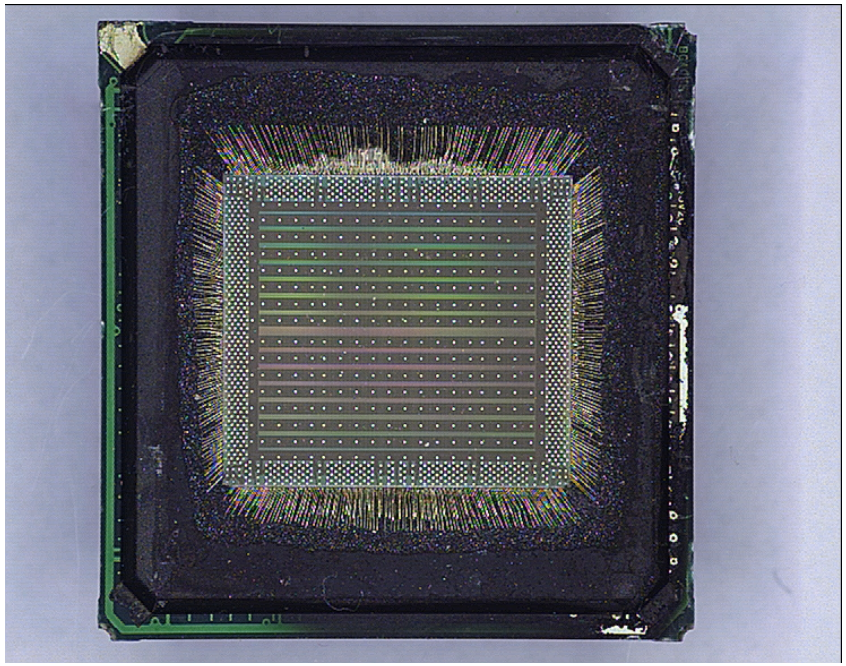



c,

XTMR_V2

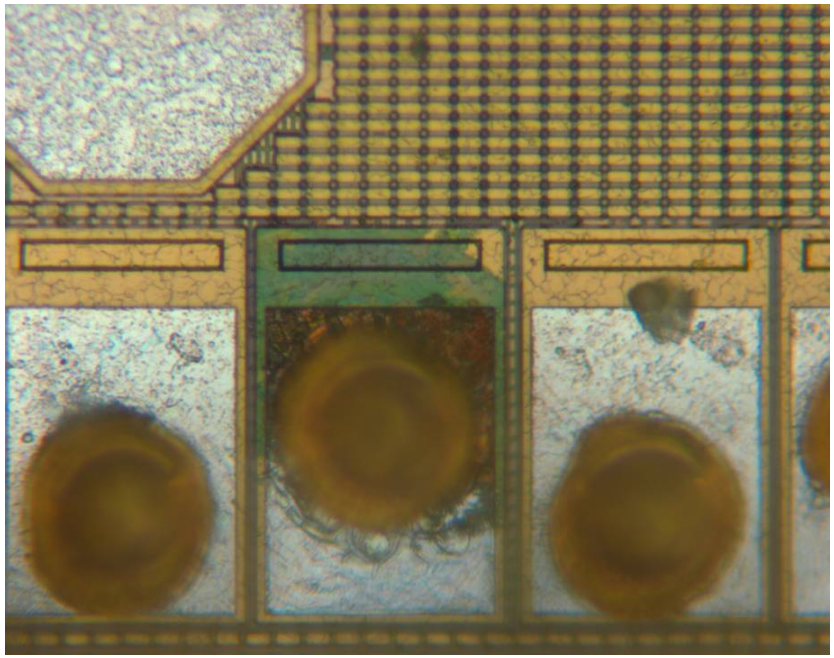


# TEST SAMPLE & FACILITY



Xilinx Virtex II XQR2V3000
0.15µm CMOS 8-layer metal process with epitaxial layer
676-pin Plastic FP

die size 16x16 mm



*Bond pad affected by chemical etching*.

Facilities - HIF/Belgium & RADEF/ Finland

- Wasted lot of beam time not giving test results
  - Bad test samples
  - FTMR not mitigated
  - XTMR_V1 => XMTR_V2

# Error cross section for “non-TMR” Design

(Number of Care Bits estimated from XTMR_V1)

| | Module | Cross Section Si [ cm2 / Care Bits ] (11 MeV cm2/mg) | Cross Section 60 MeV proton [ cm2 / Care Bits ] |
|---|---|---|---|
| XTMR_V2 | FFT | 5,3E-09 | 9,0E-15 |
| | PSR | 4,0E-09 | 5,8E-15 |
| XTMR_V1 | FFT | 4,5E-09 | |
| | PSR | 4,8E-09 | |

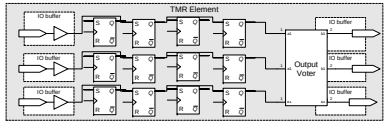
JPL ~1E-08

Too Few data points for a full SEE characterization

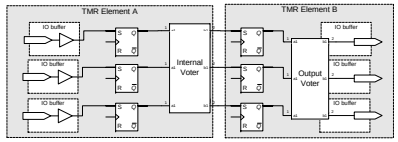
# Cross Sections PSR

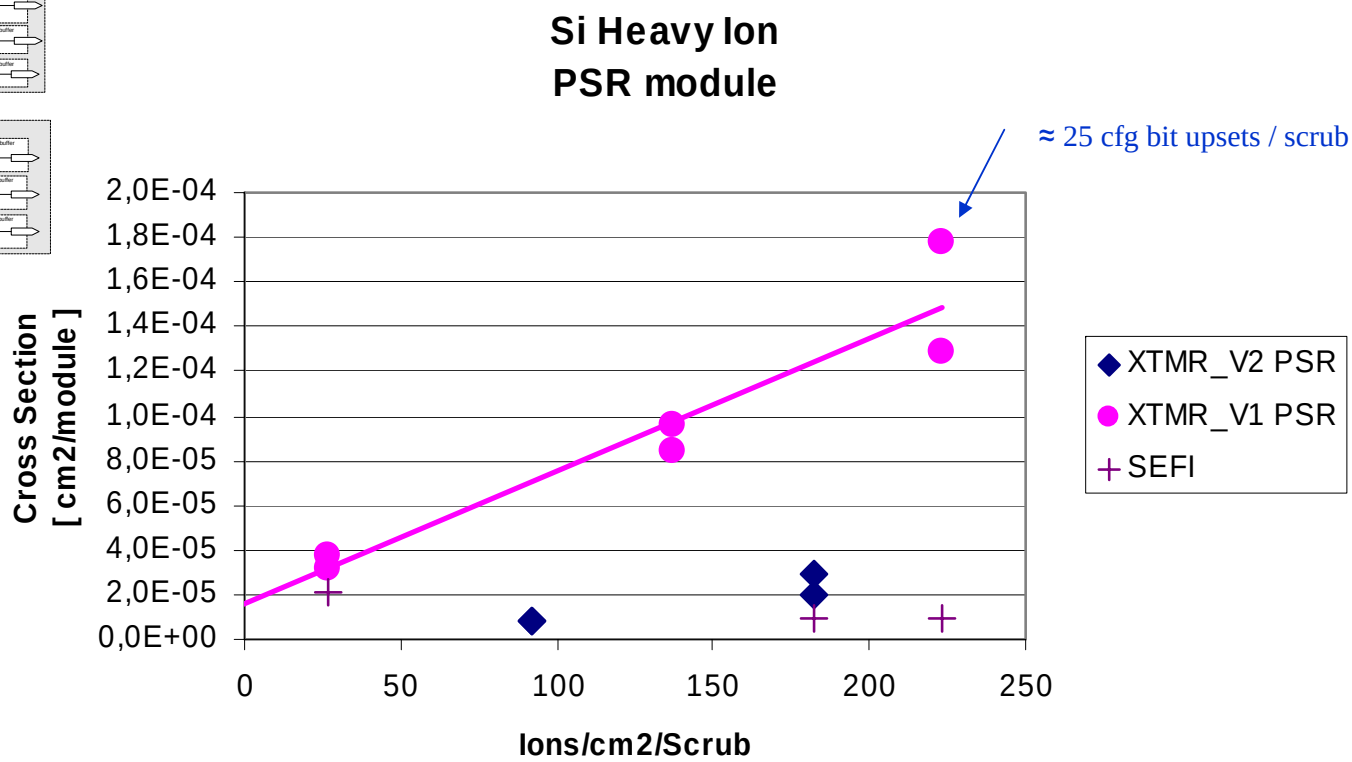
## Comparison PSR Module in design variant XTMR_V1 & XTMR_V2

V1




V2



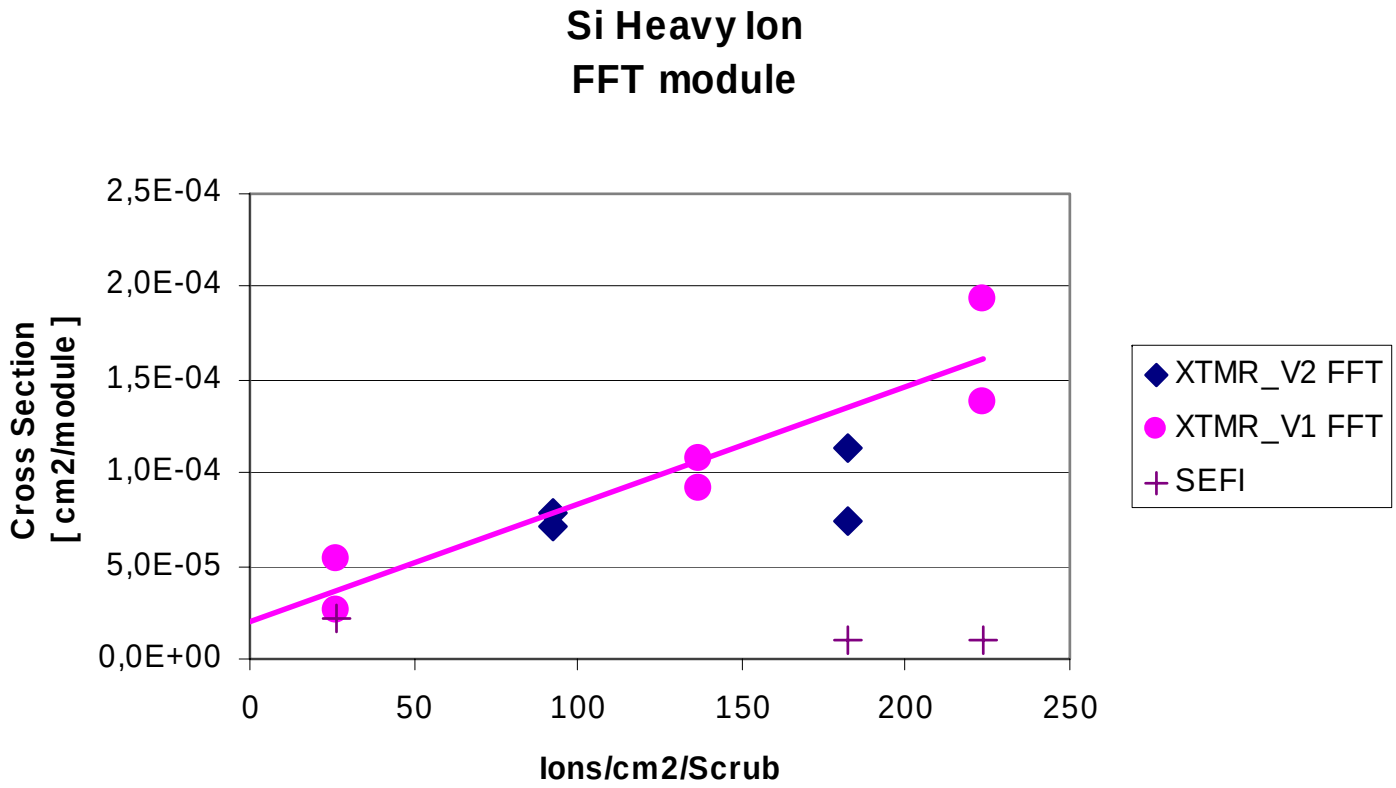




SEFI = No flux dependence
V2 = Small flux depedence
V1 = Large flux dependence

| ***Resource usage*** | FF | LUT | ”Care bits” |
|---|---|---|---|
| XTMR_V1 | 16% | 12% | 6% |
| XTMR_V2 | 16% | 41% (add of voting circuits) | 13% |

# Cross Sections FFT

## Comparison FFT Module in design variant XTMR_V1 & XTMR_V2

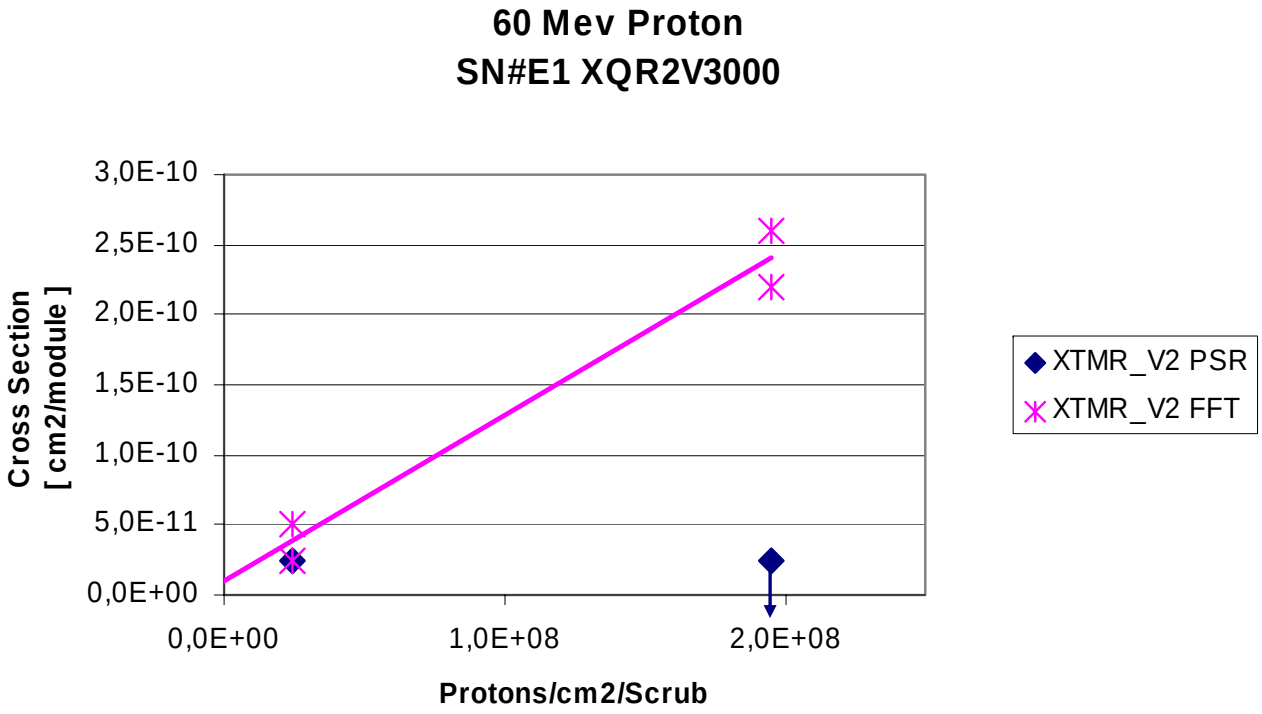



SEFI = No flux dependece
V2 & V1 = Similar flux depedence

| ***Resource usage*** | FF | LUT | ”Care bits” |
|---|---|---|---|
| XTMR_V1 | 8% | 38% | 16% |
| XTMR_V2 | 8% | 40% (small add of voters) | 17% |

# Cross Sections Proton Data

## Comparison PSR vs FFT




- No SEFI Detected (low fluence)
- Data taken on both etched and non-etched samples with the same results

| ***Resource usage*** | FF | LUT | ”Care bits” |
|---|---|---|---|
| FFT | 8% | 40% (small add of voters) | 17% |
| PSR | 16% | 41% (add of voting circuits) | 13% |

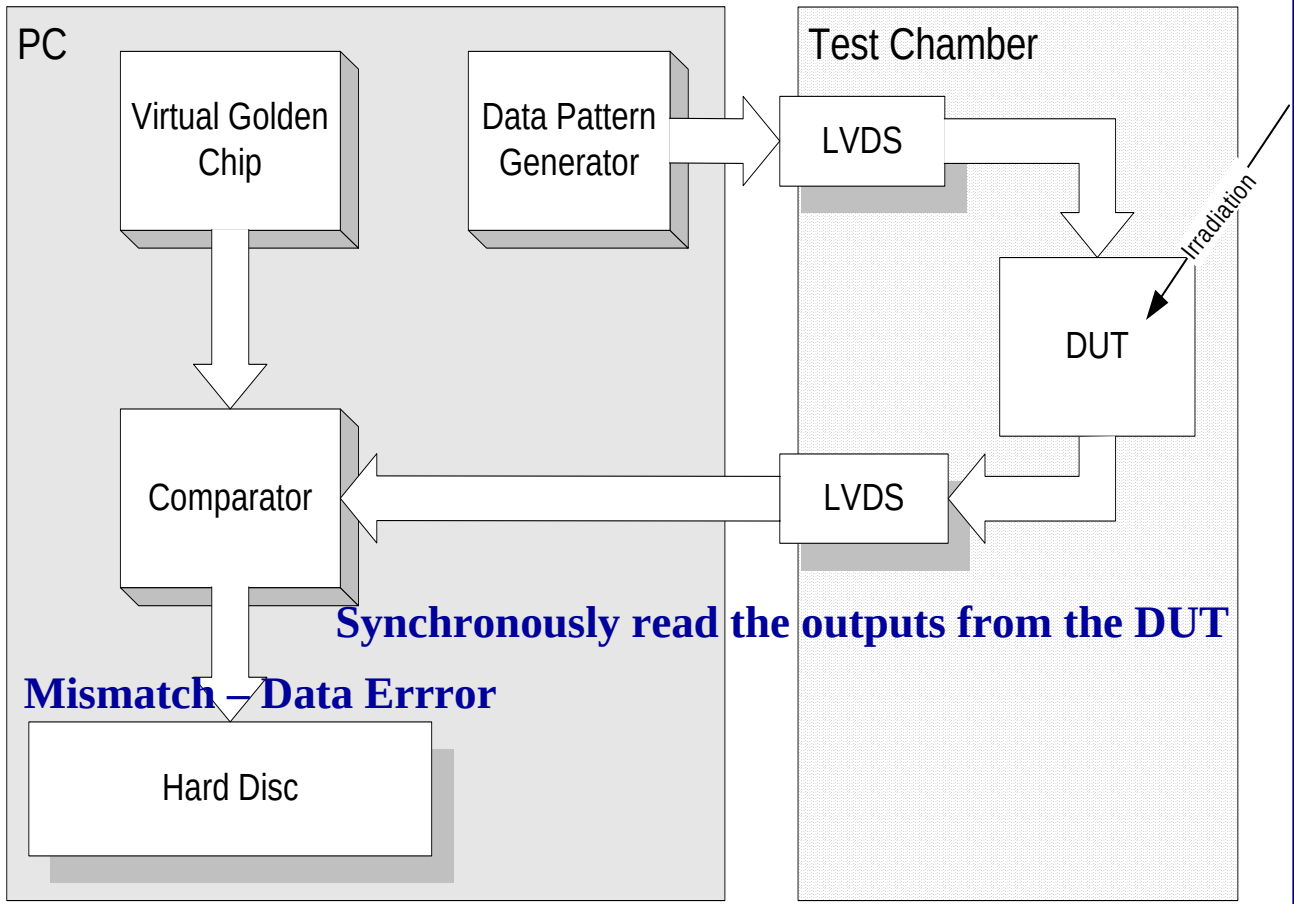
# Summary

- Xilinx Virtex-II, 676-pin plastic FP chemically etched by Xilinx
  - Bond lifts and partly damaged bonds, five etched samples were considered functional but not 100% reliable
  - Verification against non-etched sample in proton test were found to give the same results
  - Cross Section per SRAM cell in agreement with earlier measurements
- Clear flux dependence observed
  - Scrub Rate 4,9 scrub/sec
  - Flux in Accelerators high compared to space environment
- Two copies of each module in DUT design
  - Clear spread in cross section results:
    - Not identical routing implemented by Xilinx Place&Route???
    - Non- homogeneous beam over test sample???
- Simple Design (PSR) and low flux indicate TMR errror rates in the same order or magnitude as for SEFI
- No full SEE characterization
  - Test data only for 1 LET value and one proton energy

# PRINCIPAL of TEST SYSTEM ”DUT-Tester”

*Data Pattern Generator* continuously streams input test vectors into the DUT

- Max Data Flow
  - 10 Mbyte/s
- Max Clock Speed
  - 80 MHz
- Max I/O’s
  - 96



# Resource usage for all DUT design variants

| | Non-TMR | One FFT module | One PSR module | XTMR_V1 | XTMR_V2 | Total available |
|---|---|---|---|---|---|---|
| Number of FF | 2140 (7%) | 1050 (4%) | 2160 (8%) | 6420 (22%) | 6420 (22%) | 28672 |
| Number of LUT | 4238 (15%) | 5511 (19%) | 1812 (6%) | 14460 (50%) | 23287 (81%) | 28672 |
| Number of IOB | 26[1] (5%) | 12 (2,5%) | 24 (5%) | 81[1] (16%) | 81[1] (16%) | 484 |
| Number of MULT18X18 | 24 (25%) | 36 (37%) | 0 (0%) | 72 (75%) | 72 (75%) | 96 |
| Number of GCLK | 1 (6%) | - | - | 3 (18%) | 3 (18%) | 16 |
| Number of “Care Bits” | 508749 (5%) | 719404 (8%) | 318144 (3%) | 2075095 (22%) | 2854971 (30%) | 9582848 |