# SEE and TID Acceptance Tests of the Radiation Test-Bed for High Capacity Memory Components

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# Outline

1. Design of RTMC-3 Test-Bed
2. Verification of RTMC-3 with SRAMs
   - TID Test Verification
   - SEE Test Verification
3. Test and Evaluation of “state of the art” Memories: SEE Tests of NAND Flash
4. Conclusions

# 1. Test-Bed Design Approach

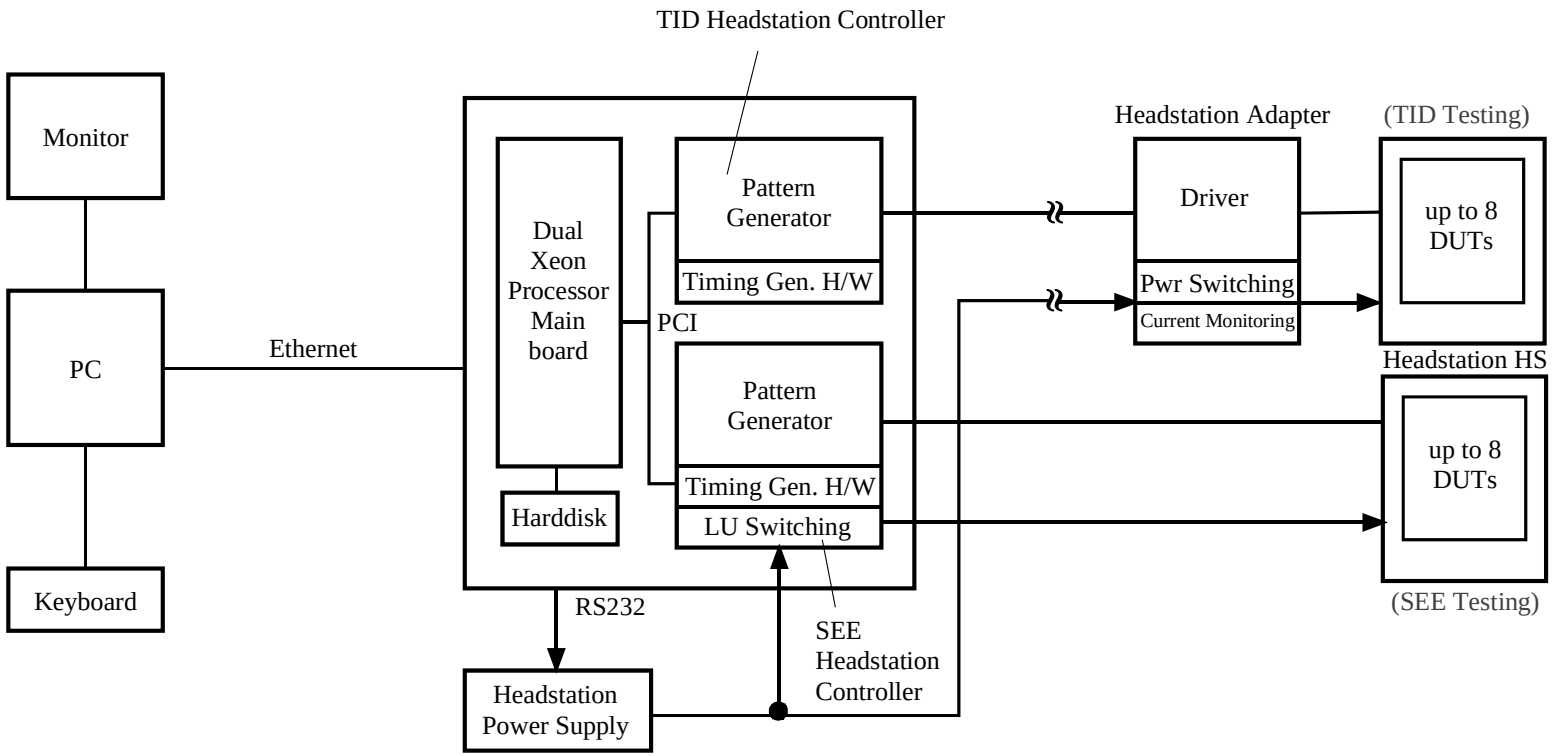
Test-Bed design mainly driven by four requirements:

- In situ testing
  - to detect and to isolate transient functional errors
- Real time event detection and recording
  - isolation of special SEE types (cluster errors, partial SEL)
  - complete testing of large capacity devices within reasonable test time
- Flexible and easily adaptable platform
  - test bed adaptable to sophisticated „memory systems on chip“ in a short time frame
- Flexible support of data evaluation

# 1. Test-Bed Implementation

- PC based H/W supported system (Fast Test Unit) with special plug-in cards for real time functions of TID and SEE-tests (Head Station Controller)
  - Adaptable device control and test patterns implemented in firmware within configurable XILINX FPGA´s
- Easily configurable test-bed S/W IDA GSEOS V
  - Operational and loop control
  - Quick-Look data analysis to support in-situ tests
  - Detailed data evaluation after tests
- Remote control of in-situ tests via network

# 1. RTMC-3 Block Diagram



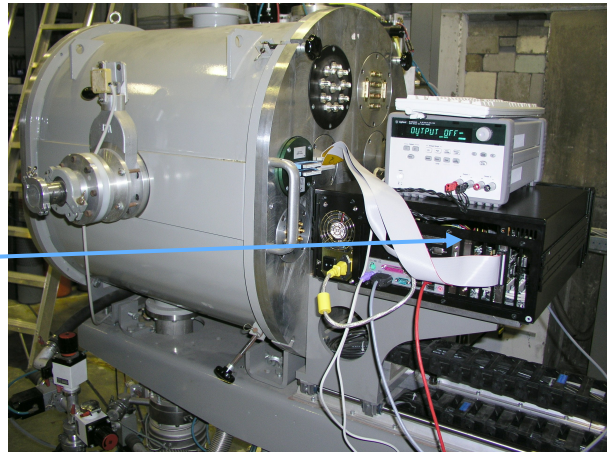

**Remote Control Unit RCU**

**Fast Test Unit FTU**
**PC + up to 5 Headstation Controller**

**DUT-Test Adapter**

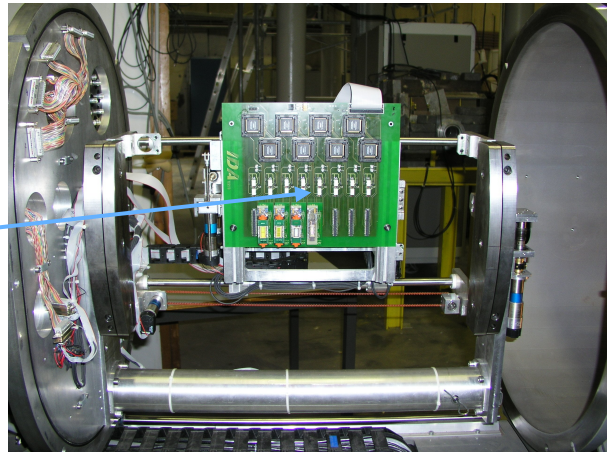
# 1. RTMC-3 Test-Bed

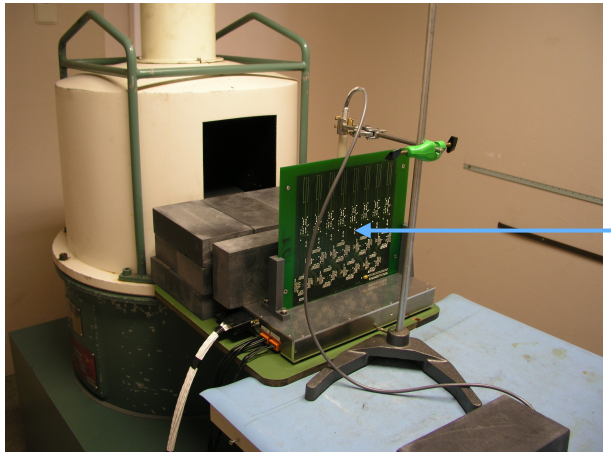
FTU



RCU

HS-SEE





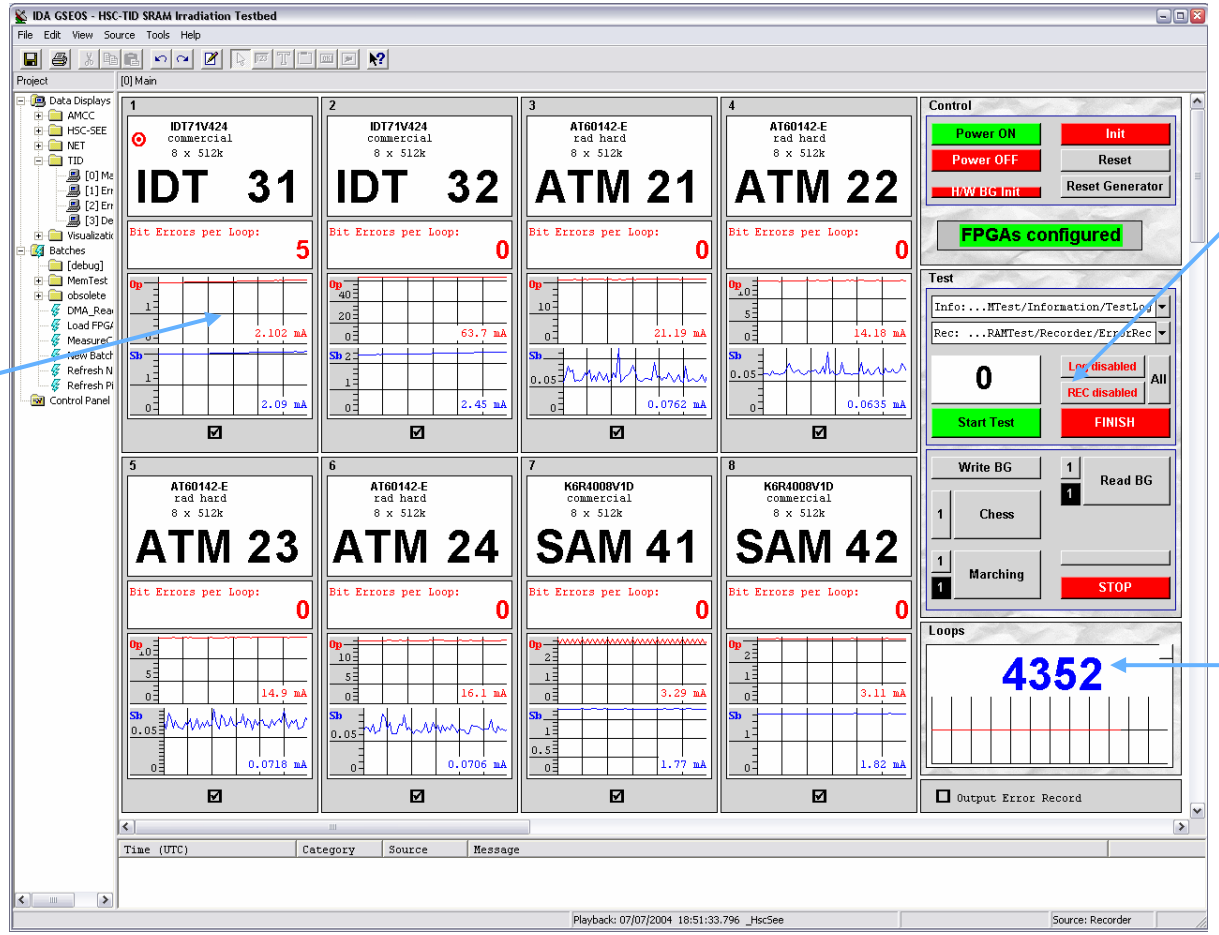
HS-TID

# 2. TID-Test Verification

- Test Facility: ESTEC Co60, ~3600 rad/hour
  - Devices: SRAM, 8 DUTs:
    (Atmel AT60142-E, IDT IDT71V424L12PHI,
    Samsung K6R4008V1D)
- Test-Bed:
  - Autonomous simultaneous in-situ test of all 8 DUTs
  - Continuous measurement of active/stand-by currents
  - Complete recording of events, i.e. currents, data errors and device failures
  - Real time visualization of all data
  - Autonomous S/W supported over-current protection

# 2. TID-Test Verification

**DUT Quick-look (error counts, currents, device failures)**

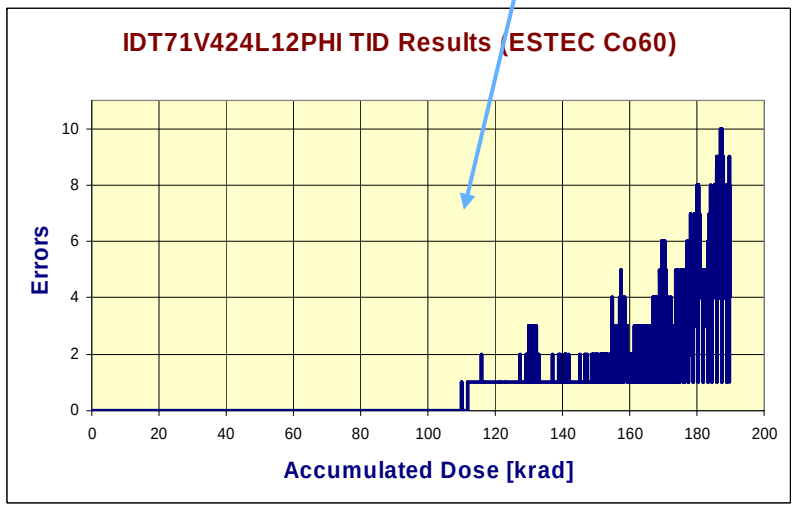


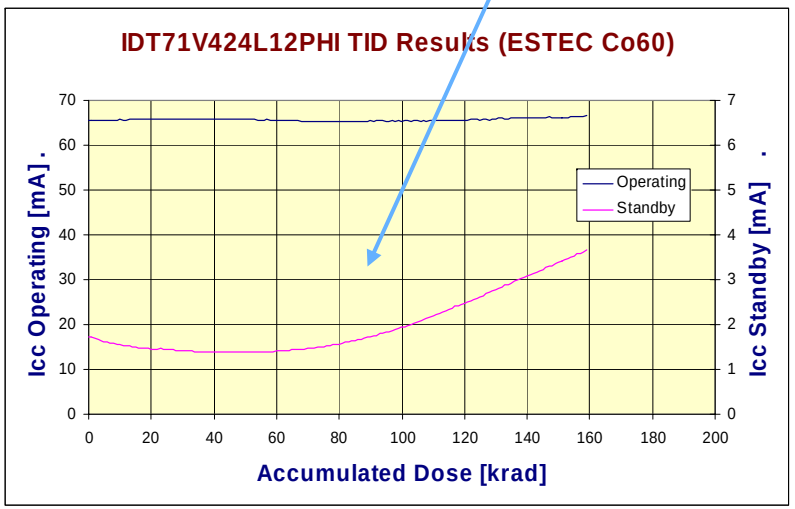

**Operational Control**

**Loop Counter**

# 2. TID-Test Verification

| Type | 1st Error, D [krad] | Device Failure, D [krad] | Current Increase, D [krad] |
|---|---|---|---|
| Atmel AT60142-E | >167.40 | >167.40 | - |
| Atmel AT60142-E | >167.40 | >167.40 | - |
| Atmel AT60142-E | >167.40 | >167.40 | - |
| Atmel AT60142-E | 128.98 | >167.40 | - |
| IDT IDT71V424L12PHI | 110.04 | >189.72 | 88.50 |
| IDT IDT71V424L12PHI | 136.46 | >159.00 | 85.30 |
| Samsung K6R4008V1D | >189.72 | >189.72 | - |
| Samsung K6R4008V1D | 7.96 | >130.67 | - |



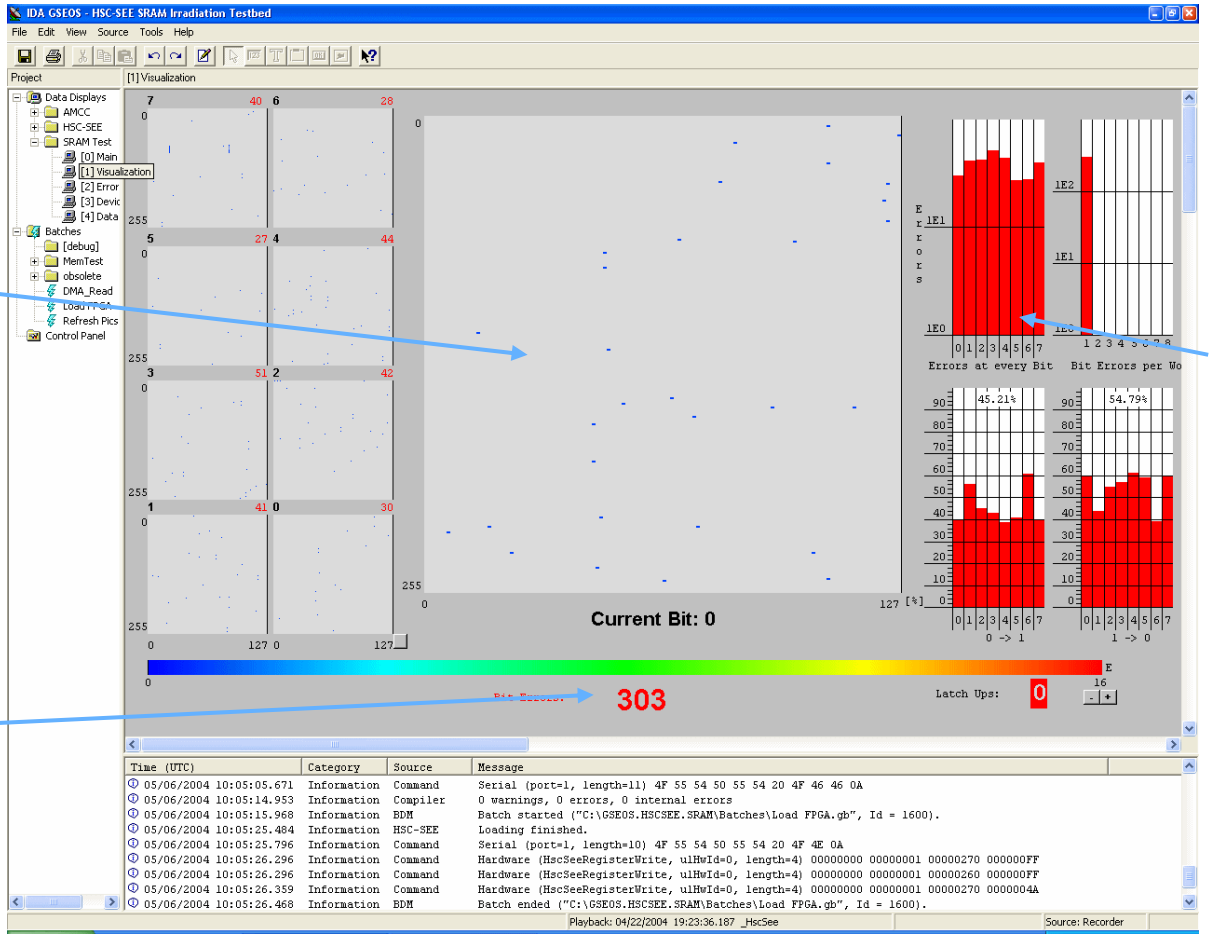
# 2. SEE-Test Verification

- Test Facility: HIF at UCL, low penetration beam M/Q ~ 5, LET 2.97…111.8 MeV/mg/cm²
- Devices: SRAM, 6DUTs:
  (Atmel AT60142-E, MHS MMDP65656EV-45, MMDP65656FV-55, White WMS512K8-70DEM, WMS512K8-45DEM)
- Test-Bed:
  - Autonomous in-situ tests of all single DUTs
  - Complete recording of anomaly events, i.e. data errors, device failures and latch-up's
  - Real time visualization of all data
  - Autonomous H/W supported fast latch-up protection (<5µsec)

# 2. SEE-Test Verification

**Error Distribution**

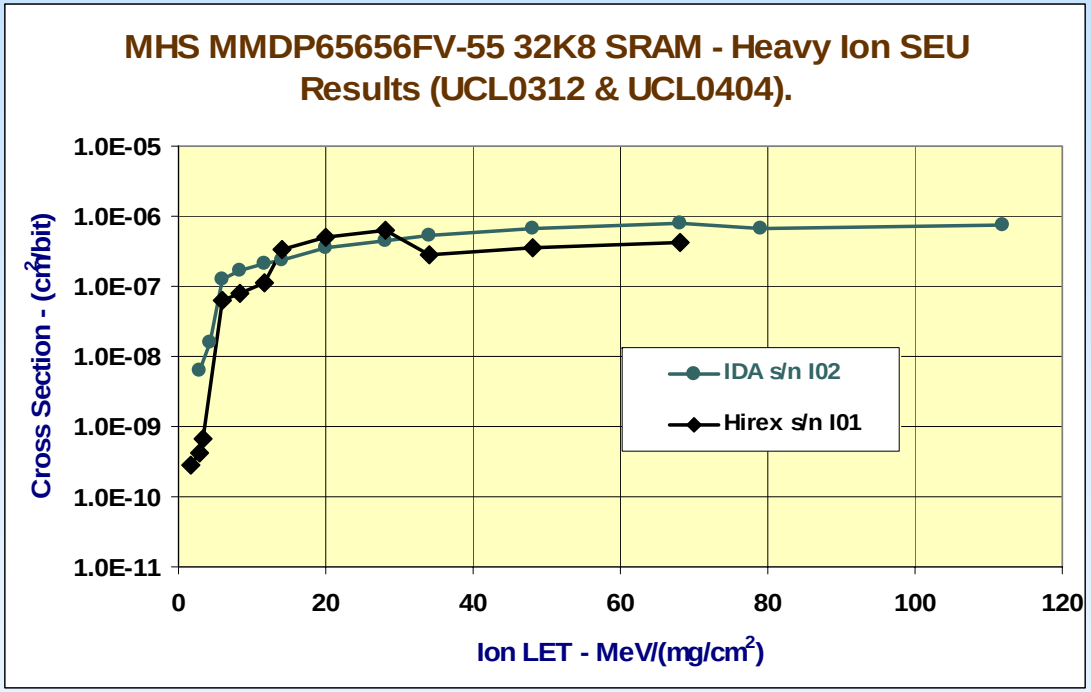
**Error Counter**




**Error Statistics**

# 2. SEE-Test Verification

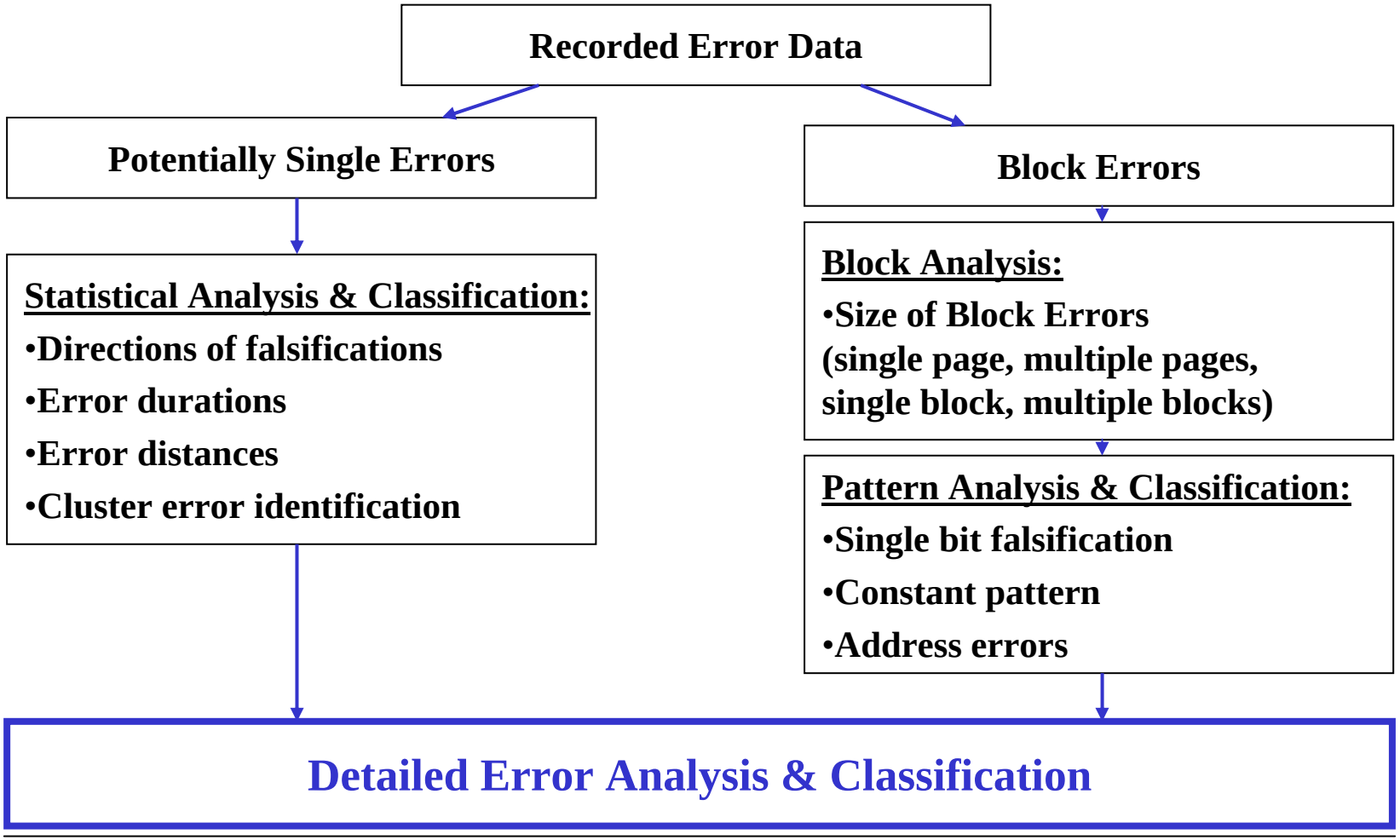
- RTMC-3 SEE-Test results are well compliant with previous measurements:



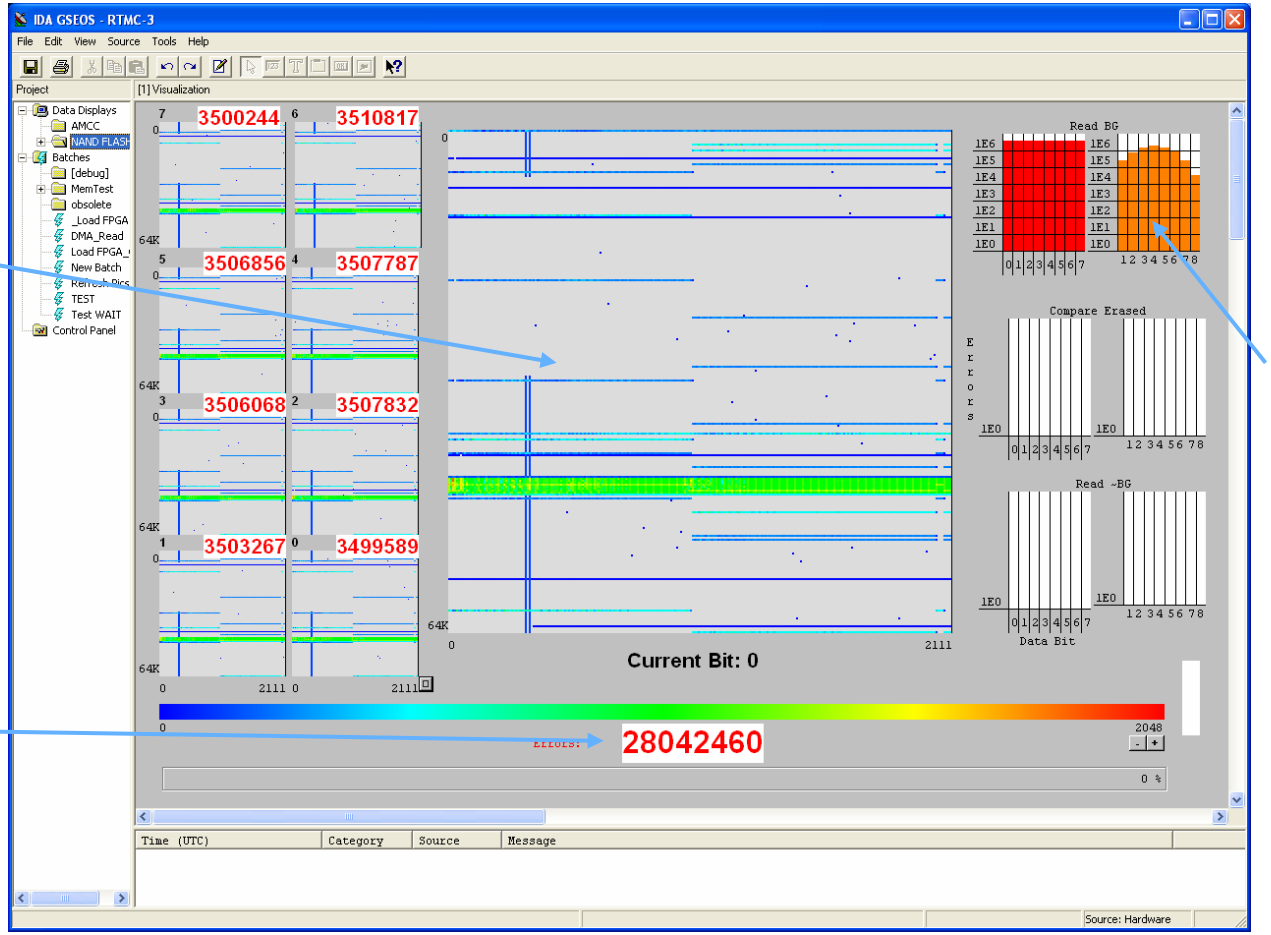
# 3. SEE-Test Evaluation Capabilities

- Quick-Look data analysis during test
  - Error counts
  - Visualization of error distribution (statistically, physically/logical)
- Detailed data analysis after test
  - Replay of error event data (real-time, single step, time scaled)
  - User definable data filtering for error analysis and classification after test

# 3. SEE-Test Evaluation



# 3. SEE-Test Evaluation Quick-Look




**Error Distribution**

**Error Counter**

**Error Statistics**

# 4. Conclusions

- RTMC-3 is verified and available for SEE- and TID-testing
- Feasibility for “state of the art” memory device tests and evaluation support demonstrated
- Further tests of complex devices (SDRAM, system on chip devices) in preparation