

High-Energy Proton Damage Assessment of 90 nm Node Multiple Gate Oxide Thickness Transistors

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Goal of the work

Introduction: multiple gate oxides for System-on-Chip

Experimental: devices and irradiation conditions

Results and discussion: linear I_S, I_D, I_B and I_G

Conclusions



□To study potential degradation mechanism by ionizing irradiation. Total Ionizing Dose (TID) degradation may result from e-h pair generation in the gate and isolation dielectrics.

□Part of the particle energy is dissipated in atomic displacements, generating defects in the silicon substrate. Do we see some effects on the device behavior?

□Is there any difference in the degradation behaviour of thin oxides grown on F or N implanted silicon?

Introduction

•System-on-Chip applications require transistors with different functionality.

- Logic and high-speed \rightarrow maximum performance (thin oxide)
- Low power/low voltage (analog; RF) → thicker gate oxide
- I/O electronics: high power \rightarrow thick oxide

Several approaches are under development:

- Oxidation and etch-back
- Local implantation of N or F (I/I) in the substrate
- N gives rise to a retardation of the oxidation rate
- F gives rise to an enhancement of the oxidation rate

•The use of multiple thickness gate oxides may give rise to a total-dose issue.



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□ <u>Wafer 4:</u> The high-performance (HP) devices have been fabricated using Shallow Trench Isolation (STI) and a 1.5 nm Rapid Thermal Oxidation (RTO) gate dielectric, with nominal length 1.5 nm. A polysilicon gate was used and dopant activation was achieved by a 1100 °C, 1 s spike anneal.

□<u>Wafer 6</u>: 2 nm RTO gate oxide (low-power/low voltage reference).

□<u>Wafer 8</u>: 8 keV F implantation at 5x10¹⁴ cm⁻² dose in the active regions, followed by a 1.5 nm RTO oxide. This should result in a thicker oxide due to SiO₂ swelling and enhanced oxidation rate by the presence of fluorine.

□<u>Wafer 10</u>: 8 keV N implantation at 3x10¹⁵ cm⁻² dose in the active regions, followed by a 2 nm RTO. This should result in a thinner oxide (< 2 nm), due to a retarded oxidation rate.



From the accumulation capacitance of a high-frequency C-V measurement on a large-area (100 μ mx100 μ m) MOS capacitor, the following effective oxide thickness (in nm) have been derived: <u>no F I/I no N I/I</u>

RTO 1.5 nm: 1.7 2.3 -- --

RTO 2 nm: -- 2.2 1.94



Proton Energy: 67 MeV; Fluence: 3x10¹² cm⁻² Bias: +1.2 V on n-type gates; 0 V on other terminals





The width of the MOSFETs is fixed at 10 μ m. Both long (L) and short (S) arrays have been studied:

Long array (L): 0.35 $\mu m,$ 0.5 $\mu m,$ 1 $\mu m,$ 3 $\mu m,$ 10 μm Short array (S): 0.07 $\mu m,$ 0.08 $\mu m,$ 0.09 $\mu m,$ 0.10 $\mu m,$ 0.11 $\mu m.$

input: from -1.2 to 1.2 V (n-) or +1.2 to -1.2 V (p-MOSFET) at $|V_{DS}|=0.025$ and 1.2 V (supply voltage). output: $|V_{DS}|$ from 0 to 1.2 V and $|V_{GS}|$ from 0.2 to 1.2 V (step 0.2 V)



Biased irr.; chip M4L5 – L=10 μ m











Most long devices did not survive and showed excessive gate leakage current

□Short devices showed less dramatic degradation: mainly the gate leakage current and subthreshold S/D leakage increased

□No strong changes found in the normal static device characteristics

 Electrical stress measurements of long devices did not exhibit any degradation of the gate current
Is there a synergistic effect between I_G and the proton irradiation (current)?

Unbiased irradiations: input characteristics





Unbiased irradiations: output characteristics





Unbiased irradiations: output characteristics







 $\blacksquare Unbiased$ irradiations showed less pronounced increases in $I_{\rm G}.$

■An unusual change in the characteristics at large V_{DS} was found, which was reflected in the output characteristics.

Little changes were found in the normal linear characteristics.

It appears that the reference wafer 4 (and 6) short devices exhibit this degradation more than wafer 8 (F I/I).



 Biased irradiations have been performed on 6 packaged devices. Some of the n-MOSFETs of the same array (separate gate and drain contacts) had a gate at 0 V (no gate current flowing), others were at +1.2 V.

•Fluence was at 3x10¹² 60 MeV p/cm².

 In addition, a number of non-packaged chips were exposed as well (contacts floating).



For 0 V on the gate: no degradation whatsoever







For 0 V on the gate: no degradation whatsoever





For 1.2 V on the gate: most devices exhibit a marked degradation





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For 1.2 V on the gate: most devices exhibit a marked degradation; the gate is a resistor.



Results Round 2







Some n-channel devices break down at the gatedrain junction.



Results Round 2









Results Round 2

Statistics: 2 out of 9 biased short-channel transistors were not degraded. None of the 0 V biased devices were degraded in round 2.









oThere appears to be a bias dependence of the radiation response of 90 nm (n-)MOSFETs. Particularly large-area transistors are broken after a high fluence of $3x10^{12}$ p/cm².

oStatistics (microdosimetry) also plays an important role: some of the biased transistors survive the irradiation without any degradation.

•The observations are tentatively interpreted in terms of a synergy between gate current flow and high-energy proton irradiation. Created defects (or latent defects) may give rise to a catastrophic failure of the gate by forming a preferential path for gate current flow.