

Heavy Ion Single Event Latch-up Test for the RAL CDS/ADC CCD Video Processing ASIC Mk6.

by

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Abstract

This presentation summarises the results of a heavy ion SEL test program carried out on the Mk6 version of the Rutherford Appleton Laboratory 16-bit correlated double sampling ADC ASIC at a 1 MHz sample rate. This ASIC was manufactured with a 0.35 μm 'opto' process on 20 μm epitaxial layer silicon, at the Austria Micro Systems (AMS) fab.



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Mk6 ASIC – Device Information I.

Designer: Rutherford Appleton Laboratory (RAL), UK.
Die manufacturer: Austria Micro System (AMS)
Process: 0.35 μm 'opto' process on 20 μm epitaxial
Package facility: Austin Semiconductor
Package: 84-pin CQFP
Date code: None
Die marking: CDS ADC v.6
Die dimensions: 6.75 x 6.75 mm approx.

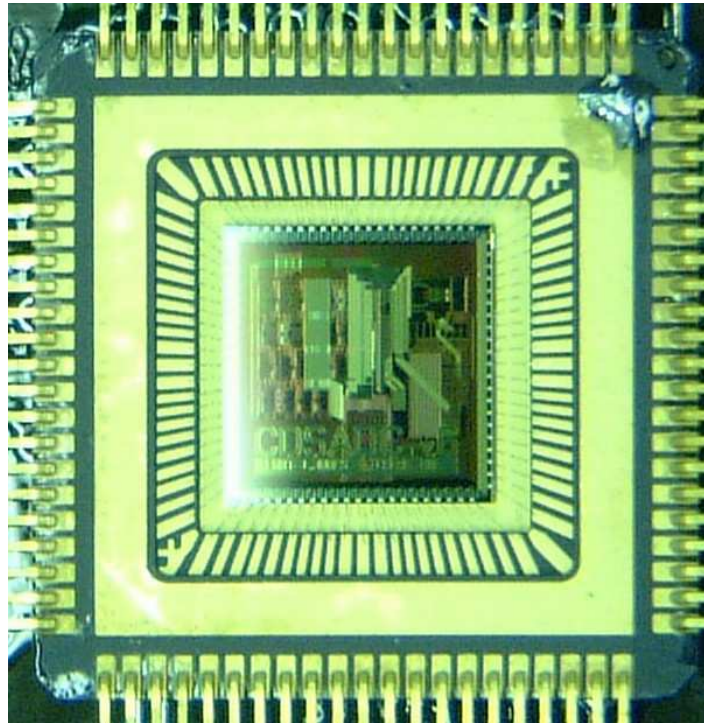


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Mk6 ASIC – Device Information II.



84-pin CQFP with lid removed showing ASIC die and bond wires



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Mk6 ASIC – Test Board I.

- # The devices were clocked at 1 MHz with signals generated by an ACTEL proASIC FPGA.
- # The waveform timings were identical to the normal CCD signal digitising mode.
- # A representative analogue CCD signal was also generated as an alternating pixel of approximately 5% and 95% of full-scale video amplitude.
- # The most significant bit was monitored as a check for functional failure.
- # The ADC input offset was set to 0 and the programmable gain amplifier (PGA) gain to 1.



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Mk6 ASIC – Test Board II.

- # The test boards also included on-board power supply conditioning and control circuitry.
- # Each ASIC had a dedicated +3.3V analogue supply with fold-back current limit set at 235 mA.
- # The ASIC power conditioning included a current monitor output and reset input.
- # The ACTEL FPGA was powered from a separate external bench supply.



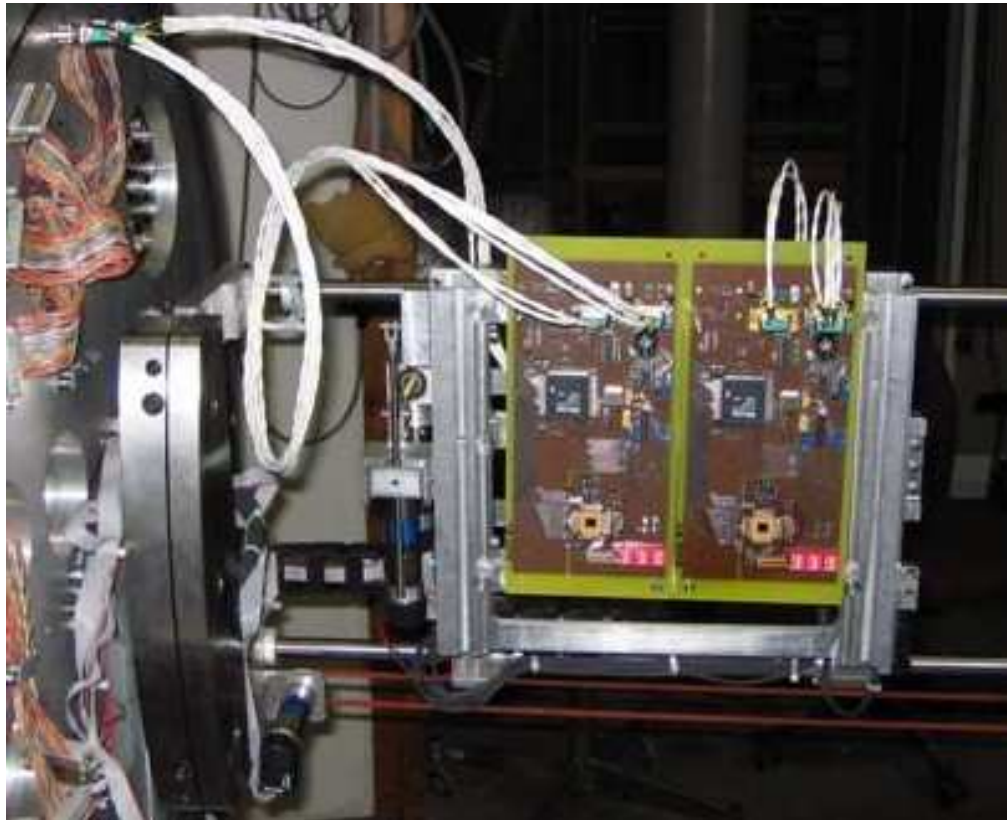
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Mk6 ASIC – Test Board III.

Test boards prior to closure of the HIF test chamber.



The CDS/ADC ASICs are positioned, with lids removed,
at the bottom of the boards.

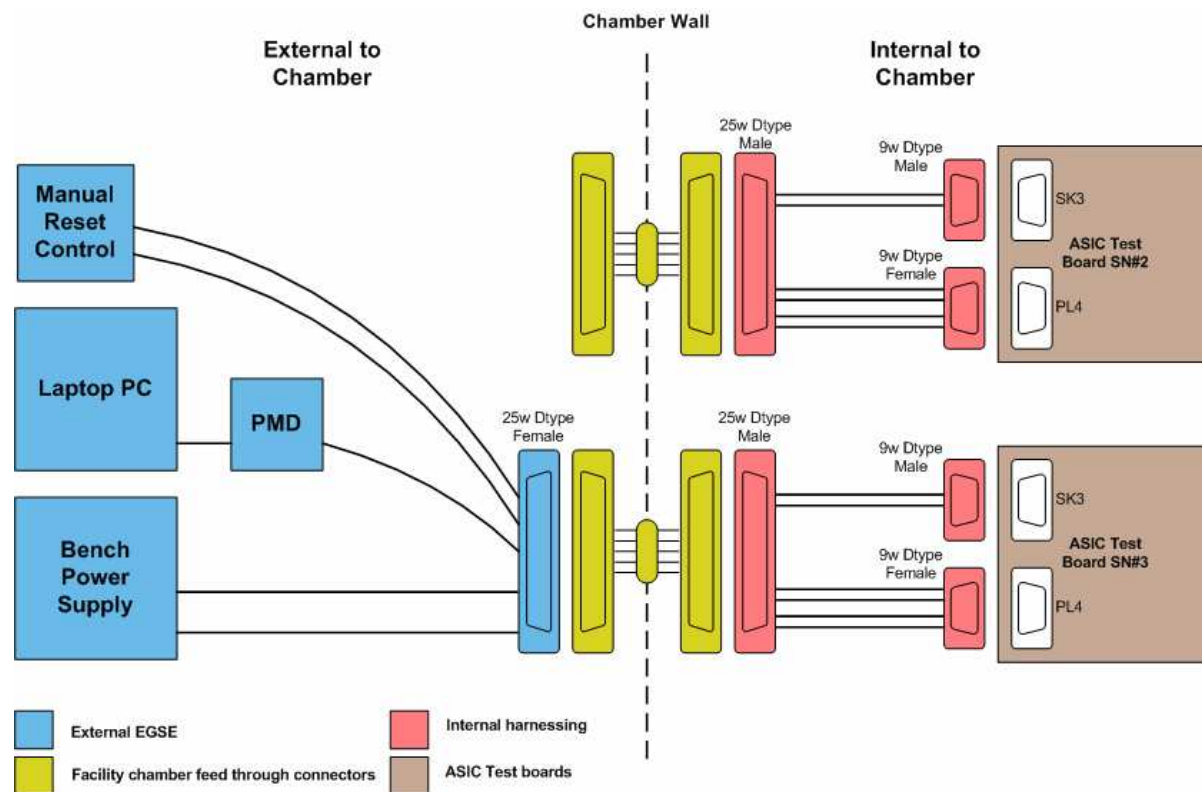


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Mk6 ASIC – Test Board IV.



ASIC test configuration

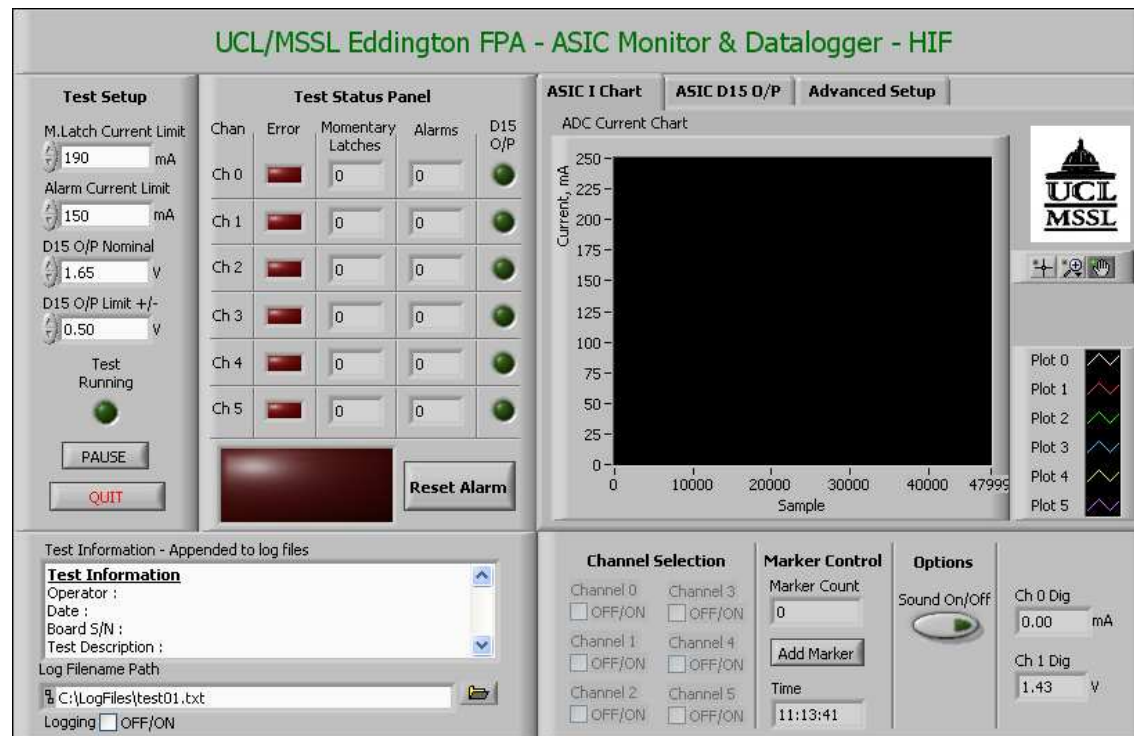


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Mk6 ASIC – Test Board V.



Screen shot of ASIC monitor & data logger



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Mk6 ASIC – Heavy Ion Test Facility I.

Heavy ion tests were performed at the CYClotron of LOuvain la NEuve (CYCLONE), Belgium using Ne^{4+} , Ar^{8+} and Kr^{17+} ions at the Heavy Ion Facility (HIF).

Ion Cocktail M/Q=4.94	Energy MeV	Range $\mu\text{m Si}$	LET MeV(mg/cm²)
$^{20}\text{Ne}^{4+}$	78	45	5.85
$^{40}\text{Ar}^{8+}$	150	42	14.1
$^{84}\text{Kr}^{17+}$	316	43	34.0
UCL – Ion Cocktail #1 produced for ESA			



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Mk6 ASIC – Heavy Ion Test Results I.

Start Time	Run No.	DUT Board	s/n	Ion-Tilt	LET-MeV (mg/cm ²)	Flux p/s/cm ²	Fluence p/cm ²	Dose rad(Si)	Time sec.	Results SEL
04:55	1	Board 2	2	Ne-0	5.85	5.00E+03	1.00E+06	94	237	0
05:00	2	Board 2	2	Ne-45	8.27	3.50E+03	1.00E+06	132	296	0
05:06	3	Board 2	2	Ne-60	11.70	2.50E+03	1.00E+06	187	416	0
05:32	4	Board 2	2	Kr-0	34.00	1.00E+03	6.00E+05	328	323	85
05:45	5	Board 2	2	Ar-0	14.10	5.00E+03	1.00E+06	226	203	0
05:50	6	Board 2	2	Ar-45	19.90	3.50E+03	1.00E+06	320	294	16
05:55	7	Board 2	2	Ar-60	28.20	2.50E+03	1.00E+06	452	399	74
06:04	8	Board 2	2	Ar-35	17.20	4.00E+03	1.00E+06	276	253	6
06:09	9	Board 2	2	Ar-30	16.30	4.00E+03	1.00E+06	261	253	4
06:14	10	Board 2	2	Ar-25	15.60	4.00E+03	1.00E+06	250	215	4
06:19	11	Board 2	2	Ar-20	15.00	4.50E+03	1.00E+06	240	228	0
06:25	12	Board 3	3	Ar-0	14.10	5.00E+03	1.00E+06	226	200	1
06:30	13	Board 3	3	Ar-45	19.90	3.50E+03	1.00E+06	320	309	16
06:37	14	Board 3	3	Ar-60	28.20	2.50E+03	1.00E+06	452	386	63
06:48	15	Board 3	3	Ar-25	15.60	4.00E+03	1.00E+06	250	266	3

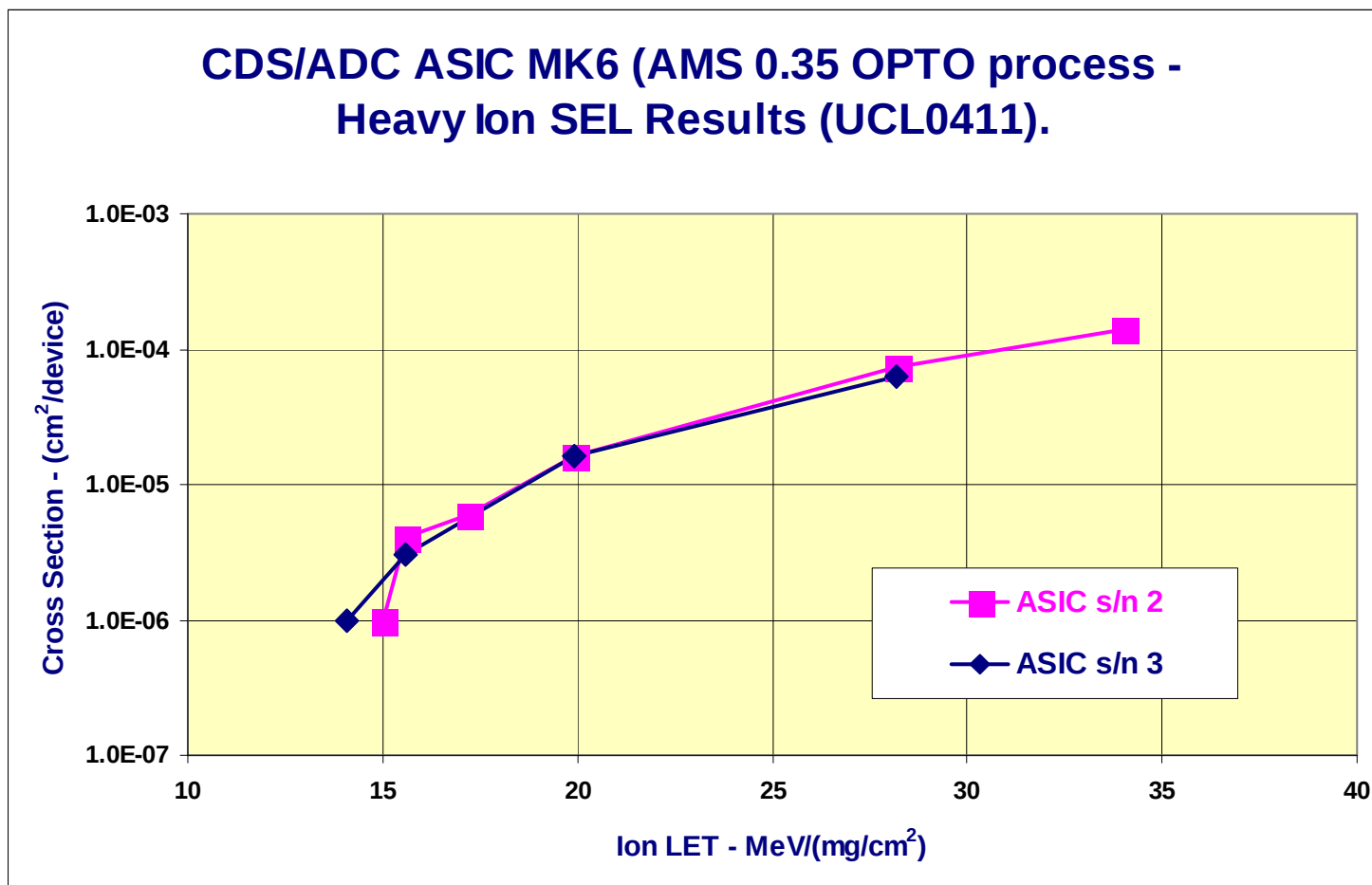


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Mk6 ASIC – Heavy Ion Test Results II.



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Mk6 ASIC – Conclusion I.

- # Two Mk6 CDS/ADC CCD Video Processing ASIC devices were heavy ion SEL tested at the HIF on 9th November 2004.
- # Both devices tested showed identical latch-up behavior with a SEL LET threshold around 14 MeV/(mg/cm²).
- # The devices were manufactured with a 0.35 μ m ‘opto’ process on 20 μ m epitaxial layer silicon, from Austria Micro Systems (AMS).



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