# Radiation SEE Evaluation of High Capacity Flash Memory Devices for Safeguard Data Recorder

First Results

Progress Presentation of ESTEC Contract No. 17442/03/NL/JA


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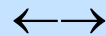
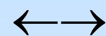
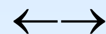
University of Jyväskylä, Jyväskylä, Finland

# Some Introductory Remarks

1. Principal SEE Response of Memory Devices
2. Application Dependent Error Assessment
3. Flash Error Types and Related Design Drivers

# Principal SEE Response of Memory Devices

| **SRAM** | **SDRAM** | **Flash NVRAM** |
|---|---|---|
| *Access typically to:*<br>Single Words |  | Strings of e.g. 2k Words |
| *Control of Memory Cell Access:*<br>Direct,<br>no device internal<br>state machine for control<br>of sequential actions |  | Indirect,<br>device internal<br>state machine controls<br>numerous sequential actions |
| | | |
| *Dominant Error Species:*<br>Random Single Bit Errors |  | SEFIs<br>Disturbances of the state machine affect kwords,<br>many Lock Ups of the state machine are resolvable by power cycling only |

# Application Dependent Error Assessment

| **SRAM** | **SDRAM** | **Flash NVRAM** |
|---|---|---|
| *Typically used for:* | | |
| Main Memories | ← → | Background Memories,<br>Disk Replacement |
| *Access Timing:* | | |
| Hard Real Time | ← → | Access Delays of ms ... s are tolerable |
| *In case of Power Cycling for Lock Up Removal:* | | |
| n.a | Complete<br>Data Loss | Stored Data are<br>not impaired |

⇒ **Assessment of Error Implications is strongly Application Dependent and requires detailed knowledge of Error Types and of Error Type Specific Cross Sections**

⇒ **In-depth Radiation SEE Tests mandatory for Device Characterisation**

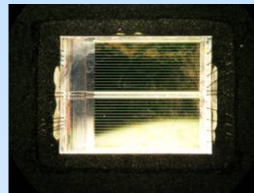
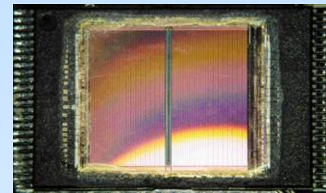
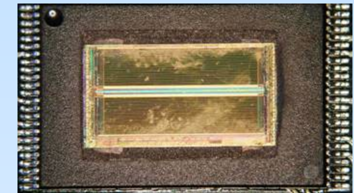
# Facility

- UCL, Belgium
- Ions used:

| Ion | Energy [MeV] | Tilt Angle | Range [µm] | LET [MeV/mg/cm²) |
|---|---|---|---|---|
| $^{22}Ne^{7+}$ | 235 | 0°, 45 | 199, 141 | 3.3, 4.67 |
| $^{28}Si^{8+}$ | 236 | 0° | 106 | 6.8 |
| $^{40}Ar^{12+}$ | 372 | 0°, 45°, 54°, 60° | 119, 84, 70, 60 | 10.1, 14.3, 17.2, 20.2 |
| $^{58}Ni^{17+}$ | 500 | 0°, 35° | 85, 70 | 20.6, 25.1 |

# Devices

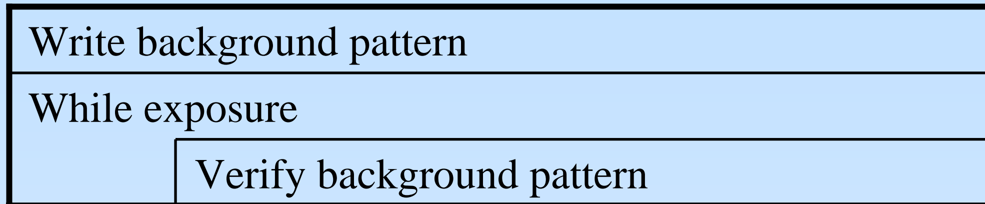
- Front opened by etching
  - Toshiba 1Gbit, Toshiba 256Mbit, Samsung 1Gbit, ST 1Gbit

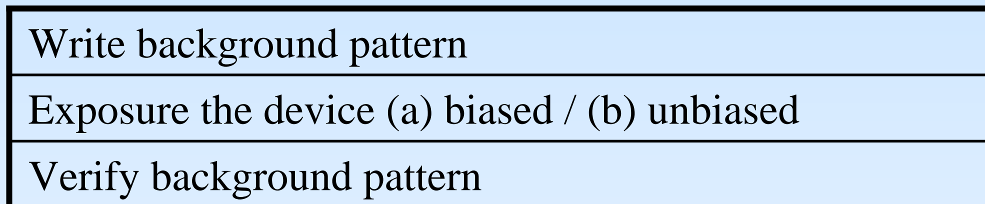
- Backside opened by precision grinding
  - Samsung 1Gbit, thickness 70 µm

# Test Modes

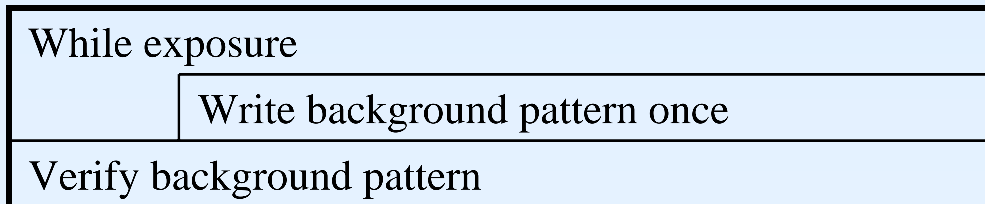
- Test Mode M2 (Read only under Irradiation)



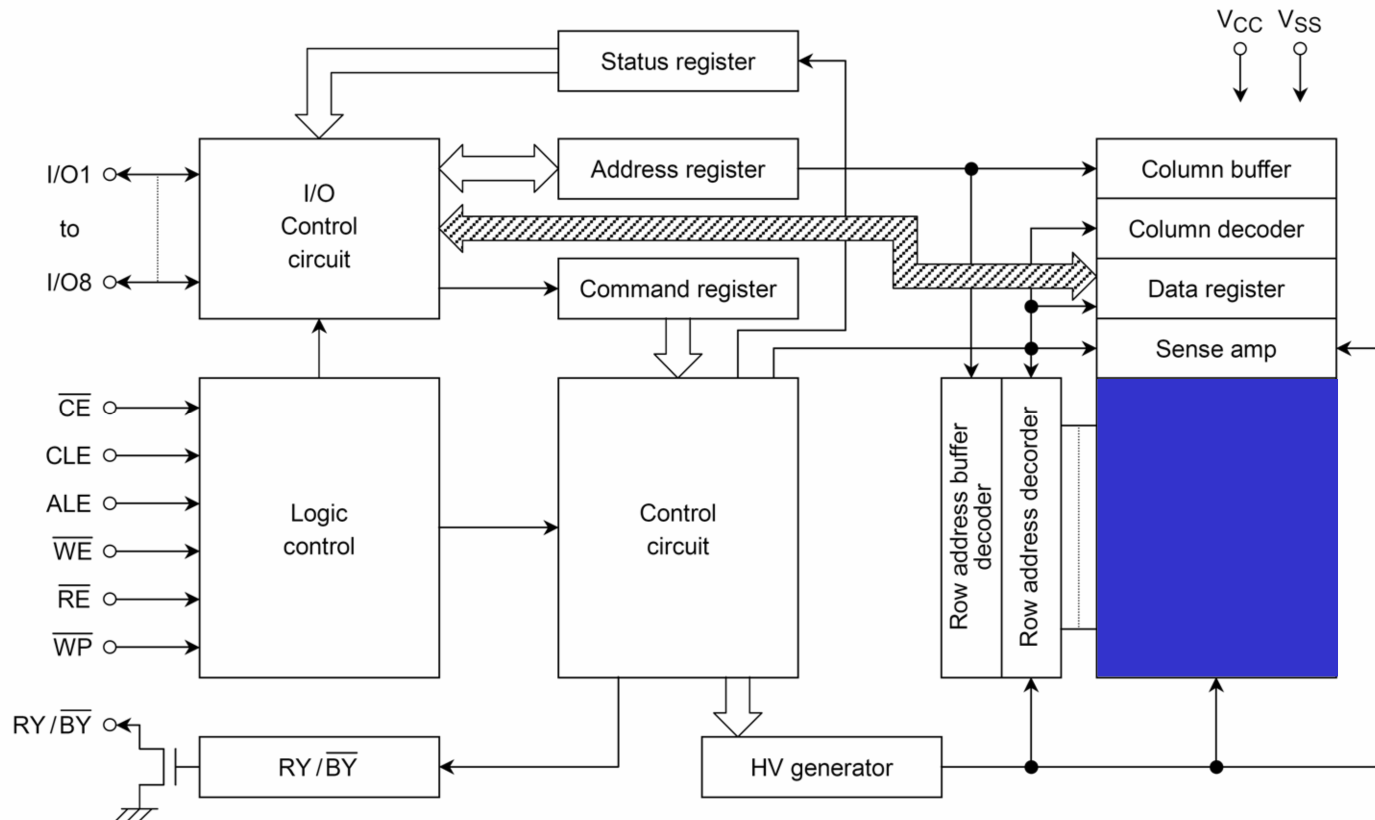

- Test Mode M3 (Storage test)




- Test Mode M4 (Write only under Irradiation)



# Flash Block Diagram




(Toshiba TC58NVG0S3AFT05)

# NAND-Flash Operation

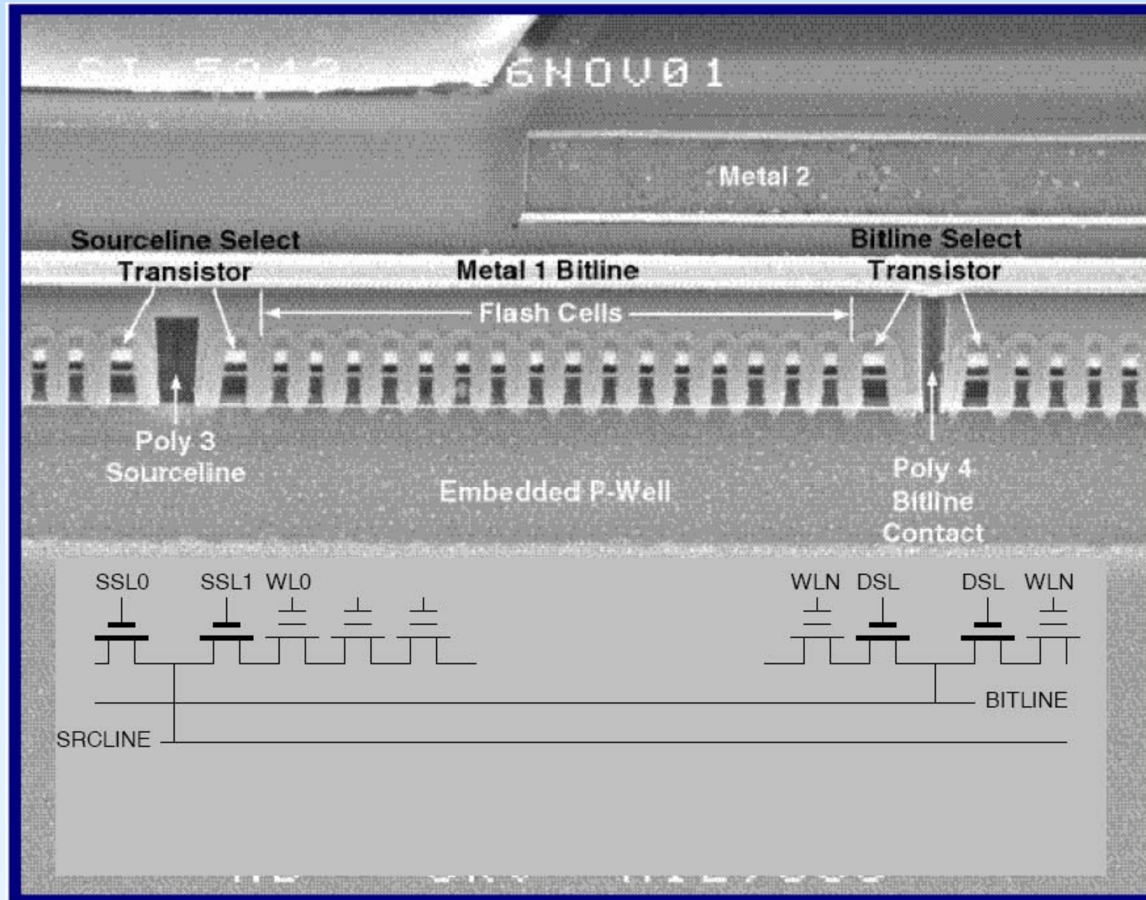
Storage Principle:

Charge transfer to Floating Gate by Fowler-Nordheim Tunneling

Charge controls Threshold Voltage of MOS-Transistor

| | | |
|---|---|---|
| Device Organization: | | e.g. 1 k blocks of 64 pages, each |
| Blockwise Erase: | ⇒ "1" | e.g. 64 x 2 k bytes at once |
| Pagewise Write: | "1" ⇒ "0" | e.g. 2 k byte at once |
| Pagewise Read: | | Nondestructive, 2 k byte at once |

# NAND-Flash Buildup



# Error Classification

## Error Types

(a) Originating from the cells

(b) Originating from the data path / (cell)

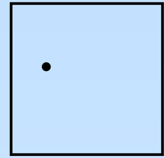
(c) Originating from the control circuitry

- (c1) Transient
- (c2) Permanent, non destructive
- (c3) Destructive

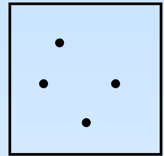
} SEFIs

# Error Types and Remedies I

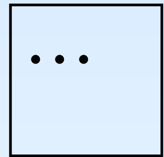
(a) MCE: Memory Cell Error
"Stuck Bits" – changes cell content?
Remedy: Error Correction, Scrubbing, if not Hard MCE



(b) SEU: Single Event Upset
Single Bit Errors
Remedy: Error Correction



(c1) CBE: Cluster Bit Error
Clusters of Single Bit Errors in a row,
mostly spaced equally
e. g. ≈ 20 % of SEU rate
Remedy: Error Correction with Symbol Scrambling



# Error Types and Remedies II

(c1) **VE: Vertical Error**

Bit Errors at the same position distributed over many pages

Remedy: Error Correction

64

(c1) **PE: Page Error**

Complete Page Readout falsified

Remedy: Detection and read again → Access Delay

2k

(c1) **BE: Block Error**

Complete Block Readout falsified

Remedy: Detection and read again → Access Delay

2k

64

# Error Types and Remedies III

(c2) B.SEFI

"Stuck Block" – Functional interrupt at one block

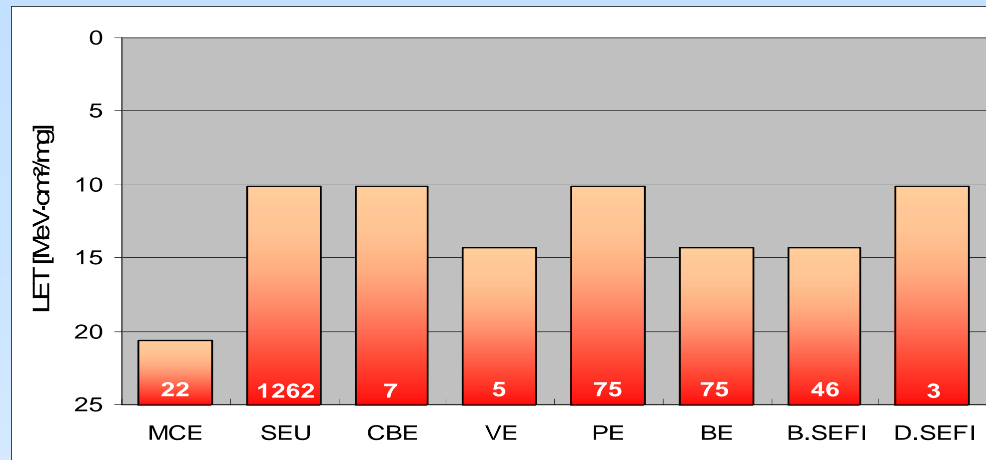
Remedy: Detection, power cycle and read again → Access Delay

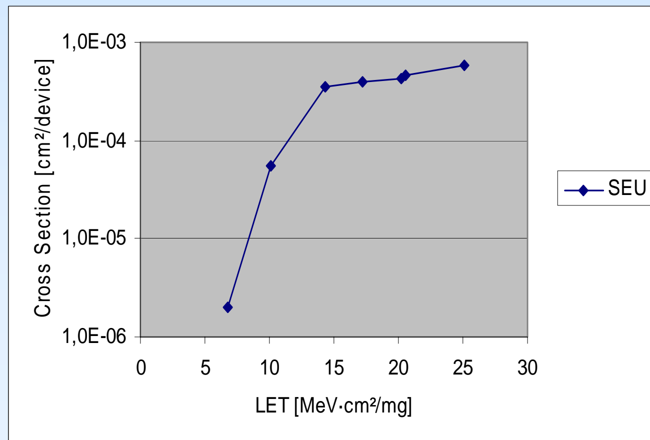
(c2) D.SEFI

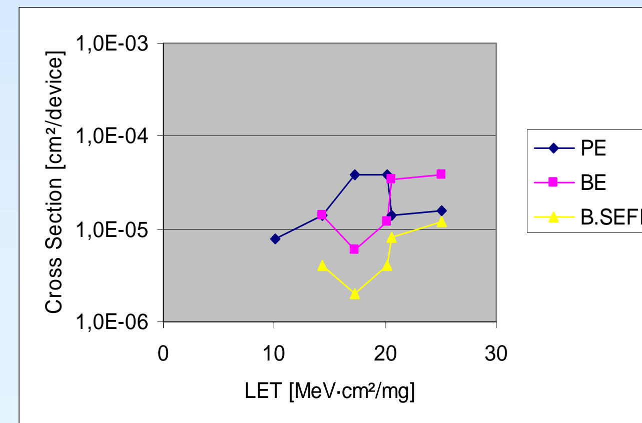
No device response

Remedy: Detection, power cycle and read again → Access Delay

# Findings for the Toshiba 1 Gbit

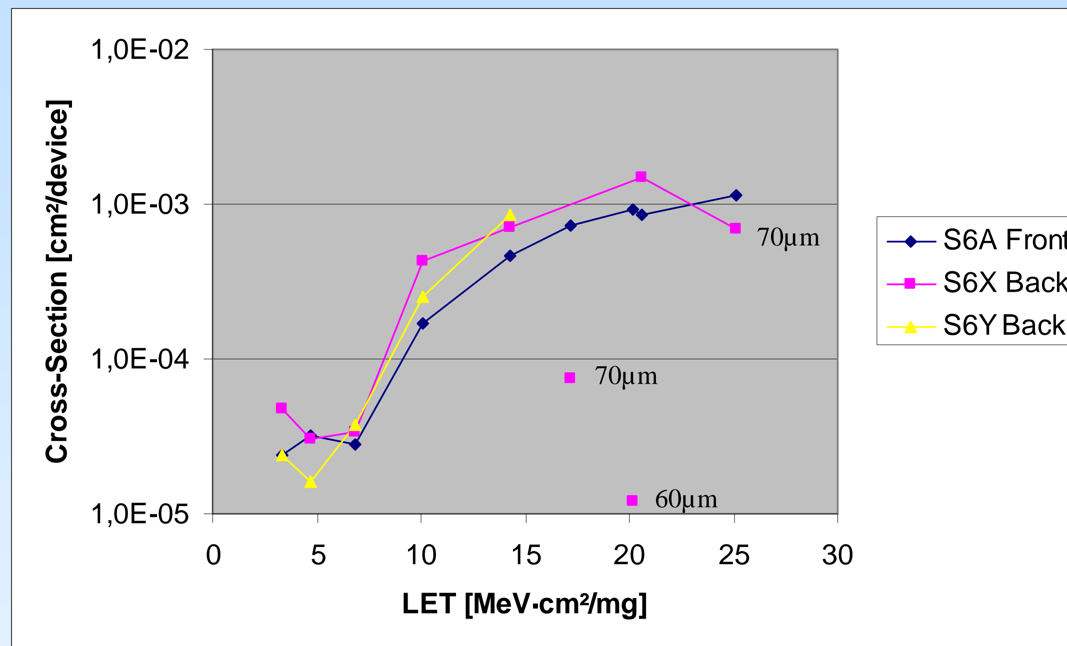


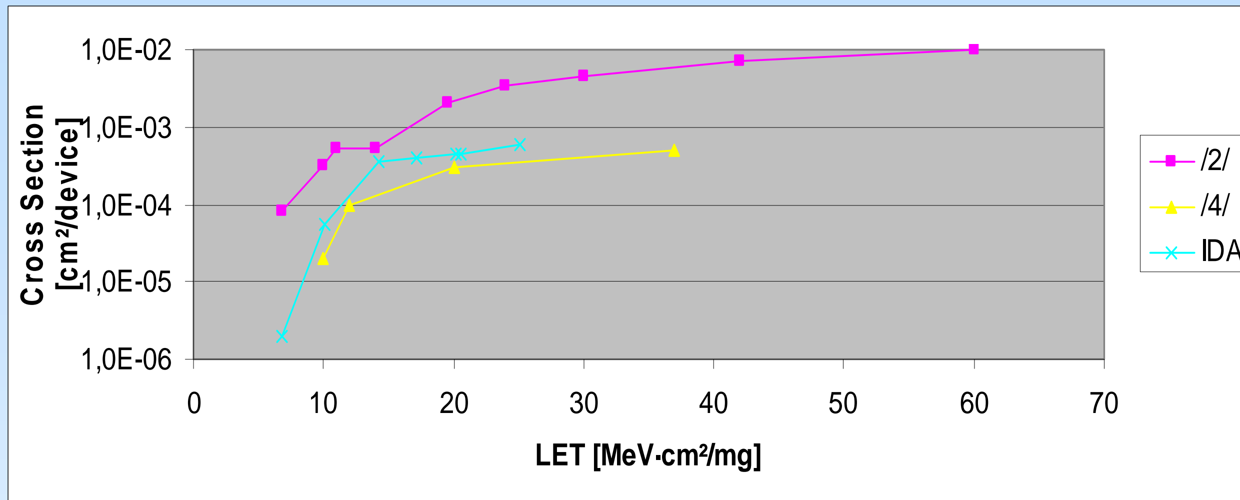
# Frontside / Backside Irradiation

- Device Type: Samsung 1 GBit K9F1GU0M




⇒ as far as the range limitation (70µm) is met
both opening techniques show comparable results

# Comparison to SEU Test Results of Similar 1 G Bit Devices




/2/ D. N. Nguyen, L. Z. Scheick, IEEE NSRC Workshop Record, 18 – 28, 2003, (JPL)
TC58100FT DC02/40 1 Gbit NAND FLASH

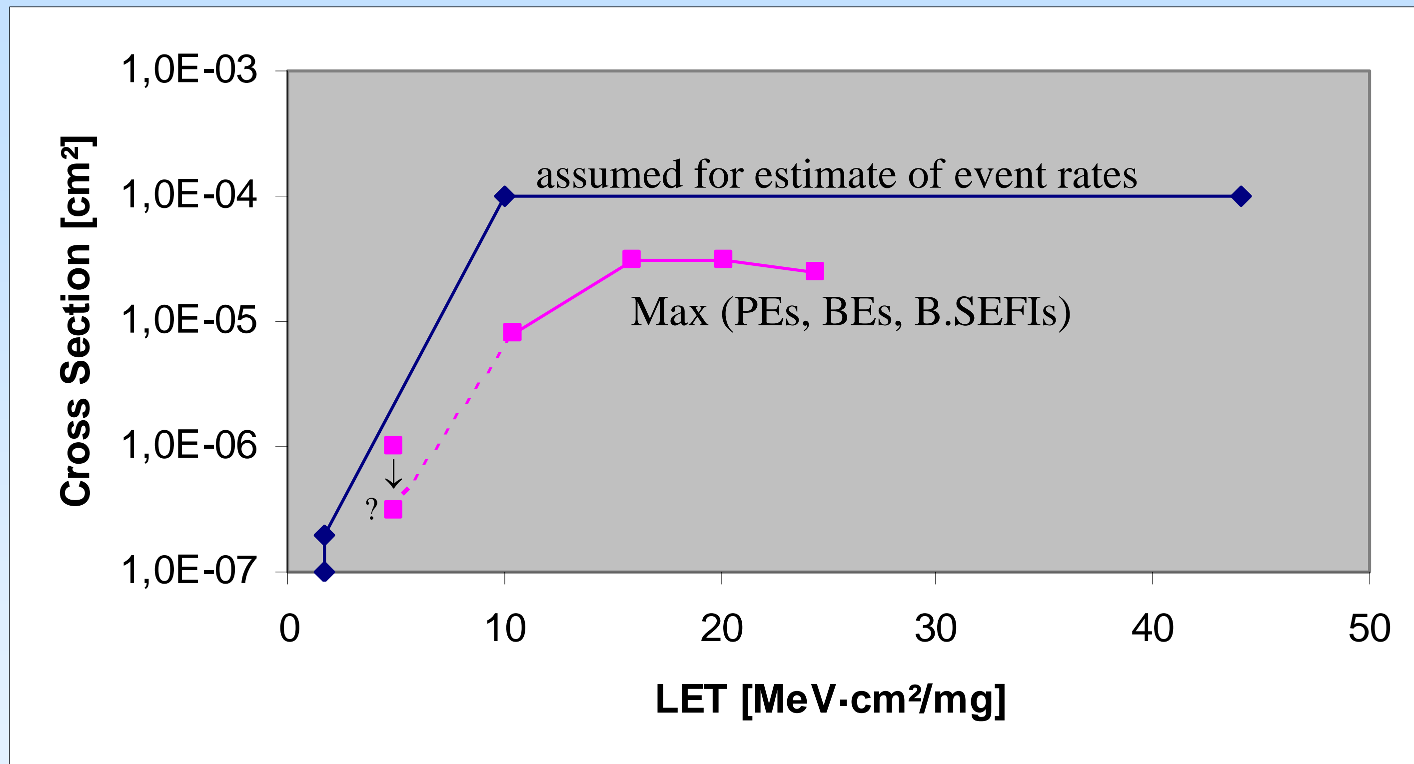
/4/ T. E. Langley, P. Murray, IEEE NSREC, Atlanta, 2004, (JPL, SEAKR)
TC58 DVG02A1 1 Gbit NAND FLASH,

Differences due to:

a) Differentiation between Single Errors and Bulk Errors,
/2/ includes all bulk errors

b) Different development stages of the Toshiba 1 Gbit device

# Frequency of Access Delays



# Frequency of Access Delays

Deep Space 1 AU, no shielding

<u>GCR background:</u> 8.70 E-4 (PEs, BEs, B.SEFIs) /d/dev

4 Gbit net = 6 devices → 5.25 E-3 (PEs, BEs, B.SEFIs) /d

≈ 2 (PEs, BEs, B.SEFIs) /y of operational time

<u>Solar Flare:</u> 5.50 E-2 (PEs, BEs, B.SEFIs) /d/dev

4 Gbit net = 6 devices → 3.30 E-1 (PEs, BEs, B.SEFIs) /d

≈ 1 (PEs, BEs, B.SEFIs) /3.3 Flare Days of operational time

Device SEFIs: ≈ 3 per 5 years of operational time

1 per 30 Flare Days of operational time