

Summary and results of recent proton testing carried out on COTS components for the LHC

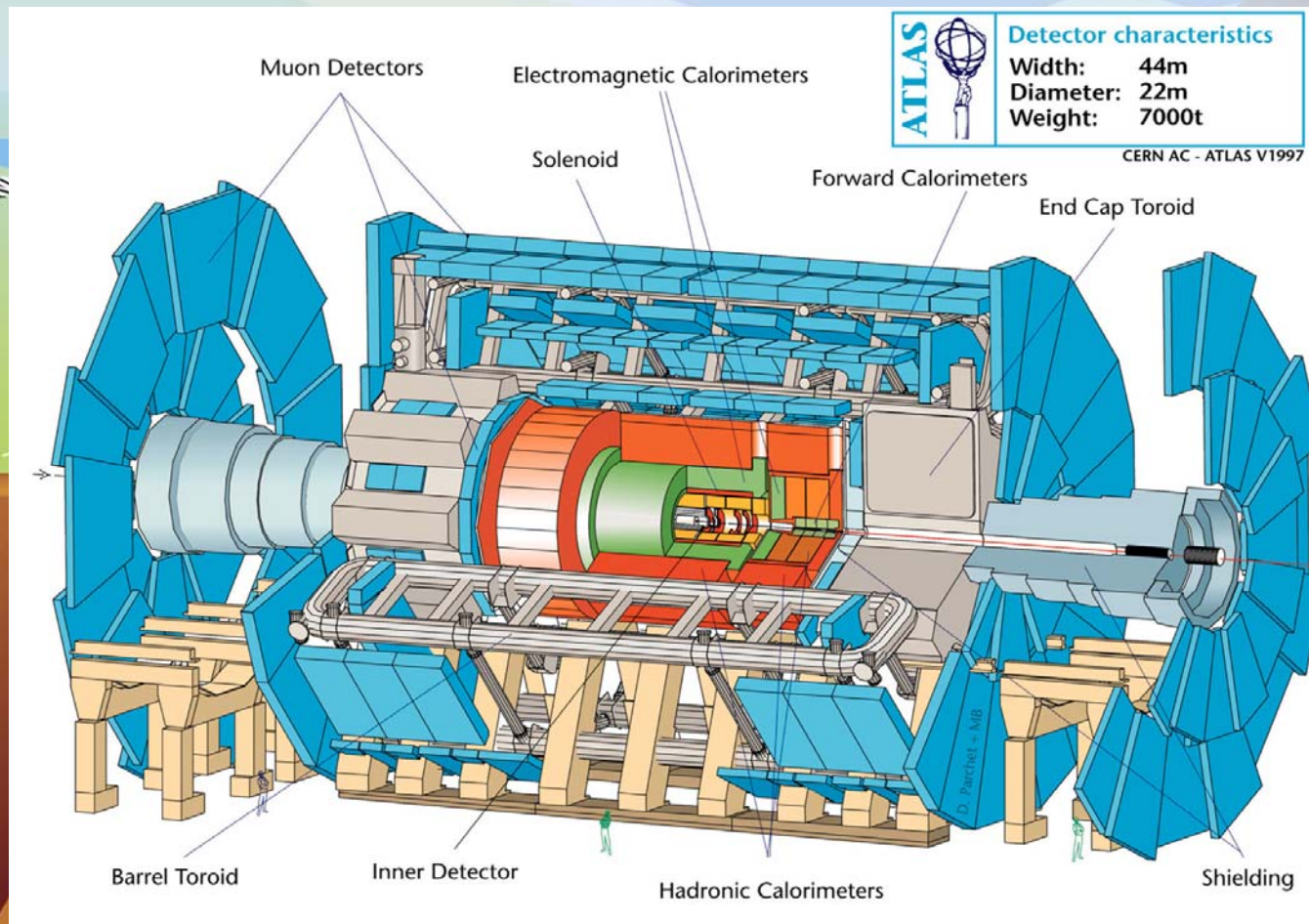
F.Faccio, T.Wijnands, F.Anghinolfi
CERN

Outline

- The LHC
 - Radiation levels and organization in the experiments
 - Radiation levels and organization in the LHC machine
- The use of proton beams for testing
 - Why 60-200MeV protons
 - How to estimate error rates in LHC
- Examples of recent testing
- Conclusion



Overall view of the LHC experiments.



ALICE
Point 2



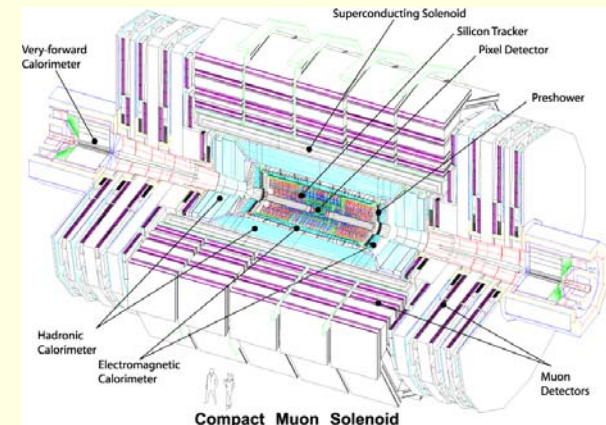
ESA QCA 200
Jyväskylä, 25 May 2000

LHC Machine and LHC experiments

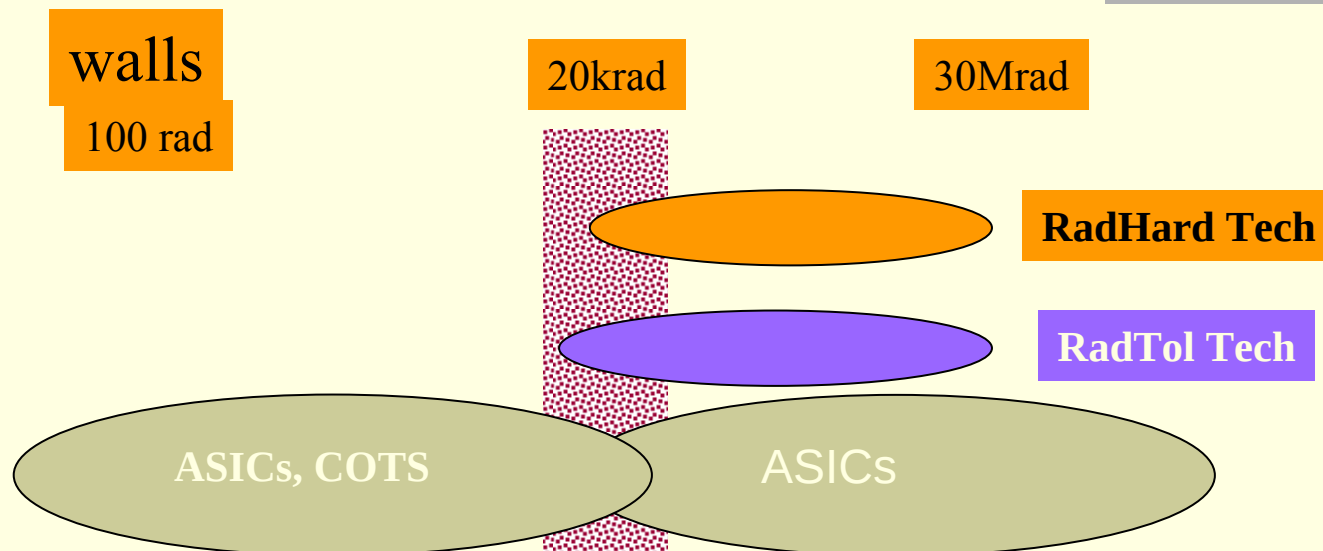
- 2 different worlds:
 - Machine (accelerator) is full responsibility of CERN, and it is built fully with CERN resources – personnel and funds
 - Experiments are large collaborations involving hundreds of Institutes/Universities worldwide. Very large and complex coordination effort is required, since experiments are built mainly with resources from outside CERN – personnel and funds

Radiation environment in the experiments

		Most exposed	Cavern Walls
TID (rad)	Alice	250K	0
	Atlas	26M	100-200
	CMS	82M	200
	LHCb	7M	200
1-MeV equivalent neutron fluence (n/cm²)	Alice	3.0×10^{12}	6.5×10^6
	Atlas	1.6×10^{15}	5.0×10^{10}
	CMS	2.5×10^{15}	5.1×10^{10}
	LHCb	9.0×10^{13}	1.5×10^{11}
Hadrons fluence (p/cm²), E>20MeV	Alice	1.3×10^{12}	8.7×10^6
	Atlas	2.3×10^{15}	1.0×10^{10}
	CMS	2.5×10^{15}	1.8×10^{10}
	LHCb	1.4×10^{14}	$< 4.3 \times 10^9$



Radiation and Technologies



RadHard Tech

Radiation Hardened by technology (Ex: DMILL)

RadTol Tech

Radiation Hardened by design, Commercial technology (Ex: 0.25 microns with radtol layout techniques)

Experiments are big collaborations



CMS Collaboration



36 Nations, 160 Institutions, 2008 Scientists and Engineers (November 2003)

TRIGGER & DATA ACQUISITION

Austria, CERN, Finland, France, Greece, Hungary, Italy, Korea, Poland, Portugal, Switzerland, UK, USA

TRACKER

Austria, Belgium, CERN, Finland, France, New Zealand, Germany, Italy, Japan*, Switzerland, UK, USA

CRYSTAL ECAL

Belarus, CERN, China, Croatia, Cyprus, France, Ireland, Italy, Japan*, Portugal, Russia, Serbia, Switzerland, UK, USA

PRESHOWER

Armenia, Belarus, CERN, Greece, India, Russia, Taipei, Uzbekistan

RETURN YOKE

Barrel: Czech Rep., Estonia, Germany, Greece, Russia
Endcap: Japan*, USA, Brazil

SUPERCONDUCTING MAGNET

All countries in CMS contribute to Magnet financing in particular:
Finland, France, Italy, Japan*, Korea, Switzerland, USA

HCAL

Barrel: Bulgaria, India, Spain*, USA
Endcap: Belarus, Bulgaria, Russia, Ukraine
HO: India

FEET

Pakistan, China

MUON CHAMBERS

Barrel: Austria, Bulgaria, CERN, China, Germany, Hungary, Italy, Spain,
Endcap: Belarus, Bulgaria, China, Korea, Pakistan, Russia, USA

FORWARD CALORIMETER

Hungary, Iran, Russia, Turkey, USA

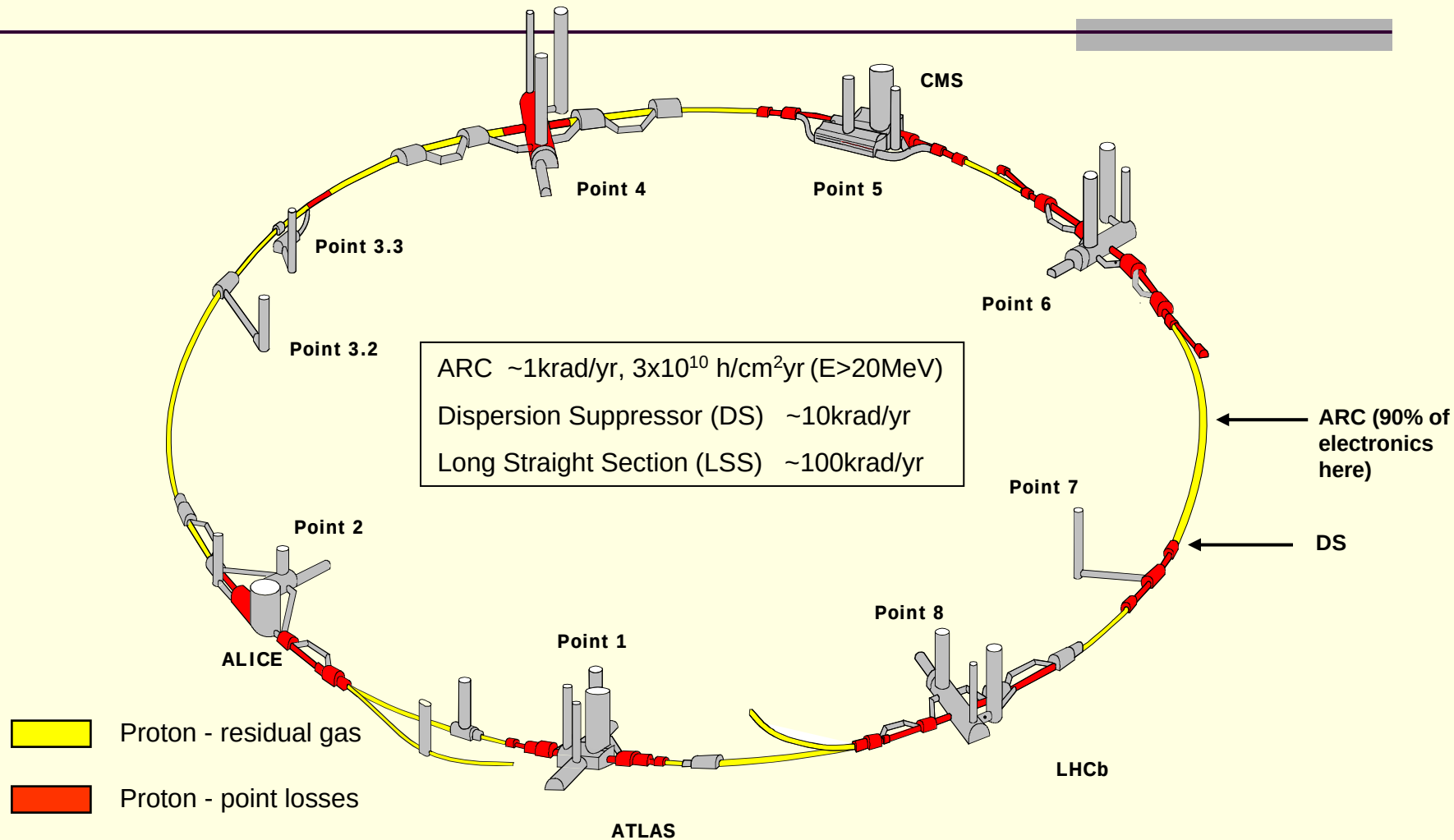
Total weight : 12500 T
Overall diameter : 15.0 m
Overall length : 21.5 m
Magnetic field : 4 Tesla

* Only through industrial contracts

Radiation qualification for the experiments

- Each experiment has 1 person/group in charge of radiation environment simulation (that changes sometimes in time...)
- ATLAS:
 - RHAWG decided on procedures to be followed for testing and qualification of components (update simulation data; decide test procedures for sources, number of samples, strategy; safety factors, etc.)
 - Review of implementation at EDR (Engineering Design Review) and PRR (Production Readiness Review)
- CMS, Alice, LHC-B: test procedure “suggested” in organized tutorial-workshop events, then review of implementation at EDR and PRR
- Very different than for space missions:
 - No specialized group of “professionals in radiation effects”
 - No sharing of testing expertise and effort
 - No “centralized” procurement (there are few exceptions, for instance the radiation tolerant voltage regulator)
 - Every collaboration is fully responsible for all aspects of the deliverable (detector or sub-detector), including radiation hardness
 - Need for educating a large number of engineers in all Countries, since almost no expertise on radiation effects did exist before LHC in HEP community

Radiation levels in the LHC machine



Radiation is caused by beam losses

■ Collisions :

Single Diffractive & Elastic interactions result in debris barreling down the beam pipe

■ Beam gas interactions : (mostly from H, O, CO, CH₄, ...)

Elastic (scattered by point like Coulomb field from gas atom)

Multiple Coulomb scattering (protons within a bunch interact)

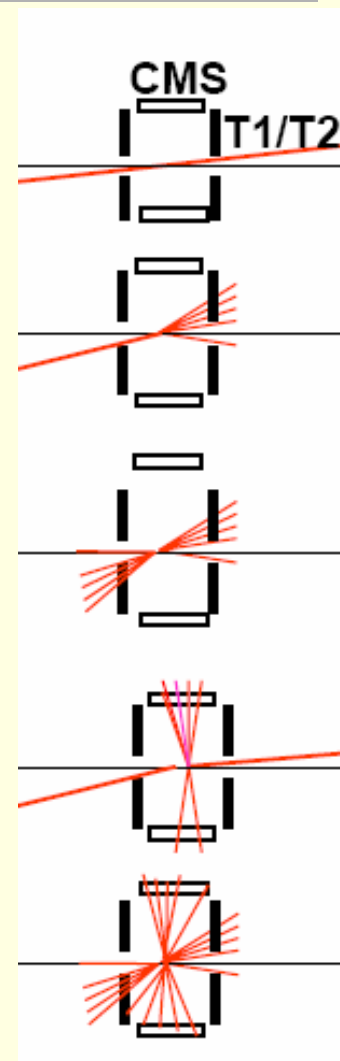
Inelastic (nuclear interaction of protons with the gas)

■ Other Loss mechanisms :

RF instabilities, Electron cloud, Mad operators, Resonances & beam instabilities

There is a **considerable uncertainty** on the radiation environment in the tunnel and experimental areas on the radiation tolerance of equipment.

A radiation monitoring system will help to **reduce this uncertainty by providing an early warning** as the radiation levels at the location of the electronic equipment increase.



Organization for LHC machine

- The decision to place electronics in the LHC tunnel was taken in January 1997 (Technical Coordination Committee, TCC):
 - *“The committee recommends that the base-line machine should use, where advantageous and following suitable testing, electronics located in the arc tunnel. This is based on the understanding that the radiation levels will be kept to less than 1 Gy per year in the area around the main dipoles and that suitable resources will be made available for adequate radiation testing”*
- Focus was on TID, not on SEEs (largely ignored at that time)
- In the following months, a RADWG (Working Group) was setup (Dec98), and a dedicated test facility was built (TCC2, June99). The facility took years to be fully characterized, but allowed for complete system tests since had particle spectra close to those expected in the tunnel, and flux 200 times larger over large areas – good for full systems! Now the facility has limited access.



Energy extraction switch,
Tested in TCC2

Radiation tolerance assurance LHC accelerator

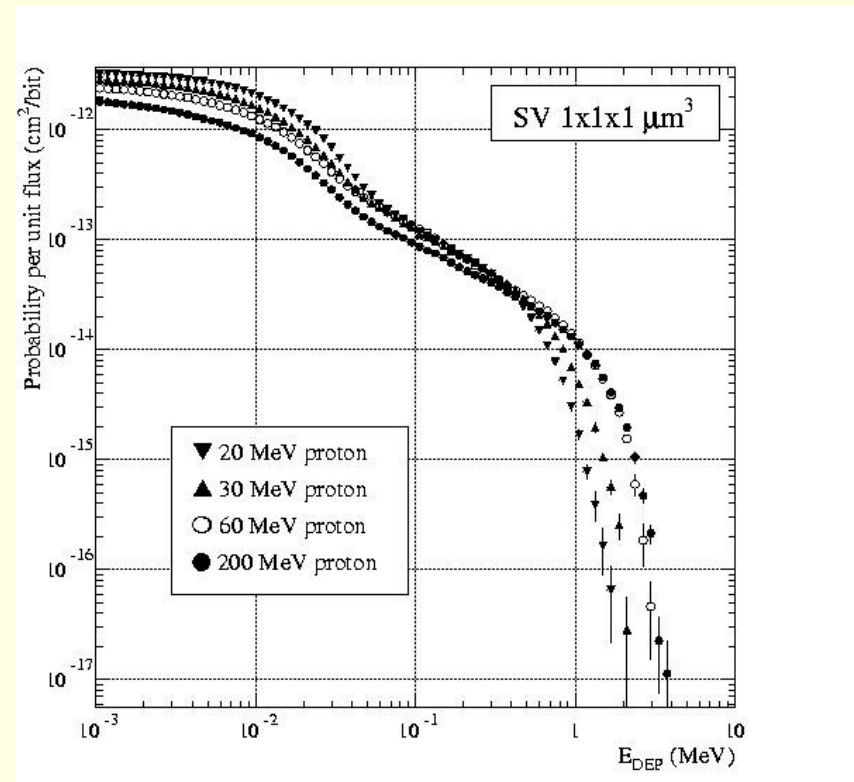
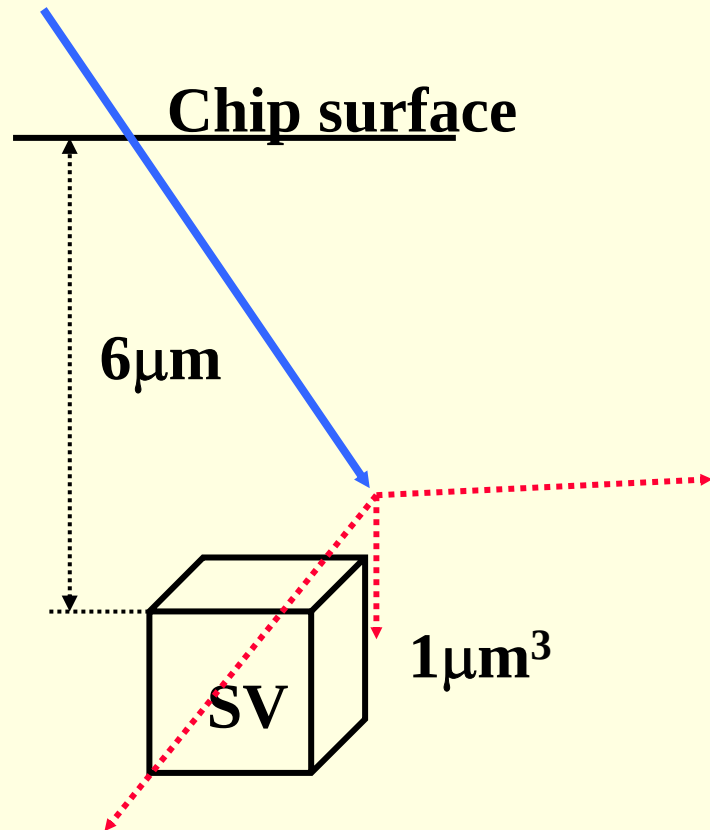
- **January 1997** : Baseline of the machine is to locate electronics under the main magnets in 27 km long tunnel
- **December 1998** : Start of the LHC Radiation Working Group (RADWG)
- **June 1999** : First radiation tests in LHC radiation test facility TCC2
- **December 1999** : Start integration of 12.000 electronic crates (with cabling) in the accelerator tunnel
- **September 2000** : Single Events from fast neutrons recognized as the major problem (not dose)
- **December 2001** : First Monte Carlo simulations of radiation levels in accelerator tunnel
First dedicated Single Event radiation tests in PSI and UCL
- **September 2002** : Discovery of a potential radiation hazard in other areas with electronics
- **2002 and 2003** : 110 hours of proton beam time, 38 experiments in LHC radiation test facility. RADWG evolves to include also RADMON, a programme devoted to monitor the radiation during commissioning and operation of the LHC machine
- **2003 and 2004** : Radiation testing decreases, as series production of electronics is starting
- **2005 and 2006** : Installation of electronics in tunnel
- **2007** : Showtime !

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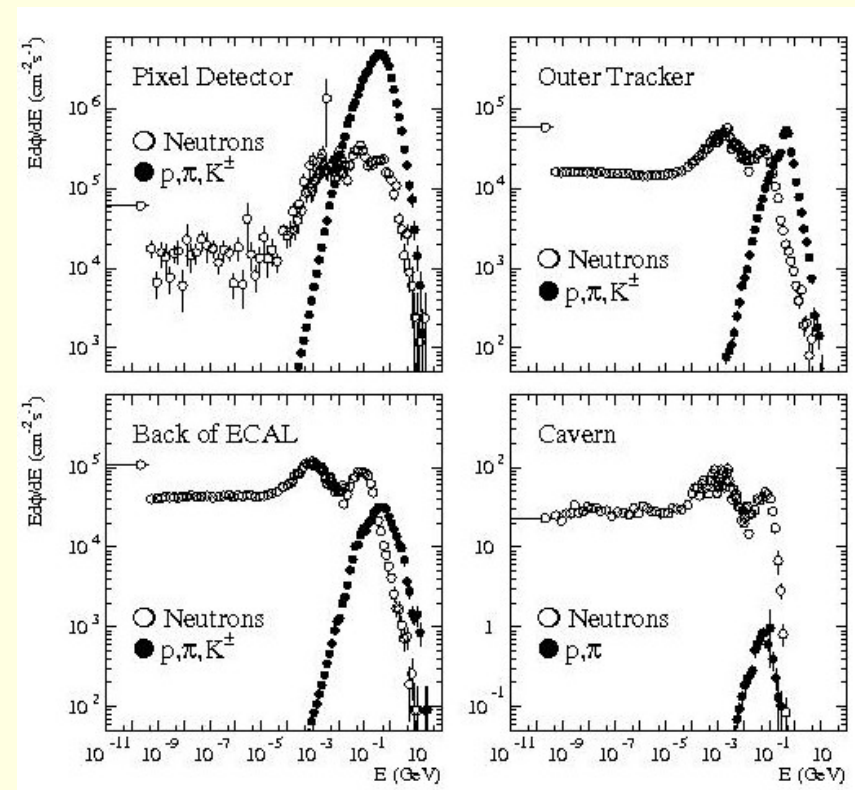
Why testing at 60-200MeV proton beams?

- Results from simulation-based work on computing SEU rates in accelerator environments (1998-2000)



Why testing at 60-200MeV proton beams?

- Particle spectra typically peak (for SEEs) around 60-200MeV
- Facilities are available in that energy range
- Protons also ionize and give displacement: it is possible to have all radiation effects in one only irradiation test (TID, SEEs, displacement)



Particle spectra in CMS

Estimate of error rate

- Test performed at only 1 proton energy (other if possible, but not required): highest available energy – but 60MeV is the minimum
 - Computation of the cross-section N_{errors}/Φ
 - Estimate of the error rate from the cross-section and the foreseen flux of hadrons above 20MeV (hypothesis: $h>20\text{MeV}$ dominate the rate, and have all the same cross-section)
 - The approach is not meant to give a perfectly correct estimate, only an order of magnitude, but
 - It provides easy guidance to non-expert personnel
 - It is realistic, since it proposes a relatively light procedure and easily accessible proton sources
 - It is the best we can do given the schedule constraints, the available resources, and our organization

Main facilities used

- Cyclone at CRC-UCL (Louvain-la-Neuve, Belgium) as from 2000: 60-70MeV protons
- PIF in PSI (Villigen, Switzerland) as from 2002: 70 or 200MeV protons
- Tests of different groups (experiments, machine) organized in “irradiation campaigns” over 1-3 days
- More than 750 hours of beam used so far, in 25 irradiation campaigns
- Each group is responsible for the test (no supervision, exception for LHC machine)
- Some results collected in an “LHC database” available on the web, but most often no sharing of results – also because the testing started in a late phase and often concerned prototype or final boards (go-nogo approach), not individual components

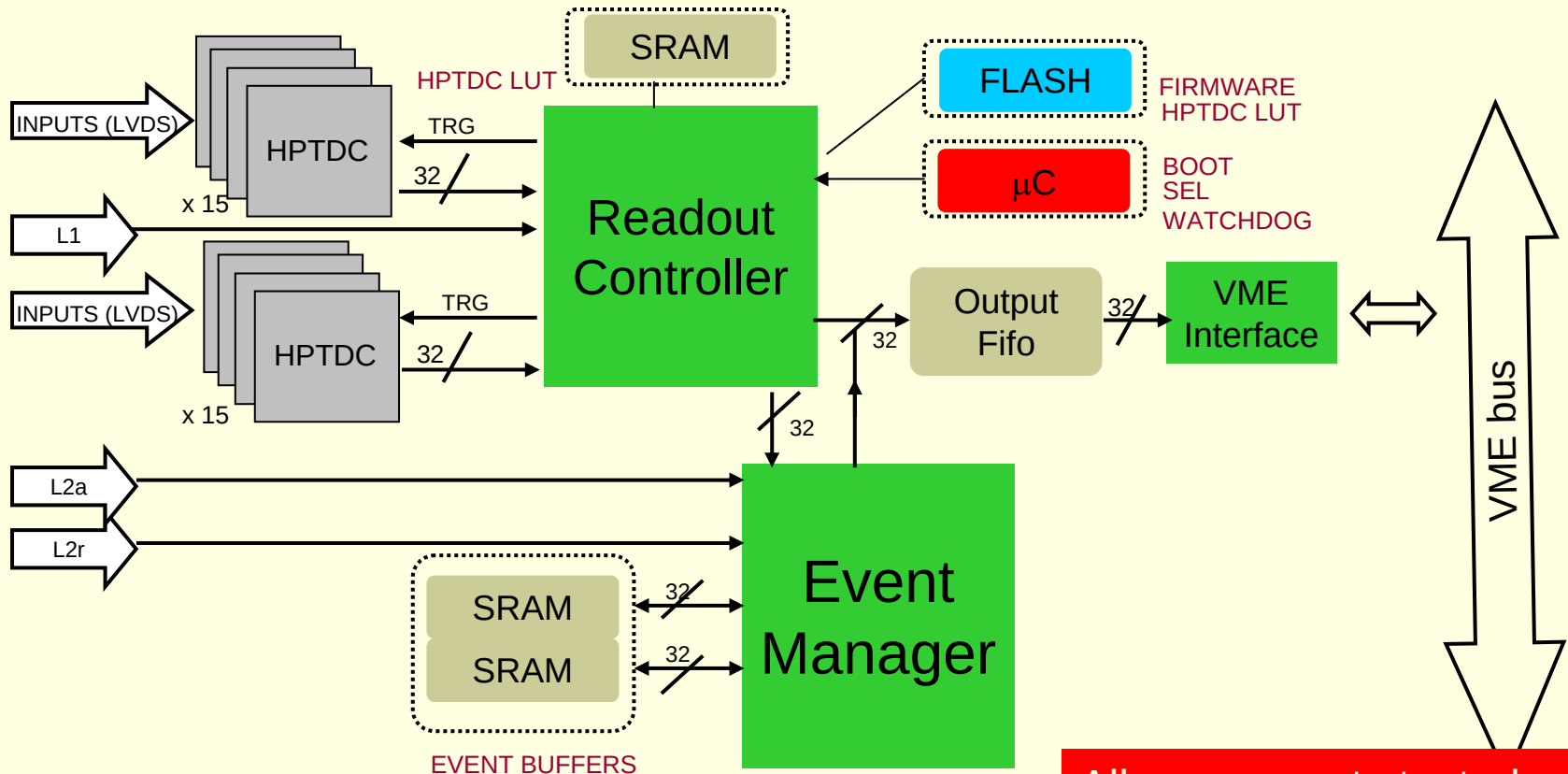
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Example 1: Alice TOF (1)

From P.Antonioli, INFN Bologna

684 Tdc Readout Module inside crates



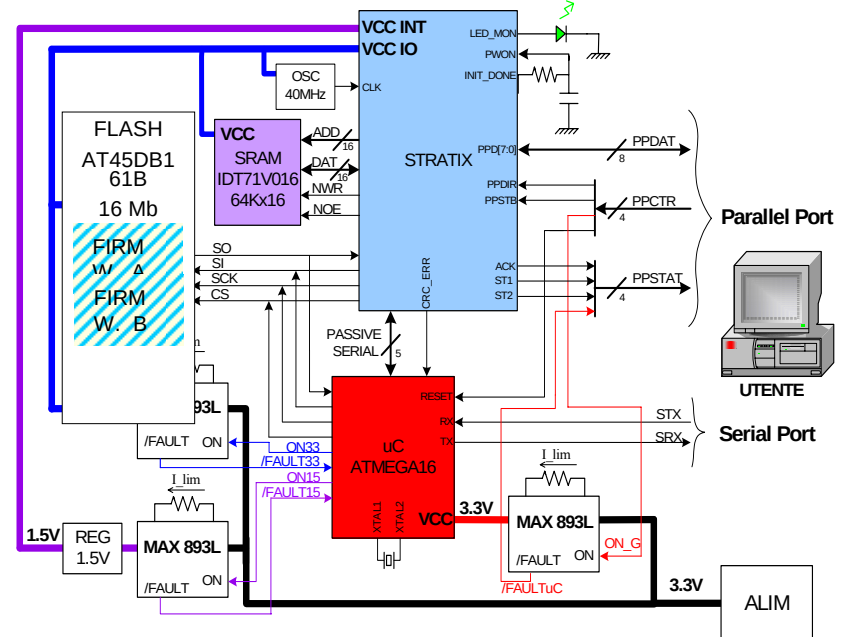
Functionalities implemented by an FPGA

All components tested during irradiation campaigns in 2004

Example 1: Alice TOF (2)

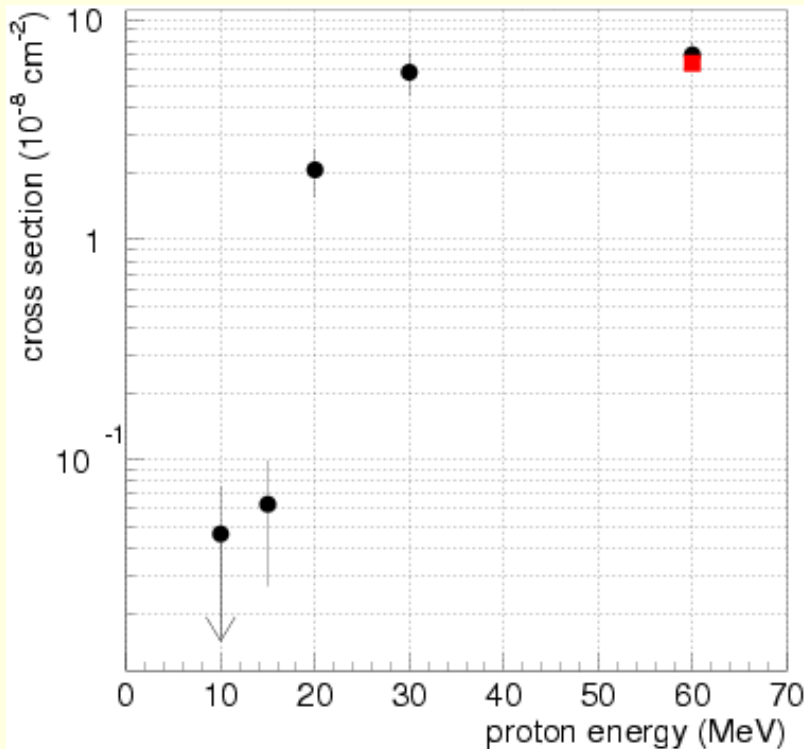
- Test card for all components: Altera Stratix EP1S20F780, IDT Ram, Atmel Flash and Micro) and latchup/SEU error recovery strategy
- Altera Stratix (and Cyclone) feature: real-time monitoring of configuration bits: a clear procedure to establish configuration changed (effective SEFI monitor)
- Atmel μ C acts as controller of power fault (latchups) + CRC_ERROR pin
- Monitor of errors in SRAM, FPGA internal memory + shift register logic check

Test at PSI (Zurich)
June 2004



Example 1: Alice TOF (3)

ALTERA STRATIX EP1S20 (configuration upset)



$$\sigma = (6.5 \pm 0.2 \text{ (stat)}) 10^{-8} \text{ cm}^2$$

Cross-section too large for the application: will replace with Actel ProAsic Plus

Example 1: Alice TOF (4)

Device	DCS (cm ²)	DCS/bit (cm ² /bit)
STRATIX (EP1S20)	$6.5 \cdot 10^{-8}$	$1.1 \cdot 10^{-14}$
STRATIX (INTMEM)	$1.8 \cdot 10^{-8}$	$3.4 \cdot 10^{-14}$
FLASH (AT45DB161B)	$< 0.9 \cdot 10^{-12}$	$< 10^{-19}$
ATMEL μ C (ATMEGA 16)	$< 0.9 \cdot 10^{-12}$	
SRAM (IDT71V416S)	$3.6 \cdot 10^{-8}$	$8.5 \cdot 10^{-15}$
Other (clock, voltage regulators,..)	No damage up to 14 krad	

No latchup observed. TID = 14 krad.

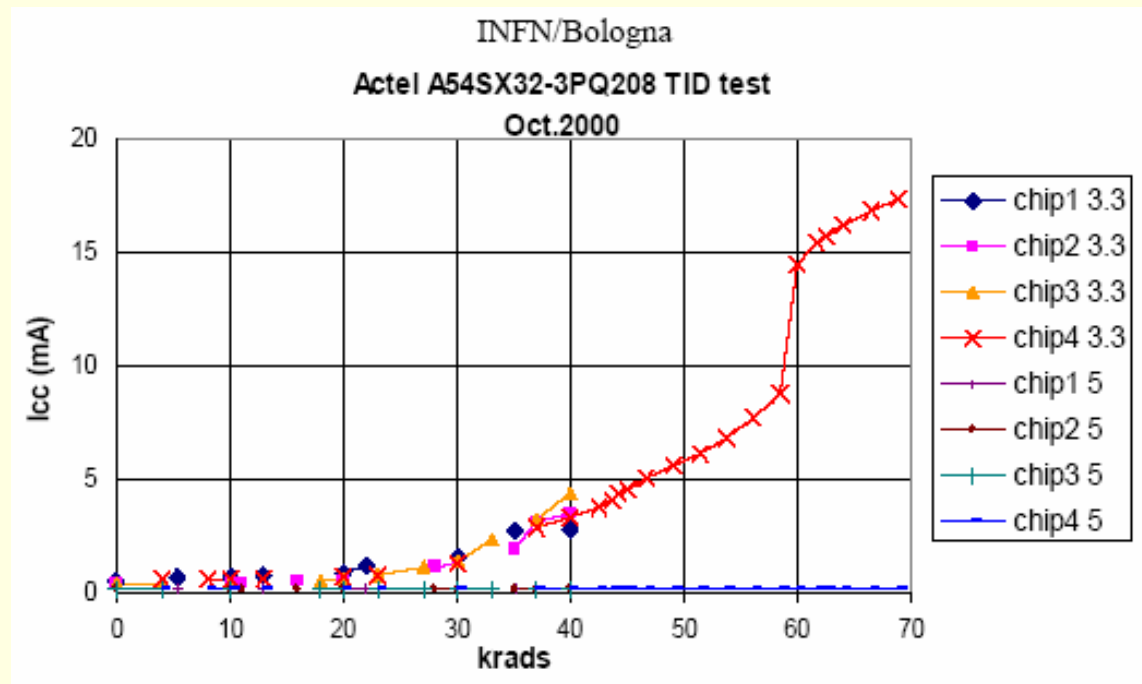
Example 2: CMS Muon Barrel (1)

From M.Dallavalle, INFN Bologna

- One FPGA used to implement the logic functions required by the system (different configurations used)
- The ACTEL A54SX32 has been chosen as the best and most cost-effective solution (48K gates). Integration of the required function uses 75-85% of the resources
- Test performed at CRC (60MeV) on 4 samples, each implementing a 450 bit register (450 FFs), refreshed and monitored at 1 MHz
- 3 samples up to 40krad, 1 sample up to 70krad
- Total integrated fluence (for the 4 chips) = $1.4 \times 10^{12} \text{ cm}^{-2}$
- Results:
 - No latch-up detected
 - No TID-induced failure, even though large increase in current (at doses well above the required level)
 - 1 logic error event: suddenly 1/3 of the FF changed state, probably due to glitch in the clock distribution

Example 2: CMS Muon Barrel (2)

- From the SEU cross-section and the environment in the application, the estimate error rate is $< 2.2 \text{ errors/10 years}$ for the whole system (about 1000 chips)



Example 3: ALICE DAQ (1)

From C. Soos, CERN

- Test of components for the DAQ DDL system using γ and n sources (TID, displacement) and protons in Uppsala – since a Swedish group is part of the collaboration
- Components used: crystal oscillators, Voltage regulators, electrical transceivers, optical transceivers, FPGAs
- The only component having real problems in the system is the FPGA. The design uses the ALTERA APEX-E (currently EP20K60E 160 kgates - 0.18 μ), for which the estimate error rate in the experiment is 1 loss of configuration per hour (for the 400 devices used in the system), some of which undetected
- Alternative solutions foresee the use of either:
 - Devices based on SRAMs that flag errors in the configuration (from Altera or Xilinx)
 - Devices based on flash memory to store the configuration (from Actel)

Example 3: ALICE DAQ (2)

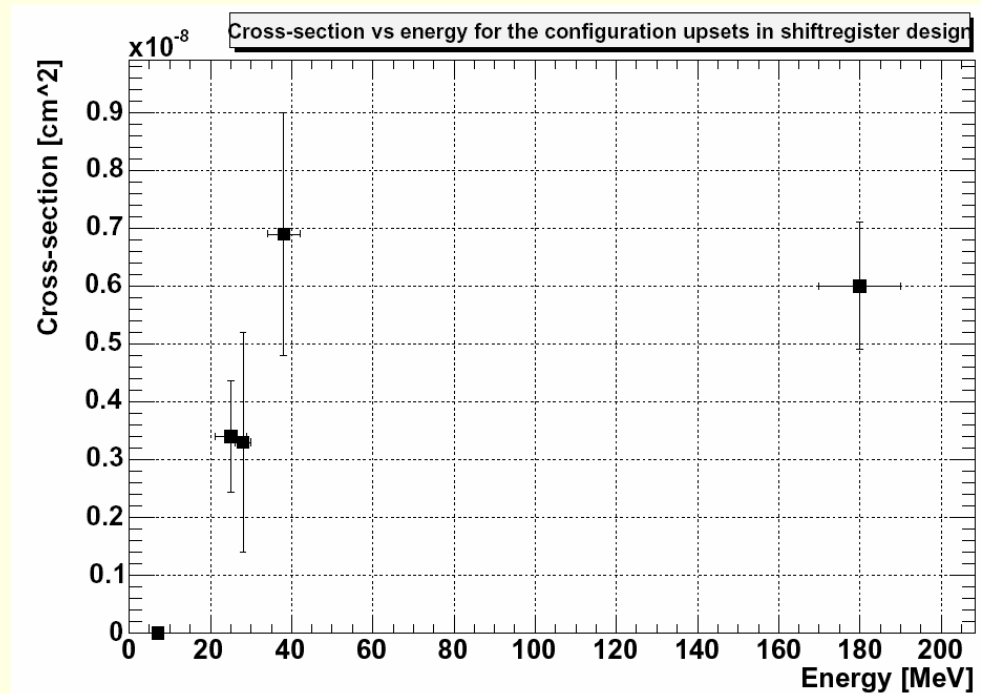
- Altera APEX-E (0.18 μm CMOS) SRAM-based
 - σ configuration cell: $\frac{4.90 - 8.20 \cdot 10^{-13} \text{ cm}^2/\text{LC}}{1.66 - 7.06 \cdot 10^{-14} \text{ cm}^2/\text{LC}}$ @ 180 MeV (p)
@ 5-14 MeV (n)
 - σ memory cell: $\frac{3.08 - 4.24 \cdot 10^{-14} \text{ cm}^2/\text{bit}}{4.64 - 5.86 \cdot 10^{-14} \text{ cm}^2/\text{bit}}$ @ 180 MeV (p)
@ 100 MeV (p)
@ 5-14 MeV (n)
- Xilinx Virtex II (0.15 μm CMOS) SRAM-based
 - σ configuration cell: $\frac{4.5 - 9.0 \cdot 10^{-13} \text{ cm}^2/\text{LC}}{5.5 - 10.2 \cdot 10^{-13} \text{ cm}^2/\text{LC}}$ @ 171 MeV (p)
@ 94 MeV (p)
@ 48 MeV (p)
- Actel ProASIC+ (0.25 μm CMOS) Flash-based
 - σ logic tile: $< \frac{2.03 \cdot 10^{-13} \text{ cm}^2/\text{LC}}{1.19 \cdot 10^{-13} \text{ cm}^2/\text{LC}}$ @ 171 MeV (p)
@ 94 MeV (p)
@ 48 MeV (p)
 - TID: temporary damage at 12 krad; device has been recovered after one hour at room temperature.

Example 4: ALICE TPC control (1)

From D.Rohrich, University of Oslo

- Main concern for their application: SEE in FPGAs
- Tests performed in Oslo (up to 28MeV) and Uppsala (up to 180MeV) to reconstruct sensitivity as a function of energy (4 points)

- Altera APEX20k400
- CS = $6.0 \times 10^{-9} \text{ cm}^2$



Example 4: ALICE TPC control (2)

- Summary of SEFI cross-sections for different FPGA tested (at 180MeV):

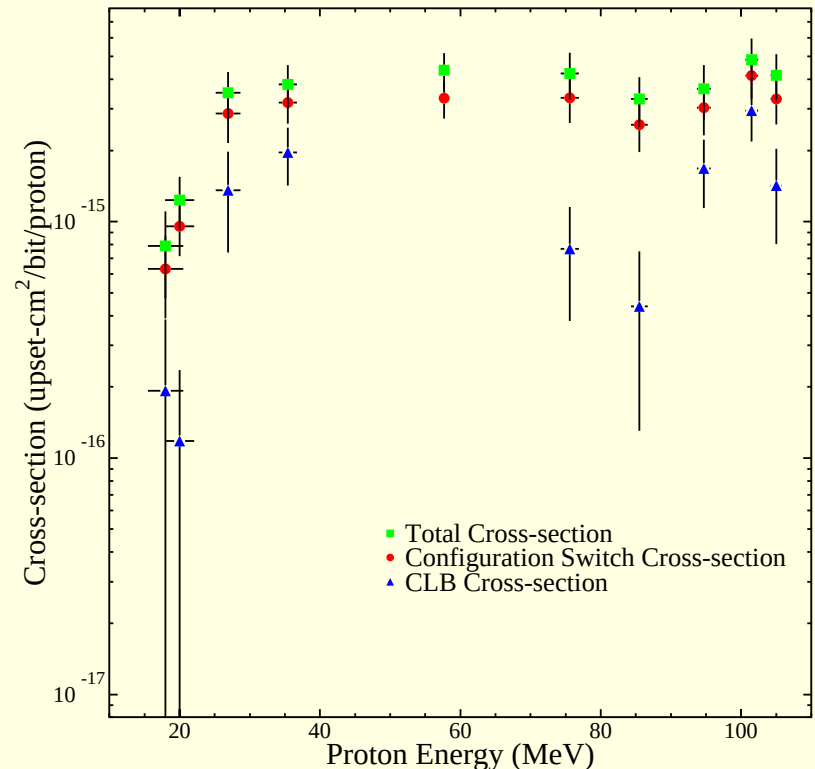
Altera APEX20k400	$6.0 \times 10^{-9} \text{ cm}^2$
Altera APEX20k60E	$1.6 \times 10^{-9} \text{ cm}^2$
Altera EPXA1F484C1	$2.0 \times 10^{-9} \text{ cm}^2$
Xilinx XC2VP7 – Virtex II-Pro	$2.0 \times 10^{-8} \text{ cm}^2$

- Error rate acceptable provided one can correct the configuration errors – Xilinx much better for this, since it allows for detection and even partial reconfiguration while running
- Alternatively, use of a ProASIC Flash from Actel (candidate APA075). Preliminary test at 25-28MeV protons showed no SEFI up to $3.7 \times 10^{11} \text{ pcm}^{-2}$, then TID failure (100krad equivalent)

Example 5: ATLAS LAr ECAL

From N.J.Buchanan, University of Alberta

- Test of Xilinx XC4036XLA-09HQ240C FPGA using protons at Triumf PIF (Vancouver) up to 120MeV
- Estimated rate of error is 1/17minutes for the full system (3000 devices)
- For TID, the current consumption starts to sharply increase around 40krad, and the device starts to have functional problems around 60krad



Example 6: ADuC (1)

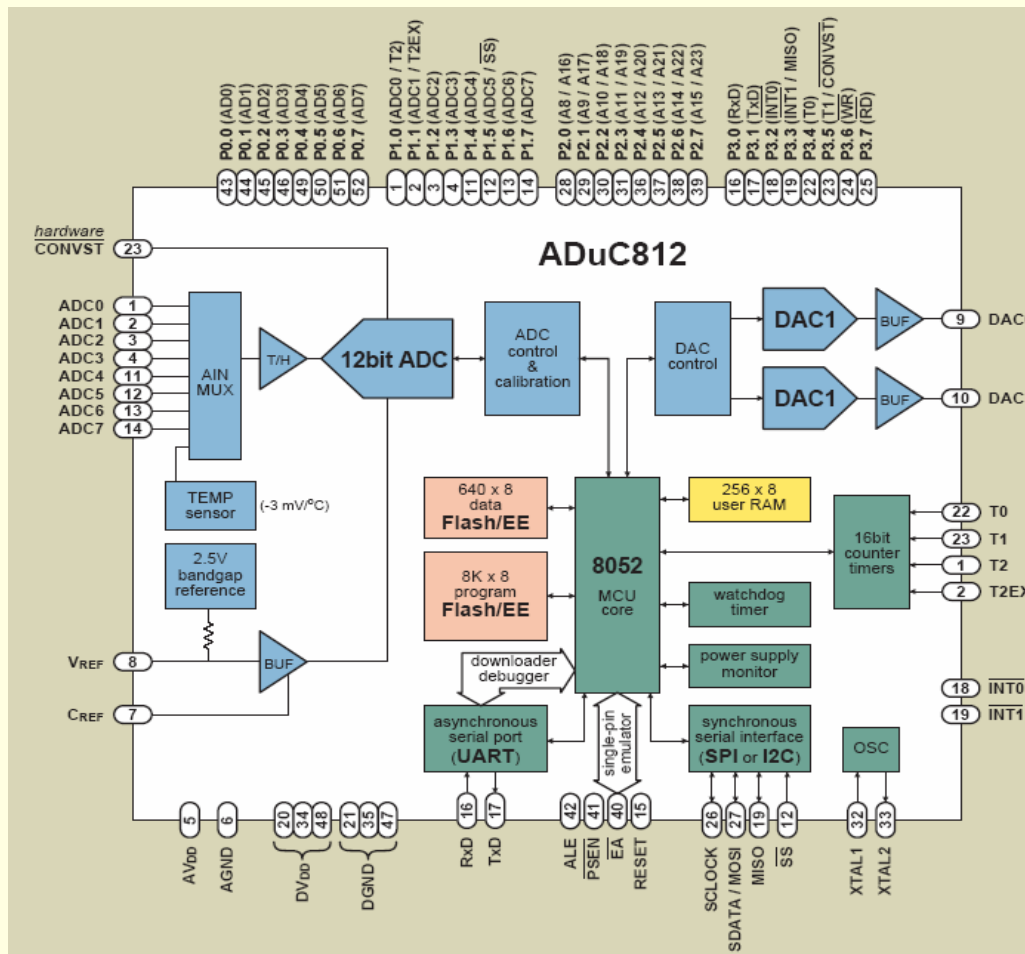
From LHC machine groups

- ADuC8XX micro-converter family
 - ADuC812
 - 8 channel 12 Bit ADC + 8051 compatible core + 8k Flash EEPROM
 - 4000 devices in LHC tunnel
 - ADuC831
 - As ADuC812 but 62k Flash EEPROM
 - 2200 devices in LHC tunnel
 - Core of Quench Protection acquisition & monitoring controllers
 - ADuC834
 - 24 Bit ADC + 8051 compatible core + 62k Flash EEPROM
 - 2600 devices in LHC tunnel

Note : 1 year LHC tunnel = TID : 1krad, 1×10^{10} h/cm², 1×10^{11} n/cm²

R. Denz CERN AT Department

Example 6: ADuC (2)



Example : ADuC812

Characteristics :

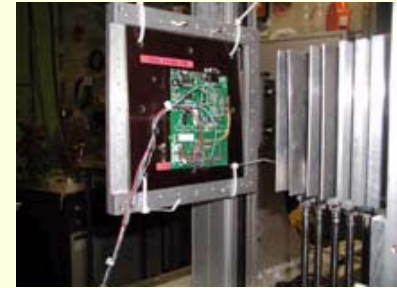
- 8-Channel, 5 μ s, 12-Bit ADC
- Two 12-Bit Voltage-Output DACs
- Industry Standard 8052 Microcontroller
- 8K-Byte Re-Programmable Flash Memory
- 640-Byte Non-Volatile Flash Memory
- 16 MHz operation

Technology :

- 56 pin Lead Plastic Flat Quad Pack Package
- powered at 3 or 5 V (5 V for SEU tests)
- dimension 0.4 μ m

Example 6: ADuC (3)

- Proton beam at PSI (OPTIS beam-line)
 - $5 \times 10^8 \text{ p cm}^{-2}\text{s}^{-1}$
- Functional test of the chip
 - Communication during the test via serial port
 - Download of test software via serial port
- Memory access tests
 - ADuC812: external SRAM (SAMSUNG K6T0808C1D-TB70)
 - ADuC831 & ADuC834: internal & external SRAM (CYPRESS CY62256LC-70ZC), internal Flash EEPROM
- Error correction algorithm
 - Bitwise triple voting for data stored in external SRAM validated



$$\text{data}[i] = (\text{d}[0][i] \& \text{d}[1][i]) | (\text{d}[0][i] \& \text{d}[2][i]) | (\text{d}[1][i] \& \text{d}[2][i])$$

Example 6: ADuC (4)

	TID failure	σ int SRAM (per bit)	σ ext SRAM (per bit)	Correct. Effic. Triple voting
ADuC812	15-18krad		$1.0 \times 10^{-13} \text{cm}^2(1)$	100%
ADuC831	14krad	$1.2 \times 10^{-13} \text{cm}^2$	$1.6 \times 10^{-13} \text{cm}^2(1)$	100%
ADuC834	5krad	$1.1 \times 10^{-13} \text{cm}^2$	$0.7 \times 10^{-13} \text{cm}^2(2)$	100%

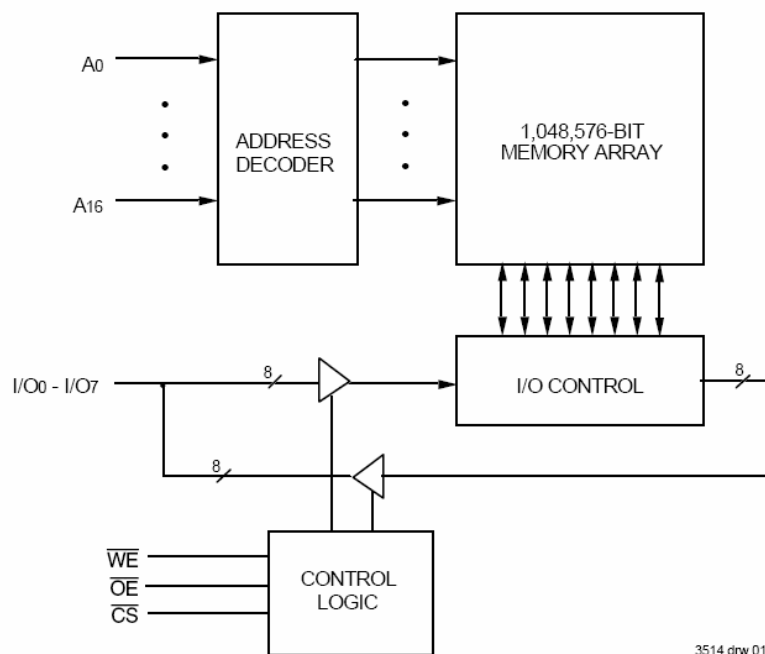
(1)= SAMSUNG K6T0808C1D-TB70

(2)= CYPRESS CY62256LC-70ZC

Example 7: SRAM – IDT71124 S15Y (1)

From LHC machine groups

Functional Block Diagram



IDT71124 S15Y 128 kB

Characteristics :

- 0.5 μm CMOS technology
- Asynchronous operation (no clock)
- 5 V operation
- 1 Mbit (128 K words x 8 bits)
- min cycle time 12 ns
- 32 pin 400 mil plastic SOJ packaging

Irradiation in a complex (HEP) radiation field :

- No latch up
- Correct operation at 20krad TID
- No Multiple Bit Upsets

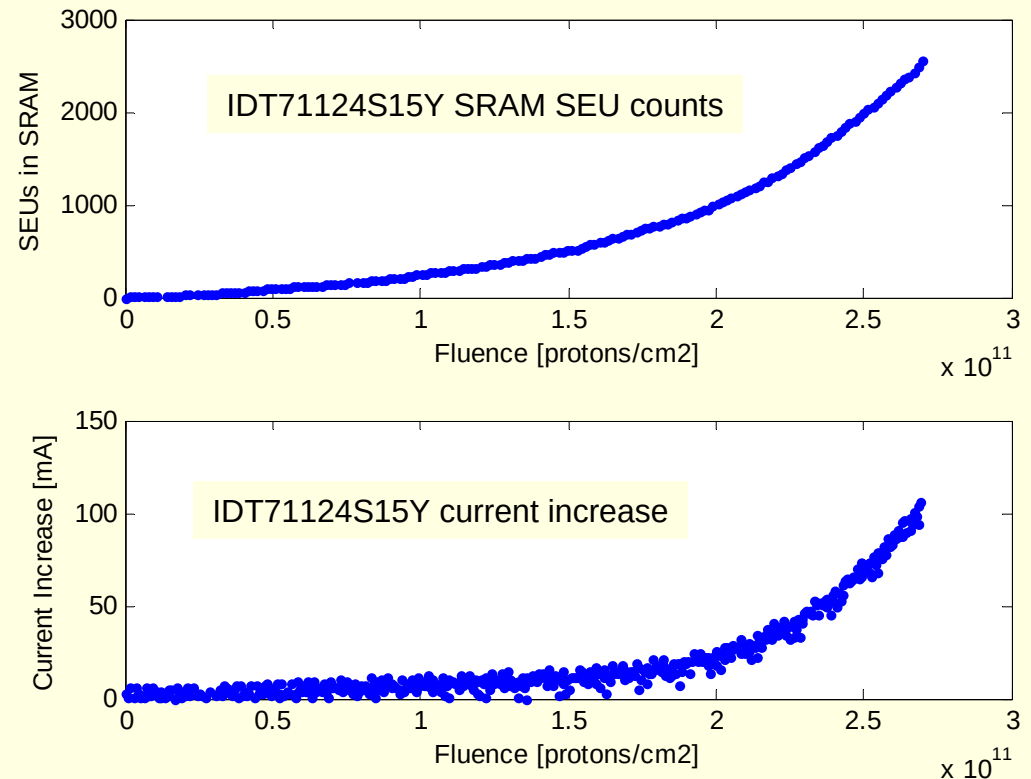
http://www1.idt.com/pcms/tempDocs/71124_DS_89431.pdf

~7000 devices in LHC tunnel

Example 7: SRAM – IDT71124 S15Y (2)

Results for 60 Mev Protons

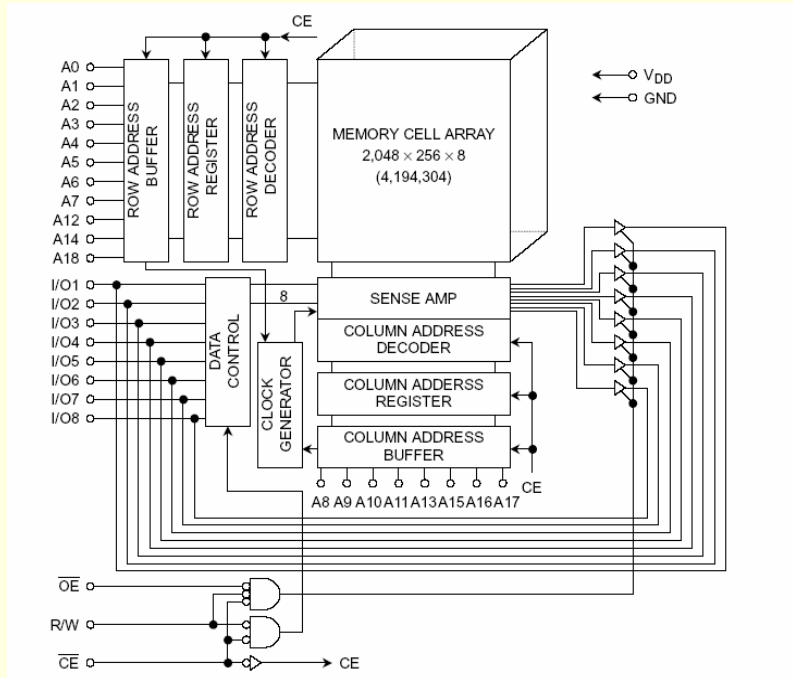
- TID effects start at ~ 12krad
- Proton cross section :
 $\sigma = 1.9 \times 10^{-15} \text{ cm}^2 \text{ per bit}$



IDT71124 S15Y 128 kB

Example 8: SRAM - TC554001AF-70L(1)

From LHC machine groups
C,Pignard CERN TS dept.



Toshiba TC554001AF-70L

~1000 devices in LHC tunnel

Characteristics :

0.4 μm technology

- 3 – 5 V operation
- 4 Mbit (524288 words x 8 bits)
- grid arrangement 8192 x 512
- min cycle time 70 ns

Heavy Ion Radiation tolerance (0.5 μm):

Latch up threshold $< 37 \text{ Mev.cm}^2/\text{mg}$

- SEU threshold $< 1.7 \text{ MeV.cm}^2/\text{mg}$
- No Multiple Bit Upsets
- Cross section 0 $\rightarrow$ 1 equal to 1 $\rightarrow$ 0
- No frequency effect at 1.25 MHz

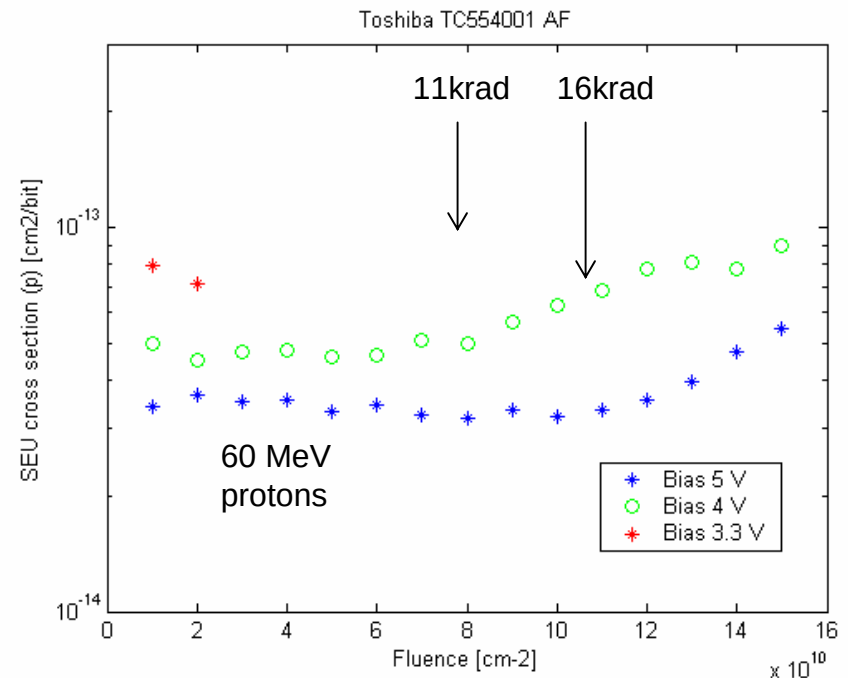
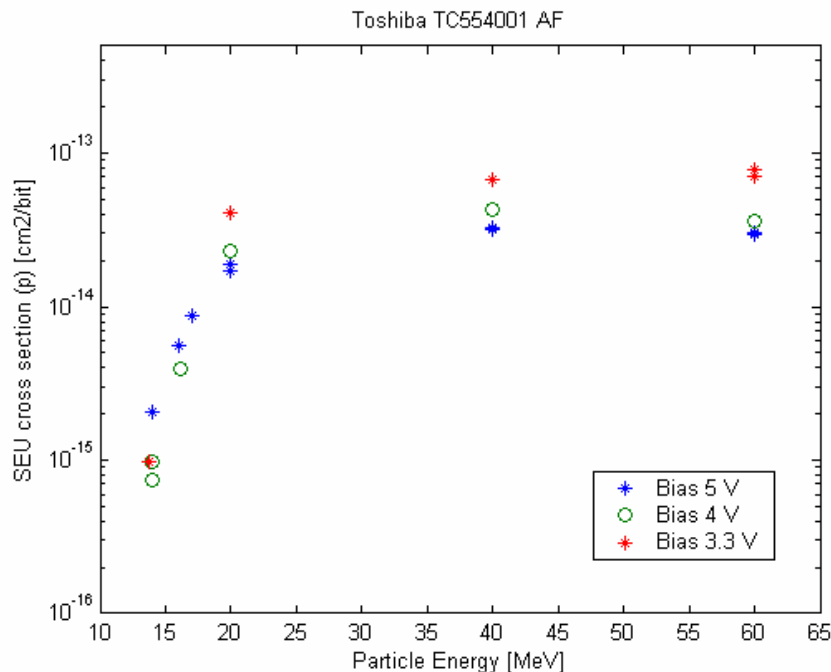
Neutron Radiation tolerance :

0.4 μm identical to 0.5 μm

- no latch up at $E_n = 180$ MeV

Ref. : Esa/Estec QCQ9956S-C
C. Sanderson, RADECS 2000

Example 8: SRAM - TC554001AF-70L(1)



SEU cross section :

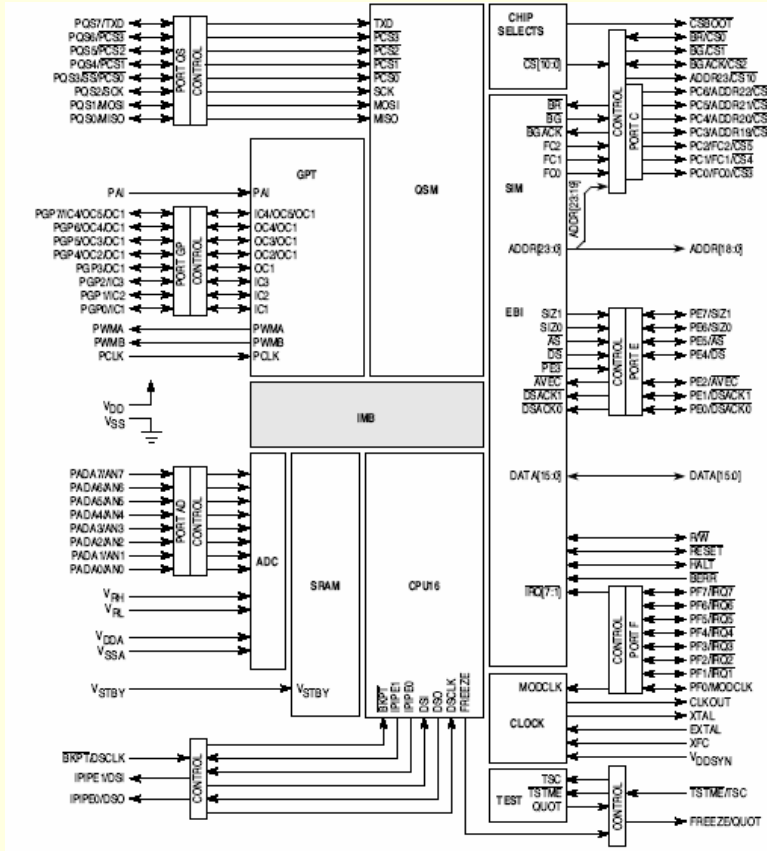
- 3 - 8 × 10⁻¹⁴cm²/bit depending on bias
- Identical to neutron cross sections
- No latch up

Cumulative effects :

- Sensitivity increased at higher dose (but can be used up to 20krad)
- Certain bits stuck at "0" after ~16krad (but can be annealed out at 100 °C – 4hrs)

Example 9: M68HC16Z1CFC16 (1)

From LHC machine groups
Q.King CERN AB dept.



Characteristics :

- 16 bit integer μ controller
- 16 MHz clock
- High density CMOS
- 1 kB internal SRAM
- 1629 bits Internal Registers

60 MeV Proton irradiation procedure

- 3 DUTs
- Program in External flash memories (2)
- Internal SRAM unused but checked for SEU (write 0x5555 and check every 24 ms)
- Internal registers
 - only 32 bits used (critical)
 - 32 critical bits set to correct value
 - 1597 bits set to default value
 - check for SEUs every 24 msec
- External SRAM with EDAC

Motorola M68HC16Z1CFC16 @ 16 MHz

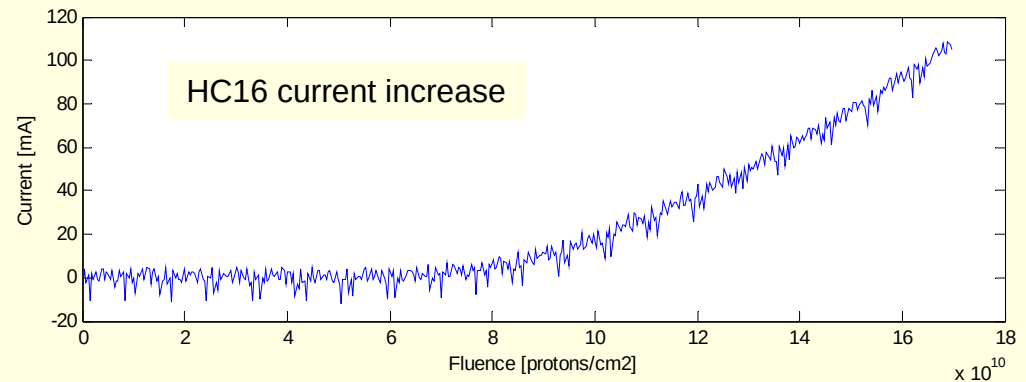
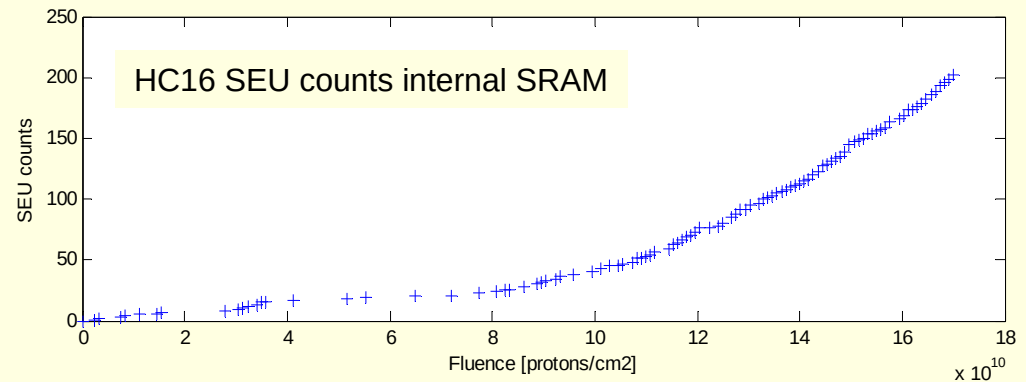
~750 devices in LHC tunnel

<http://www.mae.ncsu.edu/courses/mae589b/16z1ts.pdf>

Example 9: M68HC16Z1CFC16 (2)

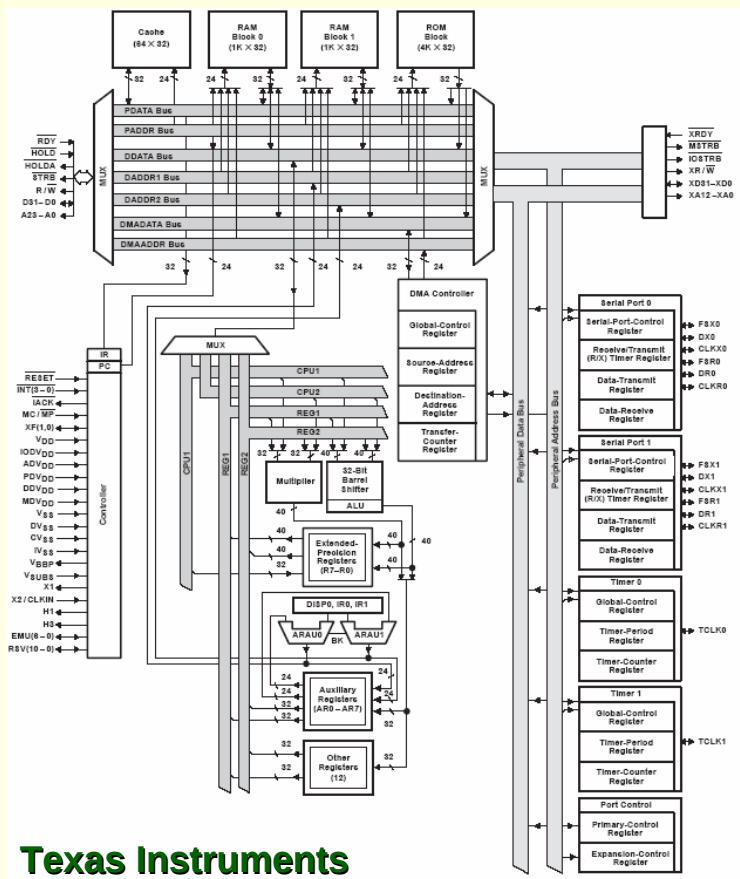
Results for 60 Mev Protons

- TID effects start at ~ 10krad
- No latchups or resets
- Internal registers :
 $\sigma = 5 \times 10^{-15} \text{ cm}^2 \text{ per bit}$ (3 SEUs in total in non critical bits in 3 devices)



Example 10: TI – TMS320C32PCM40 (HB) (1)

From LHC machine groups



Characteristics :

- 32 bit Floating point DSP 40 MHz
- High density CMOS
- 2 kB internal SRAM
- 465 bits Internal Registers

60 MeV Proton irradiation procedure

- 3 DUTs
- Operating frequency 32 MHz
- Backup program code in External flash (reloaded in C32 internal SRAM after reset)
- Operational code in Internal C32 SRAM
- Internal registers
 - only 40 bits used (critical)
 - 40 critical bits set to correct value
 - 425 bits set to default value
 - check for SEUs every 13 msec

~750 devices in LHC tunnel

Texas Instruments

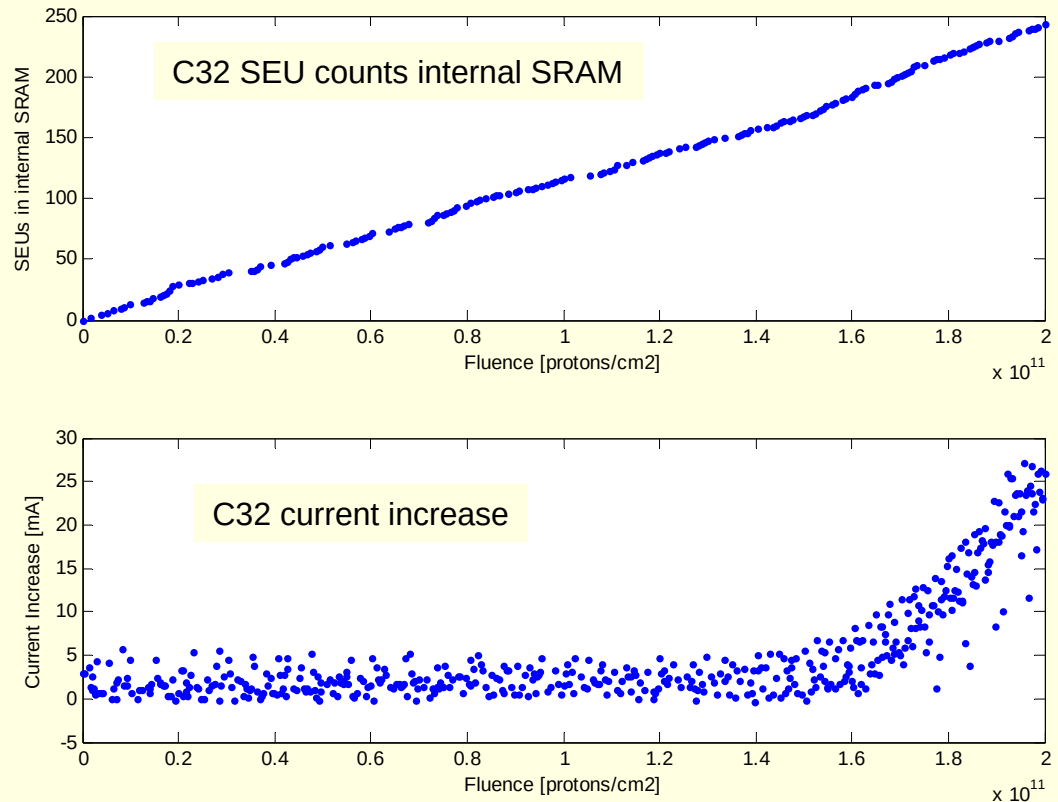
TMS320C32PCM40 @ 32 MHz

<http://focus.ti.com/docs/prod/folders/print/tms320c30.html>

Example 10: TI – TMS320C32PCM40 (HB) (2)

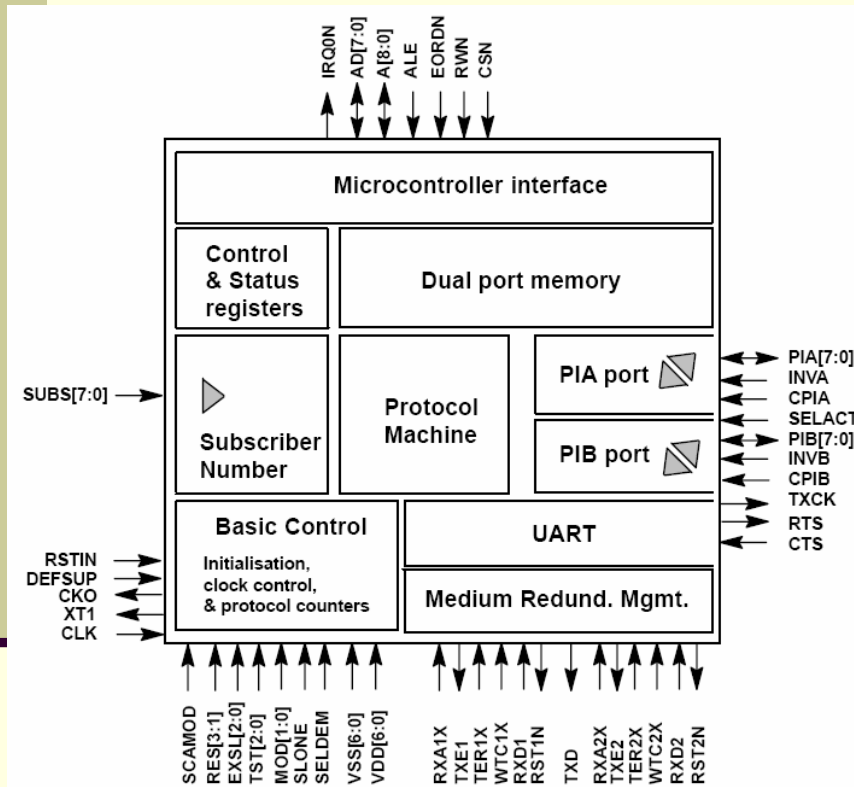
Results for 60 Mev Protons

- TID effects start at $\sim 19\text{krad}$
- No latchups - **1 reset** after 5×10^{11} 60 MeV p/cm²
- Internal registers :
 $\sigma = 1.5 \times 10^{-14}$ cm² per bit (6 SEUs in total in non critical bits in 3 devices)



Example 11: WorldFIP fieldbus – CC131 microFip (ASIC) (1)

From LHC machine groups
M.A.Rodriguez, CERN AT dept.



Characteristics :

- High density CMOS 0.6 μm
- Powered at 5 V or 3.3 V
- 31.25 kbit/s, 1 Mbit/s, 2.5 Mbit/s
- ASIC – MQFP100 packaging
- 512 bytes Dual Port Memory (incl 120 bytes Dynamic Data Memory)
- 128 bits Internal registers

~7500 devices in LHC tunnel

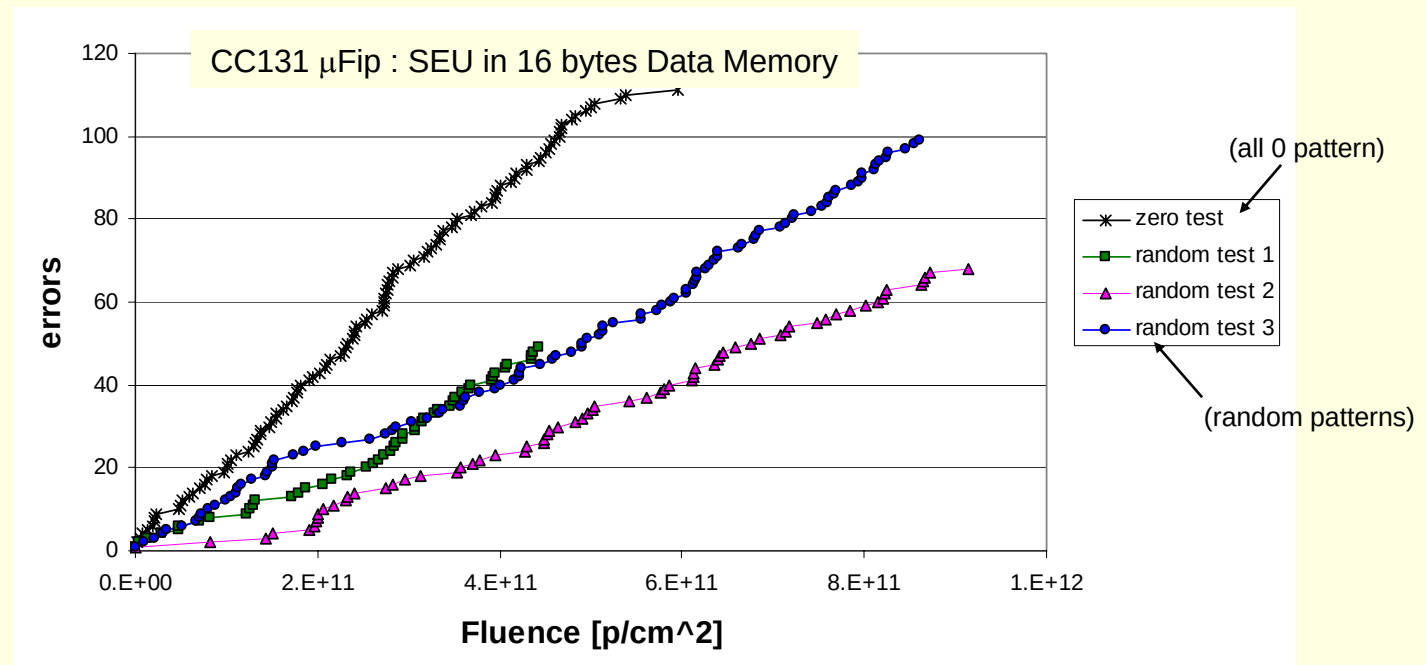
<http://www.worldfip.org>

CC131 μFIP Interface @ 40 MHz

Example 11: WorldFIP fieldbus – CC131 microFip (ASIC) (2)

SEE test with 60 MeV protons :

- CC131 Interface in μ controlled mode
- I/O back to back – use 2 variables of 8 bytes
- Write – Wait 10 sec – Read to/from data memory
- Internal registers refreshed every 200 ms by μ controller
- SEU cross section CC131 data memory $\sigma = 1.3 \times 10^{-11} \text{ cm}^2$ per bit



The LHC database

Experiment Part	Beam	Energy range	Component	Type	SEU Cross section per chip	SEE
Tile Cal HV Micro	PSI Proton Beam	300MeV	74HCT125-B	3 states gate	<3.6E-12	
			74HCT240-C	3 states buffer	<3.6E-12	
			74HCT244-C	3 states buffer	<3.6E-12	
			74HCT245-C	3 states buffer	<3.6E-12	
			MC7805 CD 2T	voltage regulator	Analog	
			PCA 82C 250T	CAN interface	3.60E-12	
			AD589JR	voltage reference	Analog	
			AMF29F010-70JC	flash memory	<8.5E-16 (bit)	
			AT25160N-10PC	EEprom	8.5E-16 (bit)	
			HCPL2611	opto coupler		
			K6T1008C2E	RAM	1.7E-14 (bit)	
			MAX233 ACWP	RS232 interface	<3.6E-12	
			MC68376 BGMFT20	Micro controller	1.80E-11	
			OPA 177GS	op amp	Analog	
TGC	CRC proton beam	70 MeV	A54SX08A	FPGA	<4.1E-13	
			SN65LV1023 (Tx)	LVDS deser	1.60E-12	2.60E-13
			SN65LV1224 (Rx)	LVDS ser	1.70E-12	3.70E-13
			SN65/75LVD family	LVDS logic	<2.5E-11	
			SN74LVTH541	Logic gate	<2.5E-11	
			SN74LVC541	Logic gate	<2.5E-11	
			SN74ALVC04	Logic gate	<2.5E-11	
			TC74AC521F	Logic gate	<2.5E-11	
			TC74SA00	Logic gate	<2.5E-11	
			TC74SA08	Logic gate	<2.5E-11	
			NL27WZ07	Driver	<2.5E-11	
			ADM708SAR	4-bits uP	<2.5E-11	
			IDT74FCT3807	Driver	<2.5E-11	
			AX250	AntiFuse FPGA	2.8E-14 (bit RAM)	
			AX250	AntiFuse FPGA	0.6E-14 (bit Register)	
			DS92LV1023 (Tx)	LVDS deser	1.20E-12	<1.2E-13
			DS92LV1224 (Rx)	LVDS ser	2.90E-11	<1.6E-13

Conclusion

- The radiation hardness assurance in both LHC machine and experiments is entire responsibility of the collaborations/groups delivering the components (control system, subdetector, ...)
- The LHC community has performed intensive radiation testing of components in the last 5 years
- The availability of proton beams has been crucial for this work, a special and big “THANK YOU” goes to CRC and PSI!
- Testing needs will most likely continue in the future, when problems in the field will start to be seen