Astrium View of Future Needs for Interconnect Complexity of Telecommunications Satellite On-board Digital Signal Processors

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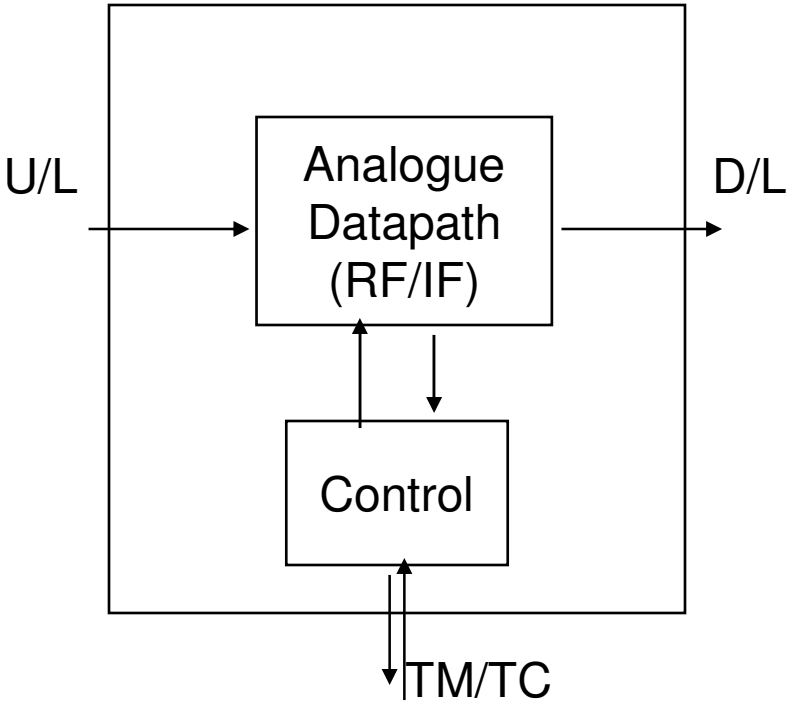
Main Themes of Presentation

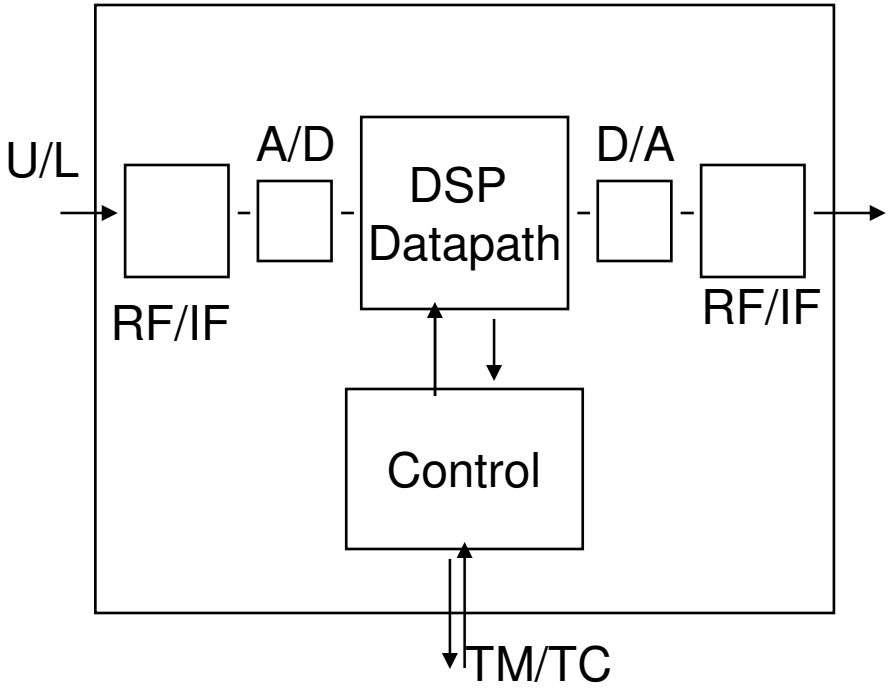
- **Context setting:**
  - What is on-board digital processing and why is it required?
- **Current generation digital processing**
- **Inmarsat 4 example**
- **Future trends in digital processing requirements**
- **Future technology and component needs**
- **Electrical HSSL requirements**
- **Complexity:**
  - Theoretical complexity of a symmetric Clos network
  - Candidates for practical next generation OBPs and their complexity
- **Conclusion**

Payload Architecture Options

Analogue Payload Architecture



Digital Processing Payload Architecture



Requirement for Payload Digital Processing

- **Transparent processing (no on-board demodulation)**
  - Flexible channel to beam routing in multiple beam systems
  - Flexible coverage in beam size, shape and location
  - Flexible frequency mapping between uplink and downlink
  - Flexible gain control

- **Regenerative processing (with on-board demodulation)**
  - Independent uplink and downlink signal format optimisation
  - On-board data rate conversion
  - Accommodation of different uplink and downlink air interface standards
  - Link advantage (potential saving of 3 dB on downlink)

Current Generation Digital Processing (some examples)

- **EADS Astrium** (main flight developments)
  - Inmarsat 4
  - Skynet 5
- **Alcatel Alenia**
  - Skyplex / Amheris
  - Syracuse
- **Boeing**
  - Thuraya
  - Spaceway
- **Lockheed Martin**
  - Aces
- **Northrop Grumman**
  - Milstar

Inmarsat 4 Processor Example

- **Processor capability was key factor in winning overall satellite contract**
- **Mission characterised by multiple spot beam coverage on mobile link (156 spot beams)**
- **Transparent digital processor required to provide flexibility**
  - Individual narrowband channels (200 kHz) flexibly routed to/from beams by control of digital beamforming weights applied to a multiple feed antenna
  - Frequency mapping flexibility by control of memory switch
- **Datapath functionality implemented in ASIC technology to limit power**
  - Comprises approx 2800 ASICs in 8 different designs
  - 0.65 micron technology from Honeywell with average of approximately 250 kgates
- **Custom A/D and D/A hybrids**
- **Second generation packaging approach**
- **Overall parameters – ~2000 W, 160 kg, 2 large units, significant cabling mass**
- **Enabling technologies were state-of-the-art 5 years ago** …
  - Small margin for supporting processors with higher arithmetic rates

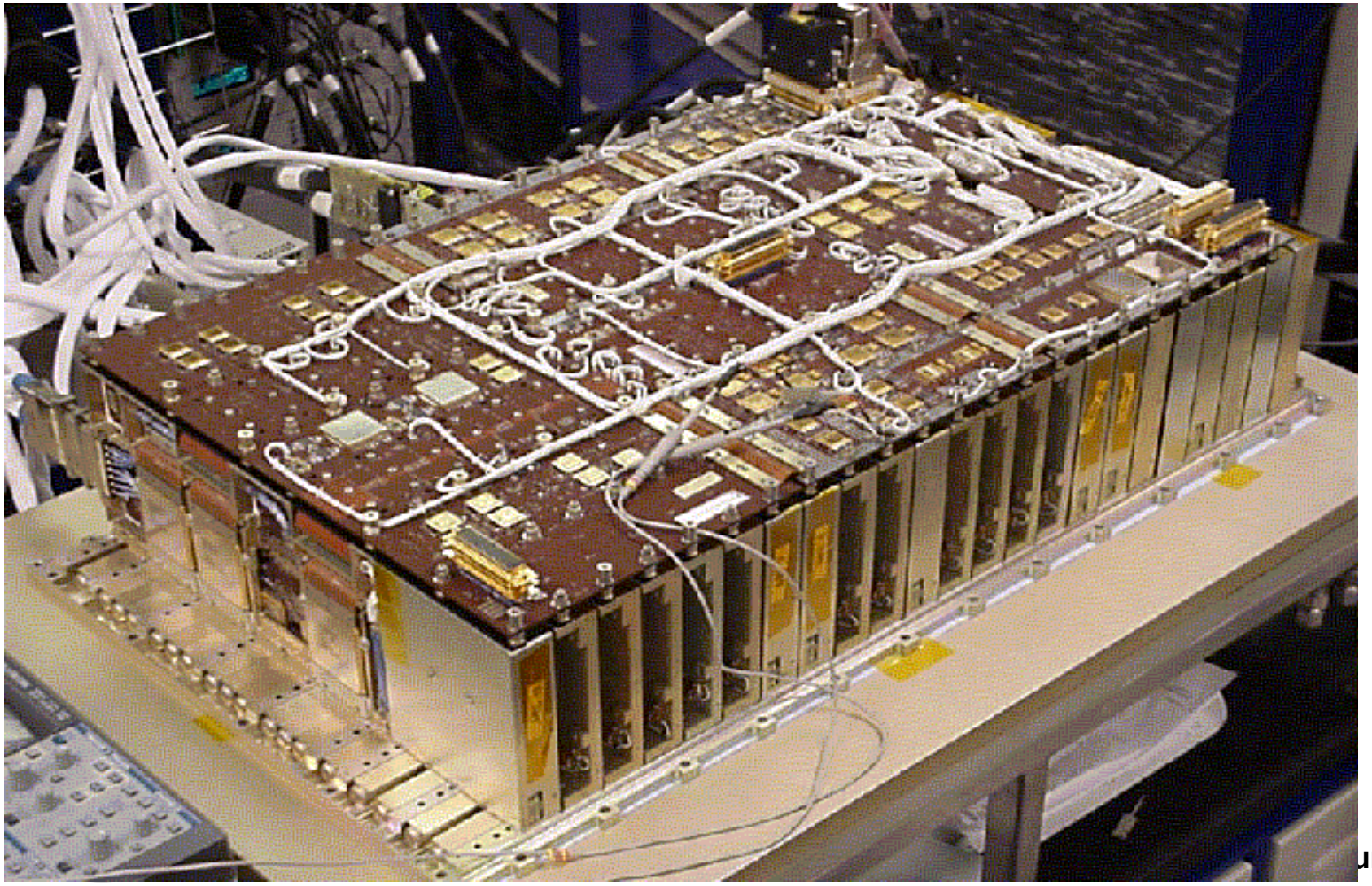
Inmarsat 4 Digital Processor

- First 2 spacecraft launched in 2005 (March & November)
- Mission supports 156 spot beams and 19 regional beams
- Fundamental requirement for flexibility in assigning capacity between beams and frequency bands – can only be met by a digital processor approach
- Processor interfaces to payload via analogue pre- and post- processors
- Channelisation and routing at 100 kHz granularity
- Independent level control on each channel
- Digital beamforming on 200 kHz channel basis - narrowband beamforming architecture
- Forward, Return and Mobile-to-mobile links
- Total routed capacity : 2 x 126 MHz
- Dedicated in-band TC/TM links for rapid routing reconfiguration

Inmarsat 4 Processor Technology

- 2 units per satellite (Forward & Return processors)
- 1.8 kW total power dissipation
- 160 kg total mass
- More than 2000 active ASICs per processor
  - 0.65 µm feature size, maximum of 300 kgates per ASIC
  - 8 separate ASIC designs
- ~300 low-power A/D and D/A hybrids
- Modular design using multi-chip modules (~180), integrating up to 10 ASICs each, wire-bonded and with up to 500 primary I/O
- 50 modules, connected to 3 back-planes/unit with up to 1000 I/O each
- ~1000 packaged ASICs in 228 ball DBGAs
- 20 bit buses running at ~20 MHz

Inmarsat 4 Processor: EQM Under Test



Needs for Digital Processing in Future Missions

- **Mobile missions**
  - Inmarsat 4 and Thuraya are flying – digital processing provides flexibility in channel to beam routing and frequency mapping
  - All future mobile missions will require transparent digital processing – increased processor complexity due to higher capacity and increased number of beams
  - Future global and regional systems
- **C/Ku and broadband (Ka) missions**
  - Trend is to increased numbers of beams with flexibility requirements in routing and frequency planning.
  - Transparent digital processing for main multi-beam forward and return traffic (MHz granularity) with wide processed bandwidth (several 100 MHz)
  - High processed traffic throughput (several 10s of Gbit/s)
  - Regenerative processing for part of traffic

General Trends in Processor Requirements

- Need is to support ever more demanding processor requirements within practical mass/power/volume constraints on the satellite
- Larger processed bandwidths (several 100s of MHz) associated with C/Ku/Ka band missions - implying the need for higher speed A/D and D/A converters
- Larger numbers of analog/digital interfaces (associated with larger numbers of beams and more complex antennas) – implying the need for low power A/D and D/A converters
- Increased dynamic range between processed signals – implying good A/D and D/A linearity (word length)
- Higher arithmetic processing loads (associated with increased processor bandwidth, scale and functional complexity) – implying the need for low power deep submicron ASIC technology with High Speed Serial Link interfaces

Key Technology Needs for Future Processors

- Deep submicron ASIC technology
  - Multi-Mgate deep sub-micron rad hard ASIC technology
  - Low voltage and power
  - HSSL interfaces
- A/D and D/A converter technology
  - Higher speed
  - Long effective word length
  - Low power
- HSSL:IP development
  - Required for ASICs and MS converters
- European sourcing of technology needed to avoid ITAR constraints
- High cost of technology and component developments suggests a European wide approach

Electrical HSSL requirements

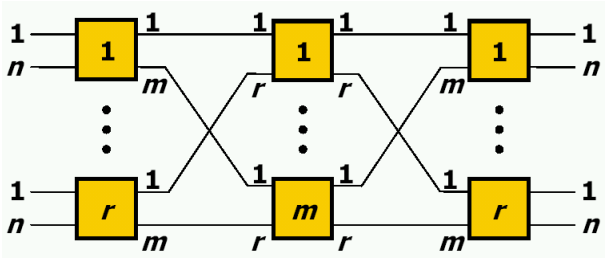
- **Functional performance …**
  - Bit rate:
    - Variable
    - More than 10 Gbps/lane (a 2 GSPS 14 bit ADC produces 28 Gbps in raw data, and up to 35 Gbps clock-encoded data)
  - Clock encoding:
    - More efficient than 8b/10b
  - Bit error ratio:
    - Better than $1:10^9$
  - Power consumption:
    - Up to 100 mW/lane
    - Optimised for scaling with bit rate
  - Static performance:
    - Minimum and well characterised BOL-to-EOL drifts
- **Electrical interface …**
  - Analogue output signal/s:
    - Differential format
    - Well-behaved output impedance
    - Tolerant to open/short/back-drive
  - Encode clock signal:
    - Differential format
    - Wide bandwidth and low additional aperture jitter – target < 300 fs rms
  - Digital input signals:
    - Support for HSSL and parallel DMUXed differential formats
  - Power supplies:
    - Minimum number and level consistent with required dynamic range
  - Mode control & Test signals
- **Timing interface …**
    - Deterministic latency at power-up
    - Deterministic performance post-SEE
- **Mechanical interface …**
    - Packaging options: single, dual, multi-, flip-chip

Complexity of the Clos Network

- **The next generation of OBPs implement a modified Clos network at their centre.**

- **For a network serving N user ports symmetrically, with n user ports per MUX/DeMUX block, with r MUX/DeMUX blocks and m ROUTER blocks respectively:**
  - Noting that N = nr, and with m = 2n – 1, for a minimum size non-blocking network,
  - Number of cross-points, $C_N = 2mnr + mr^2$,
  - or $C_N = N^2(2/n – 1/n^2) + 2N(2n – 1)$, and
  - Number of interconnects, $C_I = 2nr + 2mr$,
  - or $C_I = 2N(3 – 1/n)$

- **Overall cost depends critically on the relative cost of a cross-point to a wiring connection.**



User ports N	Cross-points C_N min	Interconnects C_I
10	120	40
20	440	80
50	1800	280
100	5400	560
200	15200	1160

Complexity of candidate architectures (1)

- This candidate features medium bandwidth and fine granularity.
- Most relevant to the next generation of mobile missions.
- The rapid growth of the interconnect complexity with feeder link bandwidth is the greater packaging challenge, than the relatively modest scale of ASIC complexity required to fulfil this class of mission.

- The functional density imposes a severe demand on the interconnect density required of any proposed packaging system.

Feeder Link B/W (MHz)	Beam Port B/W (MHz)	Number of Beam Ports	Number of DeMUX ASICs	Number of TDMs DeMUX -> ROUTERs	Number of BFN/ROUTER ASICs	Number of MUX ASICs	Number of TDMs ROUTERs -> MUX	Number of AFR Ports	Total Number of ASICs	Total Number of Interconnects
400.000	40.000	*10*	*1*	*40*	*40*	*13*	*520*	*125*	54	695
800.000	40.000	*20*	*2*	*80*	*40*	*25*	*1000*	*250*	67	1350
1200.000	40.000	*30*	*3*	*120*	*80*	*38*	*3040*	*375*	121	3565
1600.000	40.000	*40*	*4*	*160*	*80*	*50*	*4000*	*500*	134	4700
2000.000	40.000	*50*	*5*	*200*	*120*	*63*	*7560*	*625*	188	8435

Complexity of candidate architectures (2)

- This candidate features high bandwidth and fine granularity.
- Described as a flexible option.

- The ratio of feeder bandwidth to the relatively fine router granularity implies that significantly larger numbers of ASICs need to be packaged for this architecture option.

Feeder Link B/W (MHz)	Beam Port B/W (MHz)	Number of Beam Ports	Number of HR DeMUX ASICs	Number of TDMs HR DeMUXs to MR DeMUXs	Number of MR DeMUX ASICs	Number of TDMs MR DeMUXs to ROUTERs	Number of BFN/ROUTER ASICs	Number of TDMs ROUTERs to MR MUXs	Number of MR MUX ASICs	Number of TDMs MR MUXs to HR MUXs	Number of HR MUX ASICs	Number of AFR Ports	Total Number of ASICs	Total Number of TDMs
1000.000	500.000	*2*	*2*	*20*	*2*	*100*	*40*	*1000*	*50*	*500*	*50*	*50*	144	1672
2000.000	500.000	*4*	*4*	*40*	*4*	*200*	*80*	*2000*	*100*	*1000*	*100*	*100*	288	3344
5000.000	500.000	*10*	*10*	*100*	*10*	*500*	*200*	*5000*	*250*	*2500*	*250*	*250*	720	8360

Complexity of candidate architectures (3)

- This candidate features high bandwidth and relatively coarse granularity.
- Described as a broadband option.

- This architecture candidate requires rate-adaptation ASICs. HSSLs could obviate this need.

Feeder Link B/W (MHz)	Beam Port B/W (MHz)	Number of Beam Ports	Number of HR DeMUX ASICs	Number of TDMs HR DeMUXs to De-INTs	Number of De-INT ASICs	Number of TDMs De-INTs to ROUTERs	Number of BFN/ROUTER ASICs	Number of TDMs ROUTERs to INTs	Number of INT ASICs	Number of TDMs INTs to HR MUXs	Number of HR MUX ASICs	Number of AFR Ports	Total Number of ASICs	Total Number of TDMs
1000.000	500.000	*2*	*2*	*20*	*2*	*100*	*4*	*100*	*50*	*500*	*50*	*50*	108	772
2000.000	500.000	*4*	*4*	*40*	*4*	*200*	*8*	*200*	*100*	*1000*	*100*	*100*	216	1544
5000.000	500.000	*10*	*10*	*100*	*10*	*500*	*20*	*500*	*250*	*2500*	*250*	*250*	540	3860

Concluding remarks

- **This presentation has shown the expected rapid growth of the interconnect cost, within an OBP based on the Clos network.**
- **This complexity is driven by the expected size of the processed bandwidth as well as by the computational density being offered in the next generation of digital ASICs.**
- **In general the interconnects fall into 2 categories, described as inter-box and intra-box.**
  - The former need to carry the full beam port B/W, but visit only the perimeter of the DSP, having spanned distances of the order of 1 m.
  - The second category, in general much more numerous, provide the point-to-point ASIC-rank to ASIC-rank interconnect fabric and carry only a fraction of a beam port B/W. Their physical extent is of the order of several tens of cm.
- **The current focus at EADS Astrium is to realise these links electrically.**

- **Can viable optical alternatives be described and built?**