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Micro- and Nano-spacecraft as Experimental Testbeds to Raise Technology Readiness Levels.

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Overview

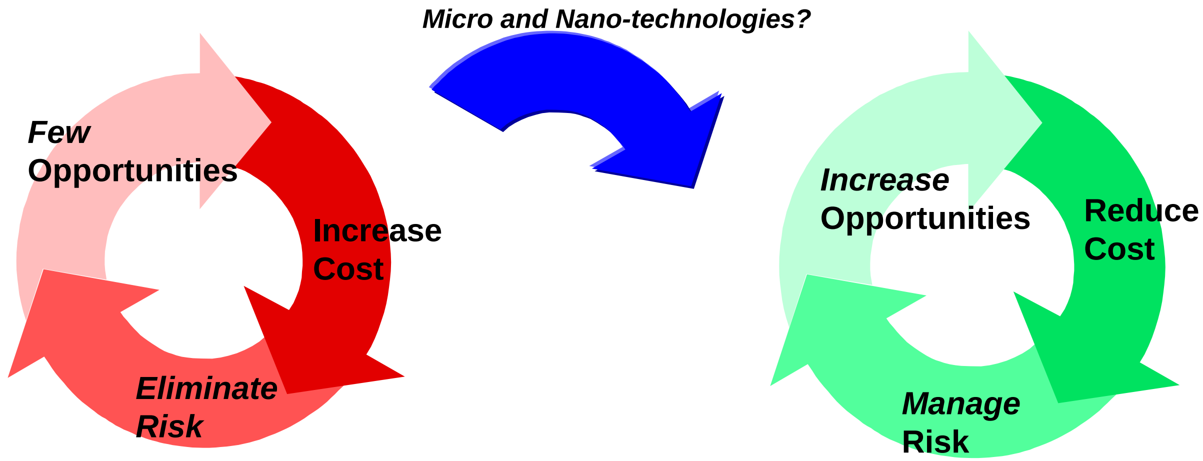
- The problem:
  - New technologies with little or no space heritage pose unacceptable risk to costly spacecraft and tend not to be flown.
  - This is acutely the case for micro technologies
  - The *'TRL gap'* problem

- An opportunity:
  - An increasing range of microtechnology devices developed for large terrestrial markets offers attractive advantages

- A possible solution:
  - Why a European consortium?
  - The case for microspace
  - Using small low cost spacecraft as test-beds
    - To increase the Technology Readiness Levels (TRL) of MEMS, MST and other micro devices in space
    - Challenges to this strategy and potential solutions

Hypothesis

Small cost-effective spacecraft can fly more frequently and are ideally placed to accept higher risk to demonstrate new technologies.



Vicious circle?

Virtuous Circle!

SSTL's preferred model !

We challenge the conventional definition of 'space-qualified' parts by testing MEMS components alongside existing heritage subsystems in small spacecraft missions, providing heritage by experience without the need for time consuming and costly qualification programmes.

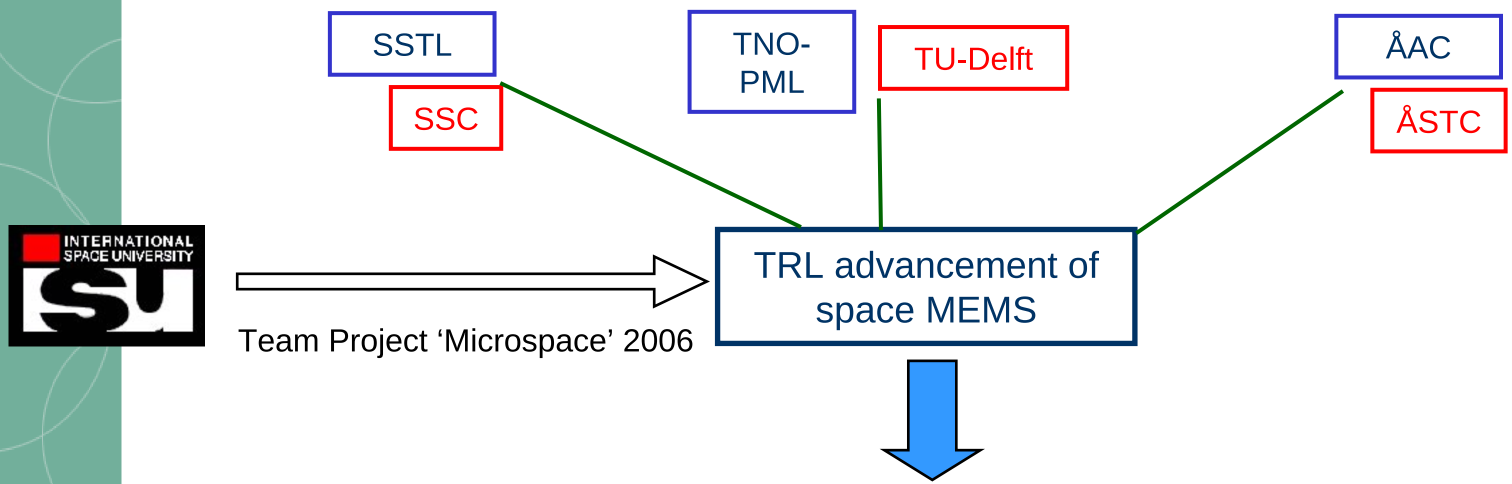
Why ‘micro’ for space?

- MEMS devices are complementary to any spacecraft customer, being inherently…
  – Small
  – Low mass and power,
    - Note also vibration tolerance due to lower inertia
- Microdevices are ideal for the small spacecraft customer, because…
  – They are batch processable to high quality standards.
  – They allow integration of all components into one system (less or no wiring, piping etc.)
  – The whole system can be made in one production process
- COTS products are also moving towards microsystems
- Moores law indicates that microprocessor size, hence capability per unit volume / mass will continue to improve. Space is a demanding environment and therefore requires high performance

Benefits of a European consortium

The best blend of expertise to advance MEMS TRLs

- Universities: low cost low risk development of new concepts. *However not necessarily responsive to customer timescales, nor willing to deal with PA/QA*
- Industry: Rapid turnaround, QA/PA and flight testing, *but not as able to adapt to and develop new ideas*
- Organisation with spaceflight heritage: understands process of making terrestrial components ‘fit’ for spaceflight and has demonstrated capability



Faster: ability to develop new platform solutions to meet missions needs from a series of standard modules, using Product Life Cycle Management Software

Cheaper: more rapid development timescales, ability to use external (MEMS house) contractors, lower launch costs

Better: higher performance and / or redundancy for similar mass, volume, power

And….Entirely new missions enabled

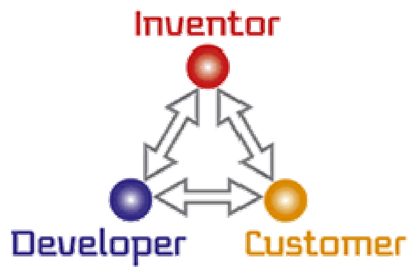
New missions?

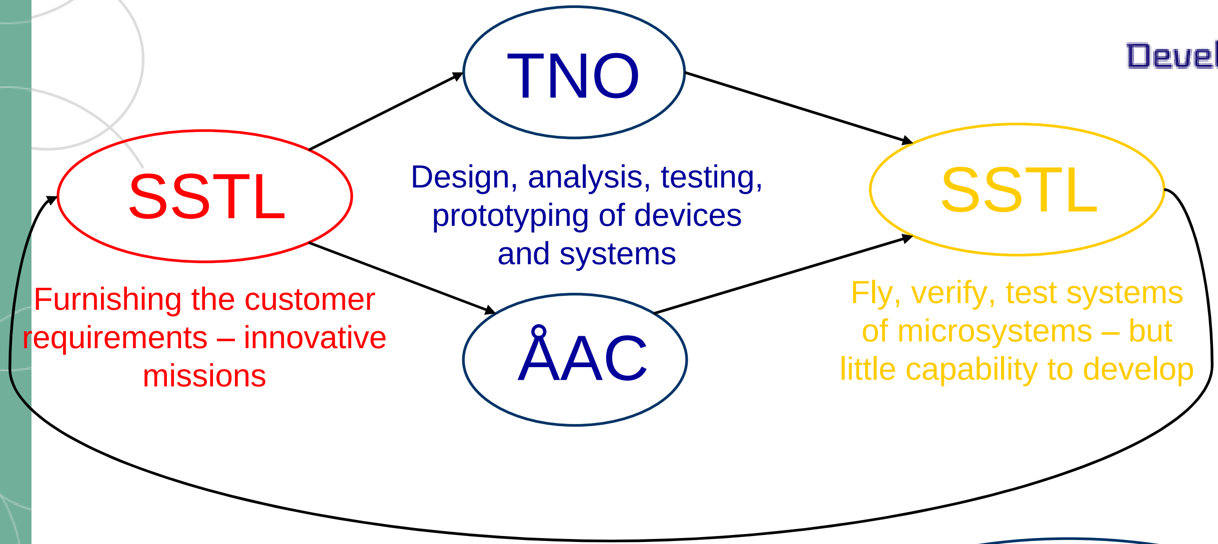
- Communications
  - E.g. relay
- Imaging / Remote sensing / Earth Observation
  - ELINT (RF monitoring of wide area e.g. battlefield)
  - EO in the visible spectrum
- Rendezvous (docking, servicing, denial of coverage, etc.)
  - Spacecraft inspection
- Science & Exploration
  - Upper atmosphere (50-250km) sounding – Earth
  - Atmosphere sounding – Venus, Titan, Jupiter, etc.

- Technology testing / demonstration
  - Heritage improvement
  - Requirements testing and development
    - E.g. spatial resolution v. spectral v. radiometric resolution for tactical applications
  - Systems (of microsystems) and clusters

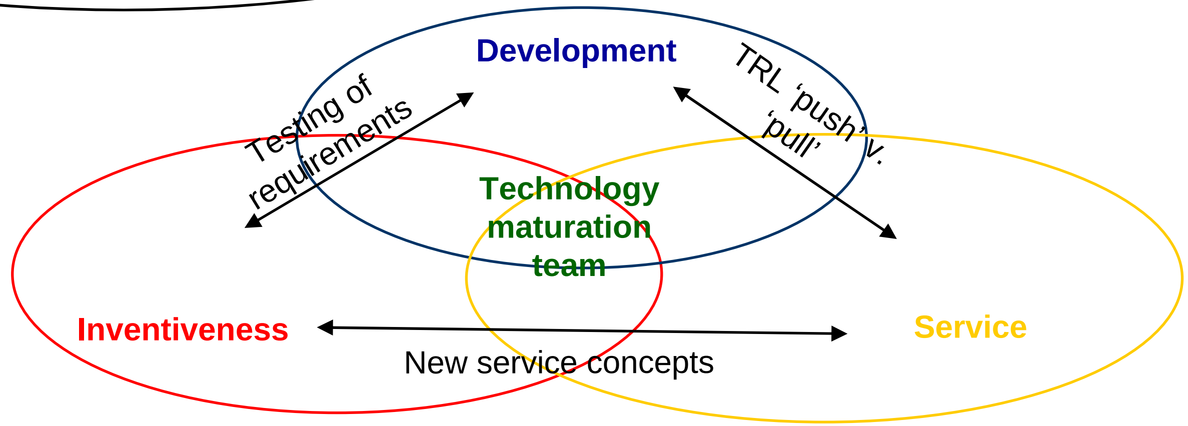
Consortium benefits (cont.)

ESA's 'Innovation triangle' concept





Continuous technology development pipeline



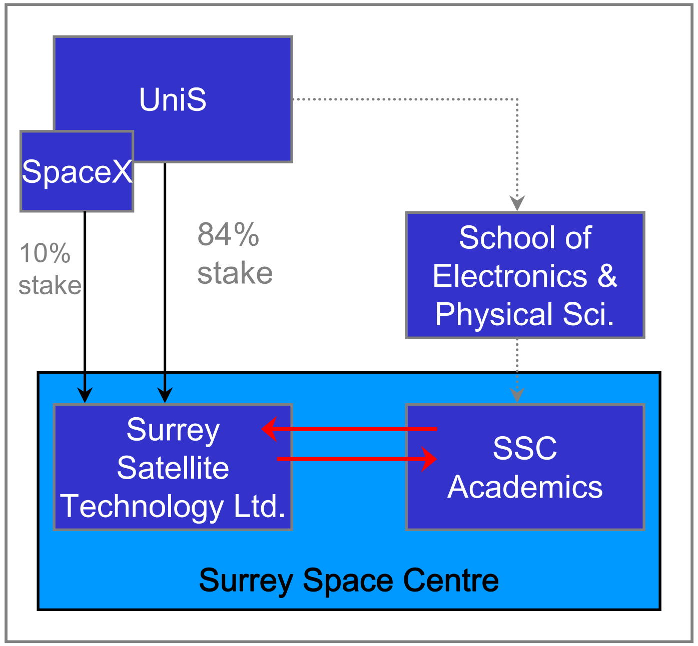
George T, Powers R (JPL) 'Closing the TRL Gap', Aerospace America, August 2003, p. 24-26

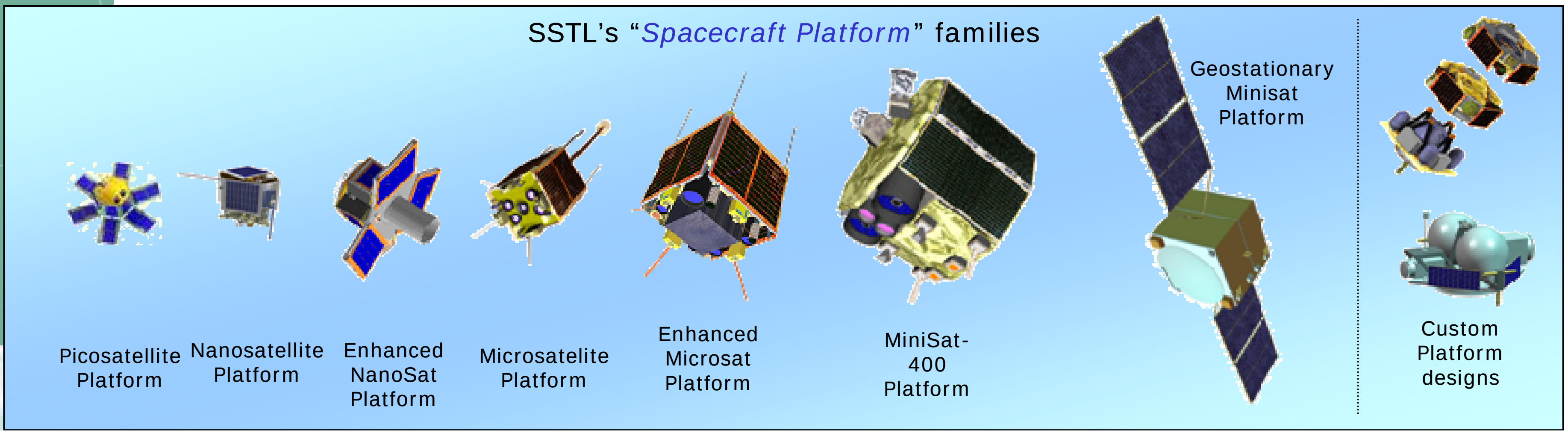
SSTL / Surrey Space Centre

- Formed in 1985
- Circa 220 staff
- Year to July 2004:
  - Turnover £19m (€28m)
  - EBT £1.1m (€1.6m)
- SSC Academic Team
  - School of electronics & physical Sciences
  - 7 Academics
  - 30+ postgraduate researchers

SSC provides long-term R&D to SSTL

SSTL provide flight opportunities to SSC





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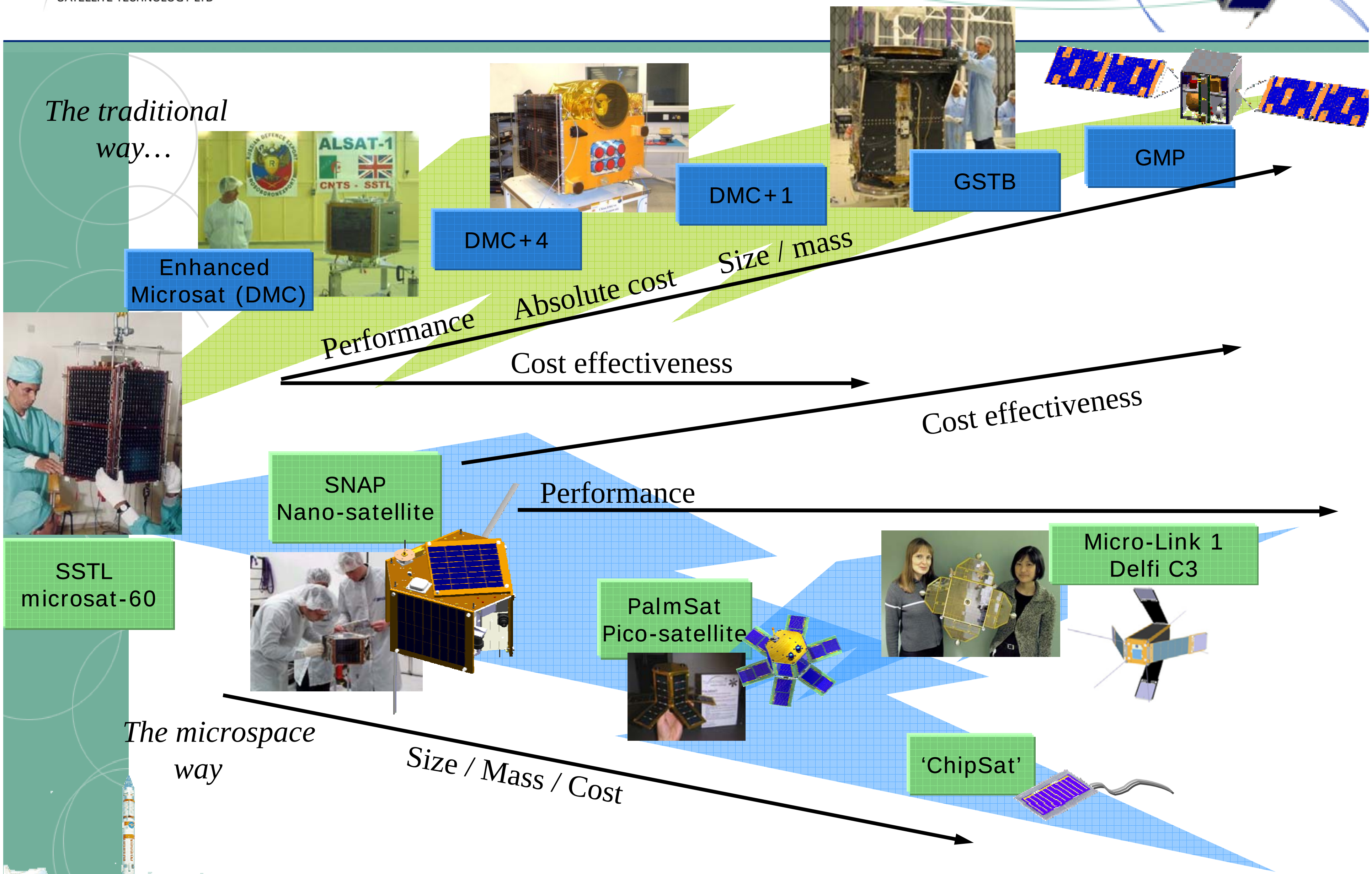
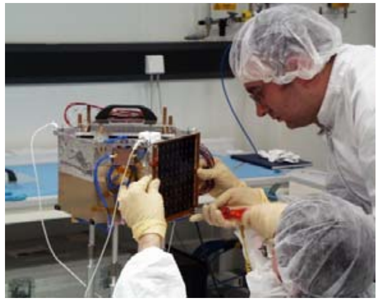
Microsystems based space mission roadmap

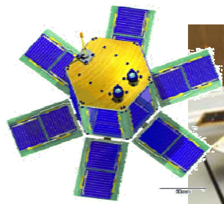


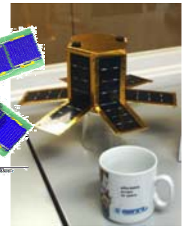
To enable the lower branch, we need to test (raise TRL) of MEMS in space

SNAP to PalmSat

- Drivers
  - Sub-1kg ‘picosatellite’
  - Initially a student group design project
  - Manoeuvrable / stabilised
  - ∆V ~3m/s requirement, Isp 48s (SNAP-1)
  - ‘Add-on’ propulsion module 100g
  - 2004 original target launch date
  - Aiming at SNAP-1 functionality
    - ultra small yet highly capable spacecraft
  - But at <$/€1M, ideally <100k
- Objectives of SSTL *and SSC*
  - Explore the lower limits of conventional technology
  - And fly MEMS components
  - Build the business case for ultra small, <£1M spacecraft
- Evaluate MEMS / conventional hybridisation
  - And reduce mission level risk by flying heritage subsystems (nanotrays) alongside MST







Testing of core subsystems for future highly integrated microspacecraft (and potentially spacecraft-on-a-chip)

- CMOS Imagers / bolometers with miniature lenses
- Useful propulsion on a chip
- Integrated power gen / energy storage
- Data processing / storage
- Low power RF comms
- MEMS Sensors
- Intersatellite links
- Advanced processing techniques

SNAP to Microlink-1

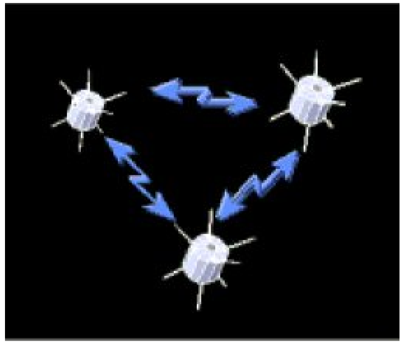
- Largely microsystems based spacecraft
- Overall implementation of MEMS on all levels, from the outer shell and in particular the functional surfaces of all modules.
- An important part of any cost model using MMS is the possibility to batch manufacture the silicon modules. Reduced cost as technology matures and the processing yields improve
- Reduce risk by testing key subsystems earlier (2007) on a Palmsat / TechDemo sat platform
  - Payload space for SSTL partners on a family of dedicated technology demonstration platforms

COMPARISON BETWEEN SSTL SNAP-1 AND NANOSPACE-1 S/C PLATFORM

Function	SNAP-1	NanoSpace-1
Launch	2000	Est. 2008
Mass	6.5 kg	9.9 kg
Battery	5 cell NiCd	16 cell Li-Ion (14.4 V)
S/C Stabilization	3-axis	3-axis (fine pointing)
Thruster technology	Butane Thruster Δv=3.5 m/s	Mono-propellant rocket, Δv=60 m/s Cold Gas Micro Thrusters Δv=35 m/s
Navigation	GPS* MTQ MGN Single momentum wheel, bias in pitch axis only	IMU 2xSun Sensors 2xSun Acquisition Sen. D-GPS MTQ MGN Optical positioning Cold Gas Thrusters
Solar Cell Technology	GaAs	Integrated Si-modules
Communication	VHF, S-band	VHF, 3-way redundant 1 Mbit/s S-band
Visual	CMOS Camera	CMOS Camera (Docking)
Internal Bus	CAN	Dual redundant 1 Mbit/s CAN, 10 Mbit/s SpaceWire (SpW)
OBC	SA1100**	Redunant LEON
Mass Memory	32 Mbit DEDDEC EDAC RAM	20 Gbit EDAC SDRAM
Solar Array Power	5-6W orbit avg	64 W
Battery Cap. (BOL)	10Whr	172 Whr
Powersystem	+12V unreg, +5V reg. Power supply. 4 independent BCRs, single PCM.. Max Power Point tracking.	Redundant +12 V reg, +3.3 V reg busses 4 way redundant PCM, distributed, and load balancing
Payload	CMOS active pixel machine vision system, inc. 3 wide angle, 1 narrow angle cameras Spread spectrum VHF comms payload UHF intersatellite link	3D-Electric Field Vector Sensor. 1 x Langmuir Probe 1 Anisotropic Magnetoresistive Mgn. 1 x Flux Gate Mgn. 2 Booms 4 RF-Antennas High Res. CMOS Camera

‘Chipsat’

- Will explore advanced packaging technologies, validity of further miniaturising the satellite platform.
  - Wafer scale integration, v.
  - Multi-chip modules
- What COTS approaches might we adapt?
  - ‘Motes’ or ‘Smart Dust’
    - Integrated processor, RF in/out, sensor interfaces and power
    - Self configuring sensor networks such as Zigbee, mobile IP
  - Formation flying may not be required but positional knowledge is crucial to reference any data collected
- Wireless harness replacement
  - Mass reduction
  - AIT time, cost reduction



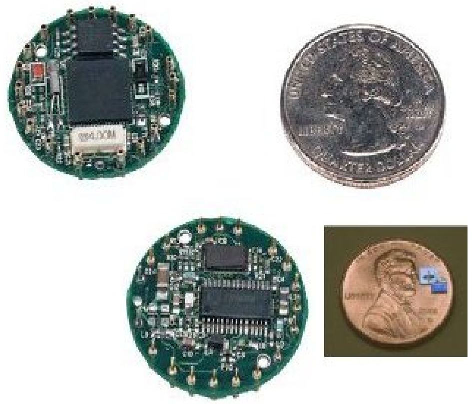


Figure 4: Current mote size compared with 'smart dust' (inset)

Images courtesy UC Berkeley, BSAC

Challenges

1. Determining whether the apparent benefits of MST (mass production) are really valid in the context of spacecraft context
   - *Need to fly numerous microsystems to verify this*
2. System level testing of integrated microsystems
   - *And making modifications at wafer batch level at low cost / short times*
3. Overcoming the TRL gap (inertia towards flying new technologies)
4. Finding appropriate launch opportunities, and developing miniature upper stages to access useful orbits
5. Evaluating and testing the business case for ‘swarms’ of spacecraft
6. Addressing the potential debris issue of ‘swarms’
7. Maximising modularity,
   - *Standard physical and electrical interfaces, onboard data handling*
8. Understanding the processes which can rapidly manufacture highly configurable small, cost effective spacecraft
9. Building a secure working relationship between spacecraft integrators and device or component suppliers such that batch quality acceptance does not compromise in-space performance.
   - *This is a major concern where space microsystems are derived from terrestrial production lines.*

Summary and roadmap