High Sensitivity Piezoresistive Silicon Microphone for Aerospace Applications

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INTRODUCTION

Process technology used in silicon micromachining to fabricate MEMS has reached an excellent level of process control in different families of physical sensors. Recently, this potential of improved reproducibility and miniaturization has also been exploited in the development of microphone technologies for various applications. Some of the innovative MEMS microphone designs use ultra thin membranes [1] to convert pressure sound waves to electrical energy.

In this paper we present an alternative approach to the capacitive transducer that consists of using a piezoresistive silicon microphone to convert acoustic energy to mechanical strain energy by bending the diaphragm. The advantage of using this technology is the elimination of signal variations due to humidity, the absence of bias circuitry, and robustness and simplicity of the fabrication process.

The fabrication process was derived from the process we normally used in the production of low pressure sensors for aerospace applications. Some modification has been performed in the post processing steps in order to optimise the mechanical structure of the thin membrane.

After packaging, the devices were characterized in terms of linearity, frequency response and power consumption. The influence of the geometrical dimensions of the membrane on the sensor sensitivity was also studied. A sensitivity of 50 microV/Pa·V has been achieved.

DESIGN AND SIMULATION

The microsystem consists of four dielectrically-isolated, silicon piezoresistors mounted in a Wheatstone bridge configuration. The piezoresistors are deposited on a 100 nm thick thermal oxide on the top of an SOI wafer in order to achieve complete electrical insulation. The physical principle is shown in Fig. 1.

The mechanical waves are transformed into an electrical signal by the silicon piezoresistor placed on the membrane in such a way as to maximise the signal.

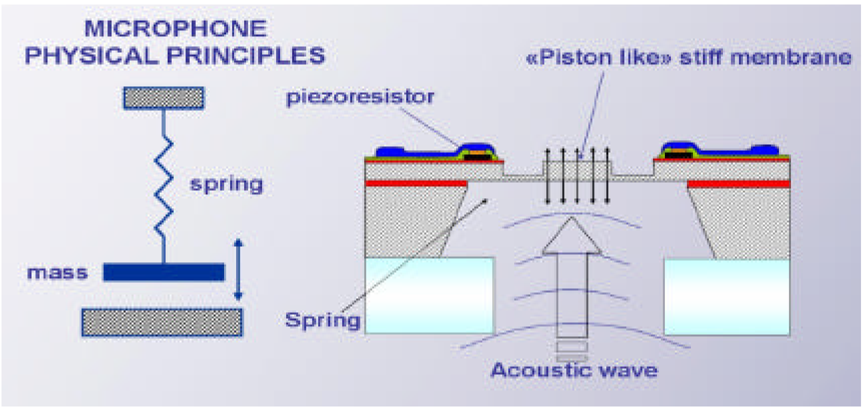

Fig.1 Device cross section.

The mechanical stress produced by the deformation of the membrane is converted to a resistance change by the piezoresistive effect. The relative resistance change can be related to the mechanical stress by the following expression [2]:

$$\Delta R/R = \Sigma \pi_i \sigma_i \qquad (1)$$

where σi are the stress and πi are the piezoresistive coefficients along the *i* direction. When the resistors are in polycrystalline silicon, the isotropy of the material gives a resistance variation completely independent of the orientation of the resistors. A positive stress causes a positive variation of resistance; a negative stress causes a negative variation of resistance. In the Wheatstone bridge configuration (Fig. 2) only two resistors Rm are placed on the membrane (where stress is positive) while the other two are placed outside the membrane where we can assume there is no stress contribution.

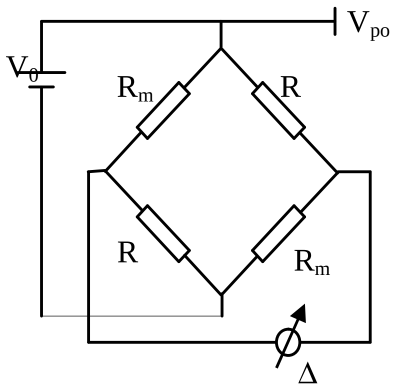

Fig.2 Wheatstone bridge resistor configuration

With no pressure applied, the bridge is balanced and the output voltage will be zero. As the membrane bends under a pressure load, a stress is induced and the resistance of the two resistors R_m placed on the active area increases according to equation (1). The voltage difference at the output nodes of the bridge will be:

$$\Delta V = V0 \cdot \Delta R_m/R \qquad (2)$$

where $\Delta R_m/R$ is the relative resistance change and V_0 is the bias voltage. The pressure sensitivity S of the device is therefore defined as:

$$S = \Delta V/ (\Delta P \cdot V_0) = \Delta R_m/R\ (1/V_0) \qquad (3)$$

A special configuration of the membrane has been designed to minimize the mechanical instability of the resistor and at the same time to increase its sensitivity to the applied pressure. The idea consists of designing a membrane weak enough to allow a larger deflection at its central zone. The central zone is circular and its thickness is greater (2-3 times) compared to the thinner area. Two cantilevers are designed to mechanically connect the central part to the edge of the membrane (Fig. 3).

The software package ANSYS, based on the finite element method (FEM), has been used to calculate the stress distribution on the membrane in order to provide information for the proper location of the piezoresistors.

Different designs have been simulated and made in order to study the influence of the geometrical parameters on piezoresistor sensitivity and on mechanical stability.

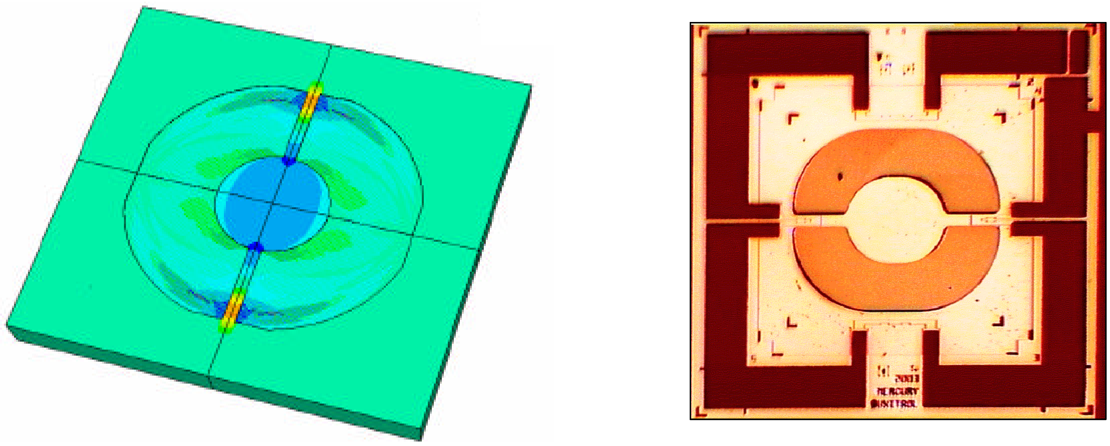

Fig.3 Simulation of the stress map by ANSYS (on the left) and design of the complete chip (on the right).

The piezoresistors are deposited on the cantilevers close to the edge of the membrane, where the stress is higher. The thickness of the cantilevers allows a distribution of the maximum stress over a larger area (compared to the stress distribution of a membrane with a constant thickness).

FABRICATION PROCESS DESCRIPTION

For the fabrication process we used SOI silicon wafers with a diameter of 100 mm and a thickness of 525 µm. The thickness of SOI is 5 microns; the thickness of silicon oxide for insulation is 400nm.

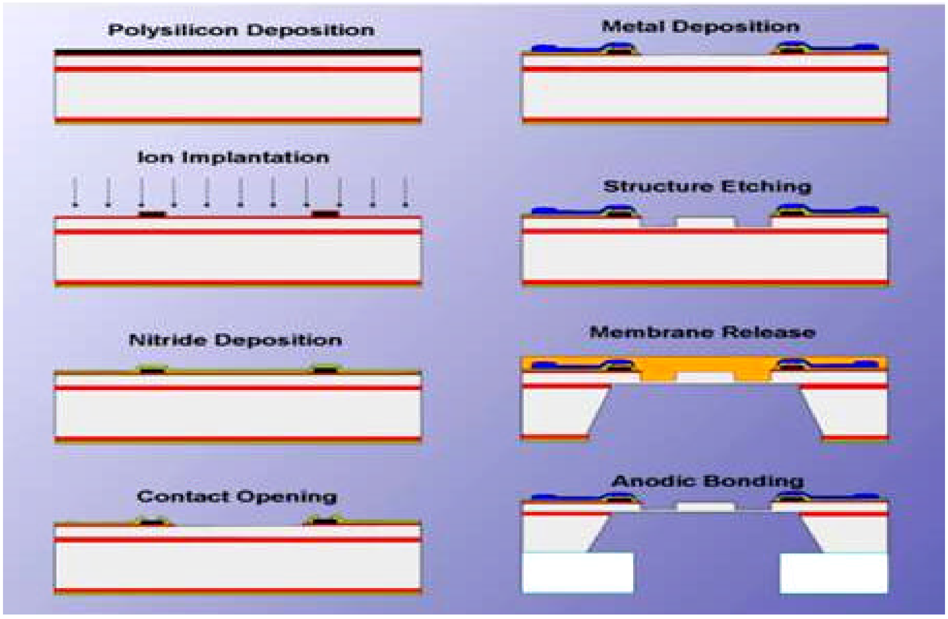

Fig.4 Main fabrication process steps.

A 7-mask process has been developed and is schematically illustrated in Fig. 4. The SOI wafers are cleaned and a screen oxide (100 nm) is grown at 1000°C in pure oxygen. Then a succession of LPCVD polysilicon deposition, resistor lithography and ion implantation step is performed to define and to dope the *p* resistors. To electrically insulate the device, a 50 nm thick thermal oxide layer is grown and a 100 nm thick LPCVD silicon nitride are deposited. A mask to define the anodic bonding tracks is patterned. At this point the contact holes are opened and a 600 nm TiW/Aluminium metallization coating is sputtered and patterned. The front side of the wafer is etched in order to define the 3D structures on the membrane (Fig. 5). The etching windows to define the membrane size are patterned and opened on the backside masking layers. A timed anisotropic etching forms the membranes. The sensing membranes are etched in (100)-oriented silicon by anisotropic etching using a KOH water solution. Finally the wafers are diced and the sensors chips are packaged for testing.

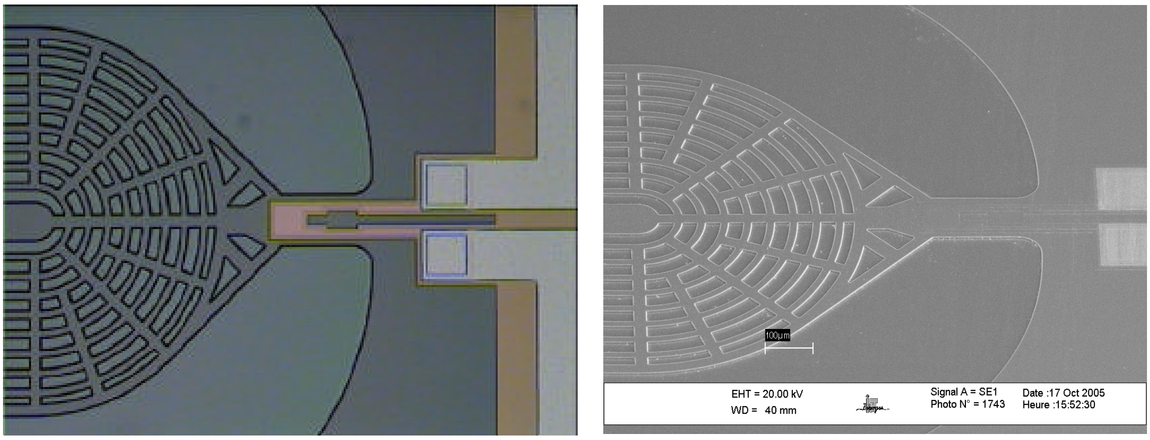

Fig.5 Optical and SEM photographs of a piezoresistor on the cantilever structure after fabrication process.

RESULTS

The characterisation of microphone frequency (less than 50 Hz) requires special testing equipment. For this reason a dedicated testing tool has been designed. This tool is based on a volume variation principle in order to generate the required small pressure variations by using a PTZ ceramic under an applied sinusoidal voltage at a frequency of 30 Hz.

A complete set of characterisation curves of the microphone devices has been made. The results obtained in terms of output voltage ΔV of the Wheatstone bridge and sensitivity as a function of the pressure are shown in Fig. 6. The measurements have been repeated several times over the same range of applied pressure. The results of the continuously repetitive tests show the absence of hysteresis effects for all the different thickness of the tested membranes. The influence of the geometrical dimensions of the membrane on the sensor sensitivity was also studied. A sensitivity of 50 microV/Pa·V has been achieved. The frequency response for all the microphones with different design is flat from 3 Hz to 600 Hz.

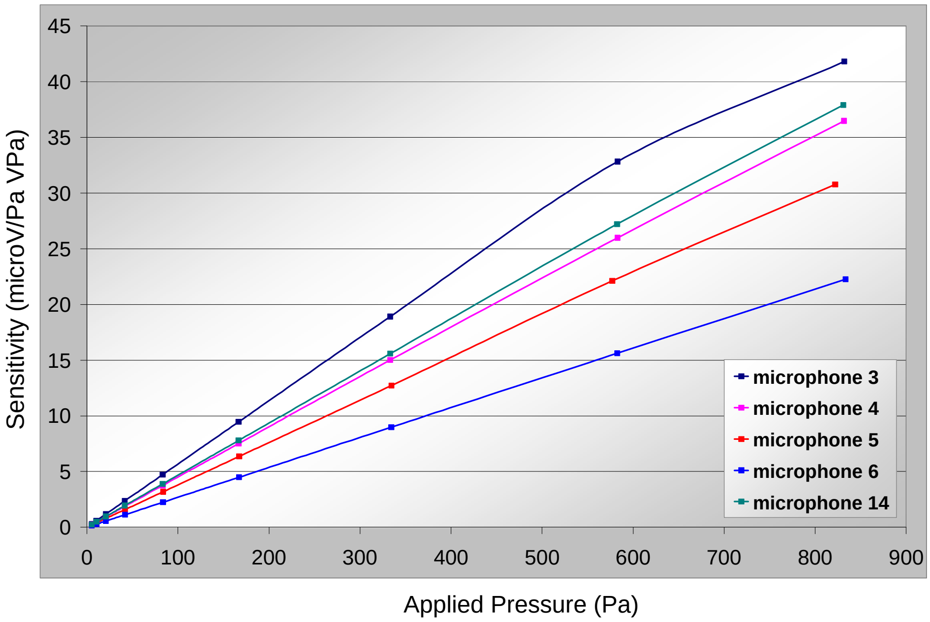

Fig.6 Measured potential as a function of applied pressure for different membrane thickness.

CONCLUSIONS

A fabrication process for the realisation of silicon piezoresistive microphones has been developed. The process includes a dedicated micromachining module for the manufacture a 3D membrane to increase the sensor sensitivity. The encouraging preliminary results obtained in terms of sensitivity demonstrate the feasibility of the technological process for piezoresistive microphones and are the starting point for the future engineering of sensors aimed to specific applications.

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