RF-MEMS Based Switch Matrices for Complex Switching Networks

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INTRODUCTION

This paper presents the results of the work carried out in the frame of the ESA contract Nr.14628/NL/CK on "micromachined devices for on-board applications". The aim is the development of a miniaturised switching matrix using micro-machining technology on silicon wafers. Shunt-capacitive and series-ohmic air-bridge micro-electro-mechanical (MEM) switches have been developed and tested. They have been used as a building block for more complicated configurations: (i) Single Pole Double Throw (SPDT) switches as intermediate devices, and (ii) switching matrices as the final solution for signal routing. Several configurations fabricated and recently tested are presented and compared. Their fabrication process is described and their measured RF-performances are reported and discussed. The construction of complicated switching networks starting from the developed devices is addressed as well.

FABRICATION PROCESS

The eight mask fabrication process developed for the fabrication of RF-MEMS switches, outlined in Fig.1, is based on surface micromachining techniques and standard CMOS type technologies. The process provides together with the movable Au bridge structures integrated high resistive poly-silicon actuation pads and optional high value resistors and DC blocking capacitors. The air-bridges and movable bridges are realized without the need of a planarization step, utilizing two electrodeposited gold layers of different thickness which are also used for the realization of the co-planar waveguides. A third gold layer is used for the realization of low resistance metal-to-metal electromechanic contacts for series ohmic switches and floating electrodes for shunt switches. The devices are fabricated on p-type, <100>, 525µm thick, 5 kΩcm high resistivity silicon FZ 4" wafers (Wacker). (a) As a first step a 1000nm thick thermal oxide is grown as an isolation layer. In order to reduce the fixed oxide charge the oxide is then annealed at 975˚C in nitrogen for one hour. Next a 630 nm thick un-doped poly-silicon layer is deposited by LPCVD at 620˚C and slightly doped with Boron by ion implantation (BF2 120 keV 6.2×10^{14} atoms/cm^2). At this point the resistors and actuation electrodes are defined. The poly-silicon layer is selectively etched by a plasma etch process and the previous implanted Boron is diffused at 925˚C for 1 hour in nitrogen, which provides a final sheet resistance for the poly-silicon of 1300 Ω□. Next a 300 nm thick silicon oxide layer is deposited from TEOS at 718˚C by a LPCVD process that provides the high isolation needed for the actuation electrodes. Contact holes are then defined and etched by a plasma process. (b) After photo mask ashing, the multilayer underpass metal is deposited by sputtering. First 30nm of Ti and 50 nm thick TiN are deposited at 400˚C. Next a 450nm thick Al 1%Si alloy and 30 nm thick Ti layers are deposited at room temperature. Finally an 80 nm thick capping layer of TiN is deposited at 300˚C to obtain a diffusion barrier between metal and gold. The total thickness of the multilayer was calculated in order to have the same height of the polysilicon, compensating the change of oxide thickness do to dry etching too. This metallization scheme provides together a high conductive metal layer and

a diffusion barrier for gold. Multilayer metal is then defined and etched. (c) The multilayer is covered with 100 nm of low temperature oxide (LTO). The via's in the LTO are defined by masking and dry etching. The etch time is calculated in order to remove the TiN capping of the multilayer metal and to expose the underlying aluminium layer. Immediately before the metallization steps the wafers undergo a via's cleaning step based either on a dip in TI-etch or Aluminum etch (cold). Next a 5 nm thick Chromium adhesion layer followed by a 150 nm Gold layer are deposited by PVD. This Cr/Au layer is defined by lithography and etched wet. Main purpose of this layer is to cover with a noble metal the exposed electrical contacts of the series ohmic switches in order to provide low resistive electrical contacts. This layer can also be used to build a floating electrode for the shunt switches. (d) The sacrificial layer for the definition of the air gap is formed by 3 µm thick photoresist. As a seed-layer for electrochemical Au deposition a 2.5/50 nm thick Cr/Au layer is deposited by PVD. (e) The movable air bridges are defined using a 4 µm thick positive resist. After an exposure to oxygen plasma at 80 ˚C and a local short etchback of the seedlayer a 2.0 µm thick gold layer is selectively grown in a commercial gold cyanide bath (Aurolyte CN 200 from Atotech). The electroplating parameters have been chosen in order to achieve a uniform thickness and a smooth surface finish. (f) The first plating mask is removed with a solvent and the CPW lines and anchor posts for the movable air bridges are defined with 5 µm thick positive resist. Again the wafers are exposed to oxygen plasma at 80 ˚C and then a 4 µm thick gold layer is selectively grown. The last plating mask and the seed layer are then removed wet. The seedlayer removal is completed by a dip in diluted (1:3) *acqua regia* in order to remove Cr/Au whiskers. At this point a sintering in nitrogen at 190 ˚C for 30 minutes is performed in order to provide the gold layers with the appropriate tensile stress. Optionally the wafers are coated with a 1.2 µm photoresist layer and pre-diced, i.e. with the dicing saw the wafers are diced about half through. This allows handling the wafer still as a whole during the next step while the dies can be easily separated by breaking along the pre-diced scribe-lines. Finally the air bridges are released with a modified plasma ashing process (30 minutes at 200˚C) in order to avoid sticking problems. A typical outcome of the process is shown in Fig.2.

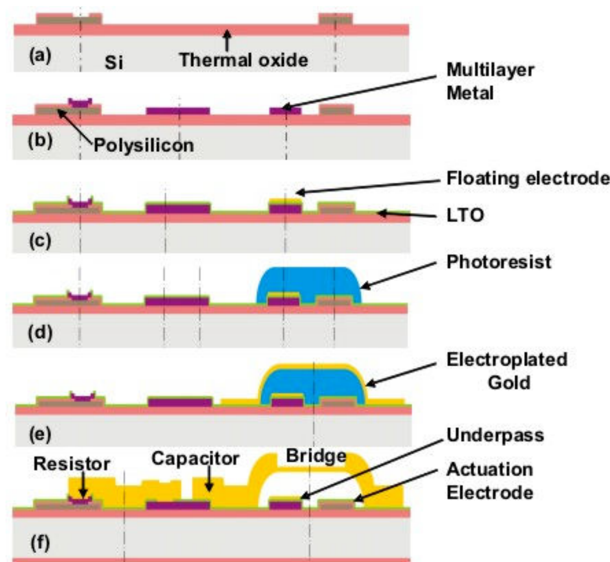
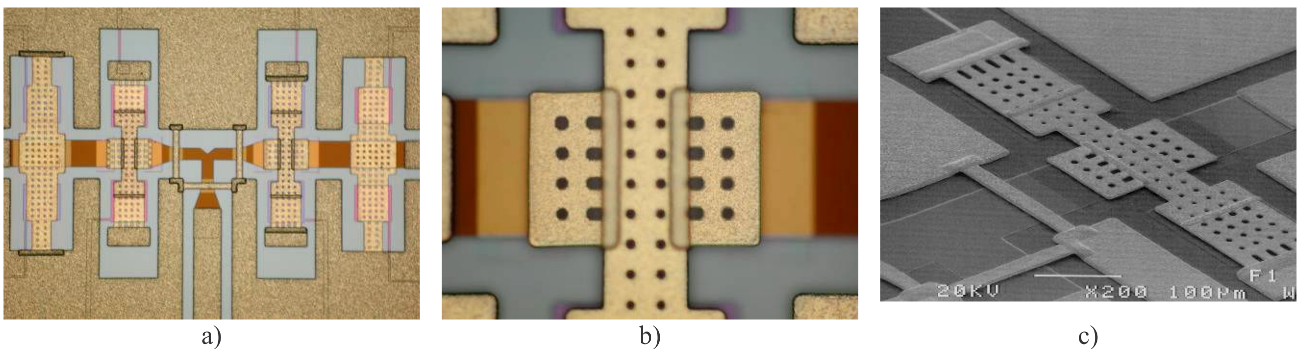


Fig. 1. Schematic fabrication process flow



a) b) c)

Fig. 2 a) SPDT based on the combination of a series ohmic and a capacitive shunt switch. b) Close-up of the mobile part of the series switch with the lateral contact wings. c) SEM picture of the series switch.

CONCEPT OF A SWITCHING MATRIX

The main goal for this research activity was to create a basic module in form of a 2x2 matrix, to be used as a building block for larger matrices. The single module will be packaged, and the connection circuitry will be realised by using a low-temperature-cofired-ceramics technology (LTCC). A mandatory element for the switch matrix is a cross-over with good electrical performances. In the design concept it has to be decided whether to realise the cross-over in an integrated solution with the MEMS switches or to fabricate it as part of the connection circuitry. From simulations it was clearly seen that the realisation of a cross-over in the available MEMS technology would always result in a coupling to the crossing line of at least -20 dB, which is not tolerable for space applications. Therefore the realisation of a crossing within the MEMS module was avoided, instead the ring matrix shown in Fig. 3a, with input and output ports positioned orthogonally each other was proposed. The necessary crossing will instead be realised together with the connecting circuitry in LTCC. A much better isolation can be achieved by routing the signals in different layers using the ground planes of the connecting microstrip lines as additional shielding.

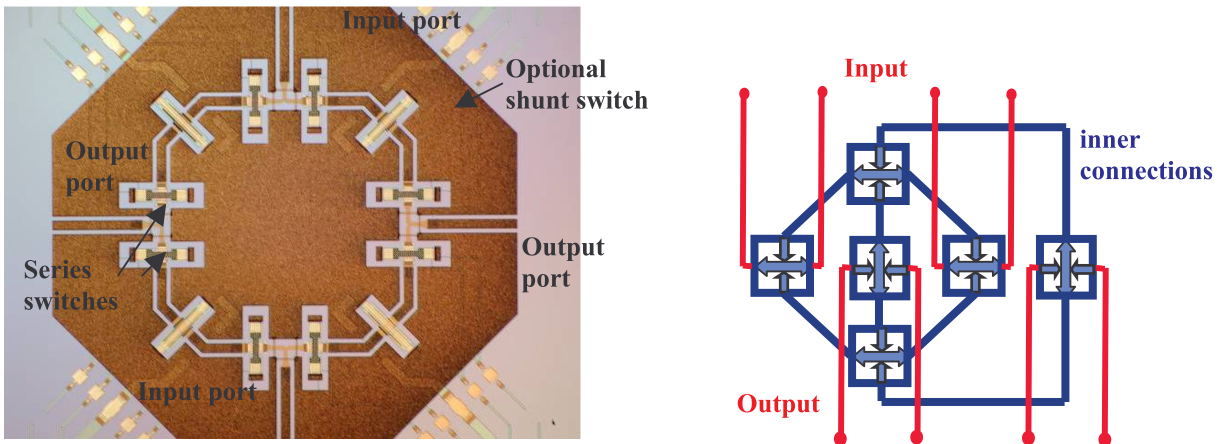


Fig. 3. a) Fabricated ring-matrix with bias pads b) combination of ring-matrices to 4x4 matrix

In what follows, it will be described how a matrix can be designed by using the proposed ring matrix as a building block. One of the most important criteria for a N x N matrix is the symmetry of the transmission paths. The number of used elements should be as low as possible. Moreover, the number of line-crossings should be minimised, as it can drastically decrease the electrical performances by causing unwanted coupling effects.
The best candidate for the realisation of a large switch matrix is therefore the Beneš architecture (see Fig. 4). The Beneš architecture yields a symmetric output, as the path crosses always the same number of switches. This solution can be easily extended to a larger structure, thus giving as a result a re-arrangeable architecture for a non-blocking matrix. Every input can be switched to every output, but switching one input from one output to the other may enforce a re-routing of other connections. Using the ring matrix as a building block for the Beneš architecture, it can easily be realised in an LTCC environment. Three different conductive layers and three different ground planes are necessary. The connection of input and output ports can be realised on the top layer, and the inner connections of the ring matrices can be placed in the first buried layer. A third layer is needed for the DC biasing network. This topology gives a very symmetric response, as in every path the same number of switches and vias is crossed. It is also worth noting that the difference in the length of the various interconnecting lines can be adjusted by meandering the lines (see Fig. 3b).

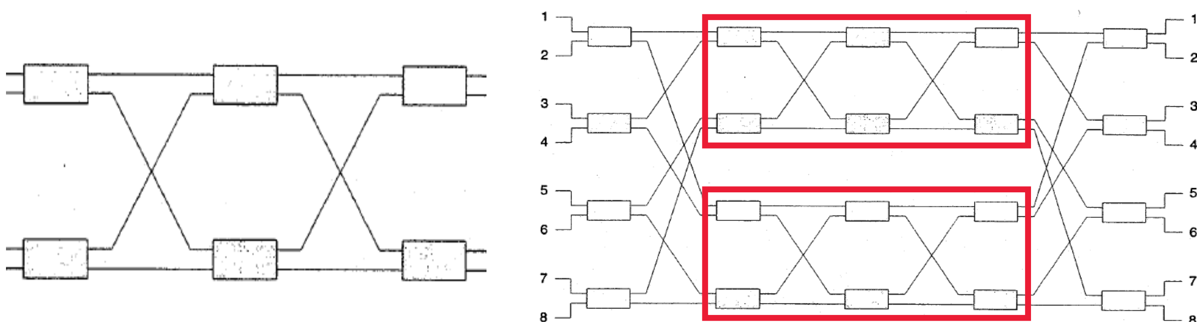


Fig. 4. Beneš architecture a) 4 x 4 matrix b) 8 x 8 matrix

MEM SWITCHES PERFORMANCES

Several MEM switches were developed to be used as building blocks for the switching matrix. They are air-bridge series-ohmic or shunt -capacitive switches as described in [1], and examples of the obtained devices are shown in Fig. 2. A variant of the series configuration was implemented with a floating electrode on the top of the isolation layer, in order to obtain an easy predictable frequency of resonance in the isolation state, as first suggested in [2]. They were characterized as stand-alone devices (see Fig. 5) or in Single Pole Double Throw (SPDT) configurations (see Fig. 6), where the single switches are placed on the arms of a T-junction (see Fig. 2 for an example).

The measured insertion loss on the single switches is comprehensive of the input/output line losses, which contribute by about 0.15 dB @ 20 GHz. The shunt switches overall loss is comparable with such a value, thus confirming the very low loss nature of this kind of switch. The series switch insertion loss is compared to the one measured on an actuated by design version. This means that the spacer was intentionally omitted during the fabrication process, and thus the bridge is melted with the underpass, achieving in this way an almost ideal ohmic contact. As it can be observed the loss difference between the two configurations (the really actuated device and the technologically actuated one) is lower than 0.1 dB, and the increase of the losses with respect to the shunt switches is lower than 0.2 dB, thus showing that a good ohmic contact has been obtained.

Return loss is an important feature in order to use the developed switches in complex configurations. All the single switches have a return loss better than 20 dB up to 40 GHz, and a return loss better than 30 dB up to 30 GHz was obtained by implementing the floating electrode on the shunt switch. Since in the shunt switch with the floating electrode the down state capacitance is not influenced by the bridge dimensions, the latter have been optimized in order to improve the transmission characteristic of the switch. Thanks to the design of an optimized T-junction, a return loss better than 20 dB at least up to 30 GHz is obtained on the SPDT devices.

Comparing the isolation of the shunt switches with and without the floating electrode, its influence is evident. Indeed without it a residual air gap in the actuated state shifts the resonance frequency towards higher values (>40 GHz, while the nominal one is 16 GHz).

If the SPDTs have to be used as stand-alone devices, a series and shunt switch couple shall be used in order to achieve a wide-band isolation. In Fig. 6 the isolation performances of the SPDTs adopting this configuration is shown in both cases, when the shunt switch is actuated and when it is non-actuated (up-state for the bridge). The difference between the two states allows to evaluate the shunt switch contribution. On the other hand, since in the proposed 2x2 matrix configuration every route will crosses two SPDTs, in this case the utilization of a single series switch per arm may be sufficient.

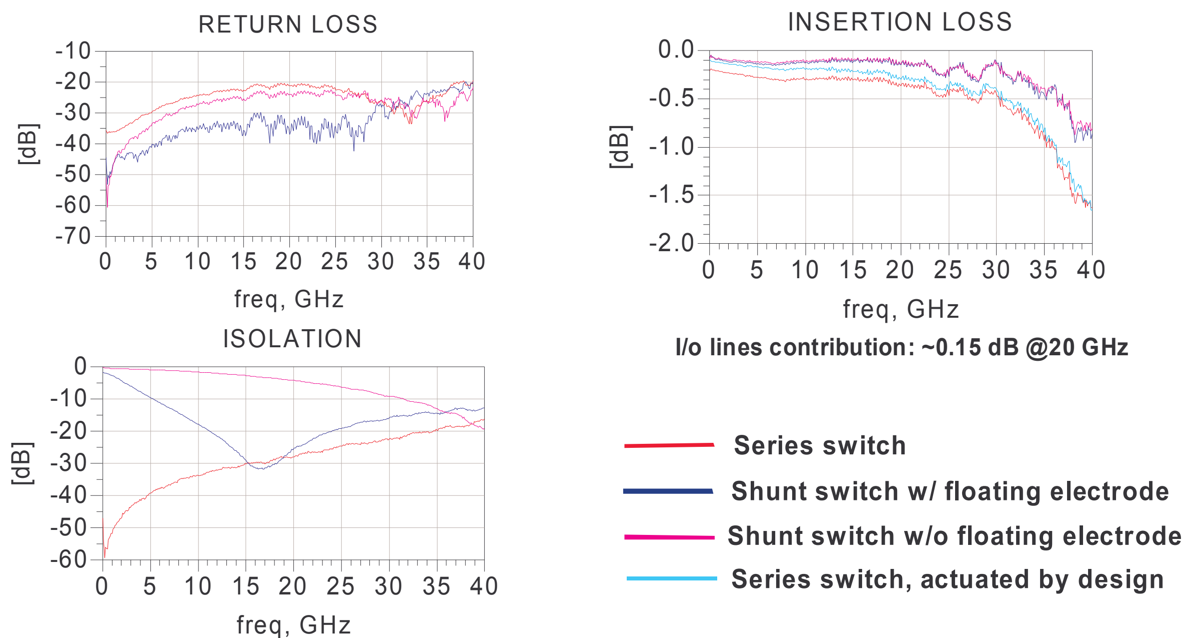


Fig. 5. Single switches RF-performance

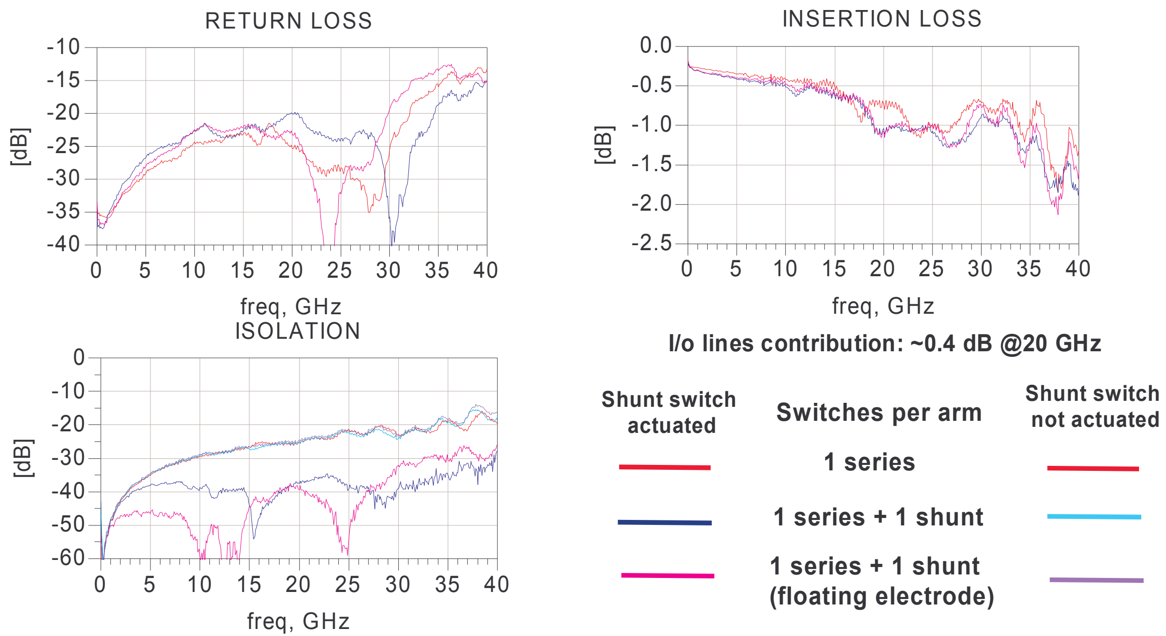


Fig. 6. SPDT switches RF-performances

SWITCHING MATRIX OPTIMIZATION

After an initial survey based on circuital simulations the two inputs- two outputs switching network configuration using SPDTs with only one series switch per arm was evaluated to be the best choice. Electromagnetic simulations were carried out in order to confirm this result and to optimize the switching network dimensions.

At first the distance between the SPDTs was kept as small as possible. After that, the ground plane corners were cut in order to host the actuation pads and minimize the overall area. The electromagnetic simulation evidenced two critical points with this dimensioning (see Fig. 7): a strong interaction between two adjacent switches and relevant border effects due to the ground plane cuts. The simulation was then repeated with an increased distance between the SPDTs (see Fig. 8) and avoiding the ground plane cuts. As it is shown in Fig. 9, this solution not only affects the return loss (because of the different SPDTs impedance combination) but isolation as well. This is due to the reduced SPDTs interaction and border effects, which, in turn, decreases the overall radiation and couplings in the structure. The electromagnetic simulation confirms that with a careful dimensioning and design, the SPDTs with only one switch per arm may provide a satisfying (i.e. better than 40 dB) isolation in the 0-30 GHz band. The insertion loss is expected to be only slightly affected by the distance increase because of the small values of this latter (steps having a length of 200 µm were indeed considered). The M2 matrix dimensioning is expected to provide the best return loss and will keep the overall network area smaller than the M3 one, which only provides a slight isolation improvement. It was thus stated that M2 was the optimised solution.

The electromagnetic simulations allowed not only to estimate coupling, radiation and switches interactions, but to check eventual ground problems as well. Indeed five distinct ground planes are present in the network: an inner one and four external, which correspond to the four corners of the structure. The ground planes are connected by using air bridges placed at the SPDTs T-junctions and at the signal line bends. As evidenced by the simulation, the choice for positioning them allows to keep the ground planes equipotential and do avoid the propagation of the coplanar waveguide odd mode.

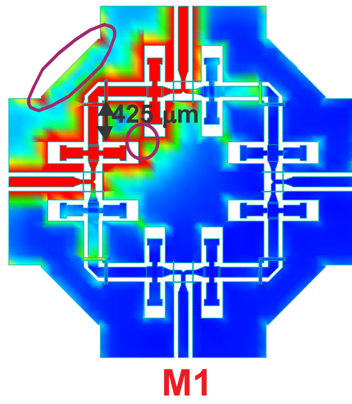
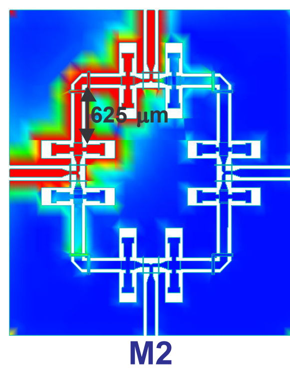


Fig. 7. 2x2 matrix electromagnetic simulation with minimal SPDTs distance



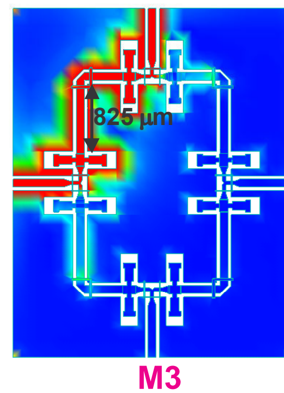


Fig. 8. 2x2 matrix electromagnetic simulations with an increased SPDTs distance

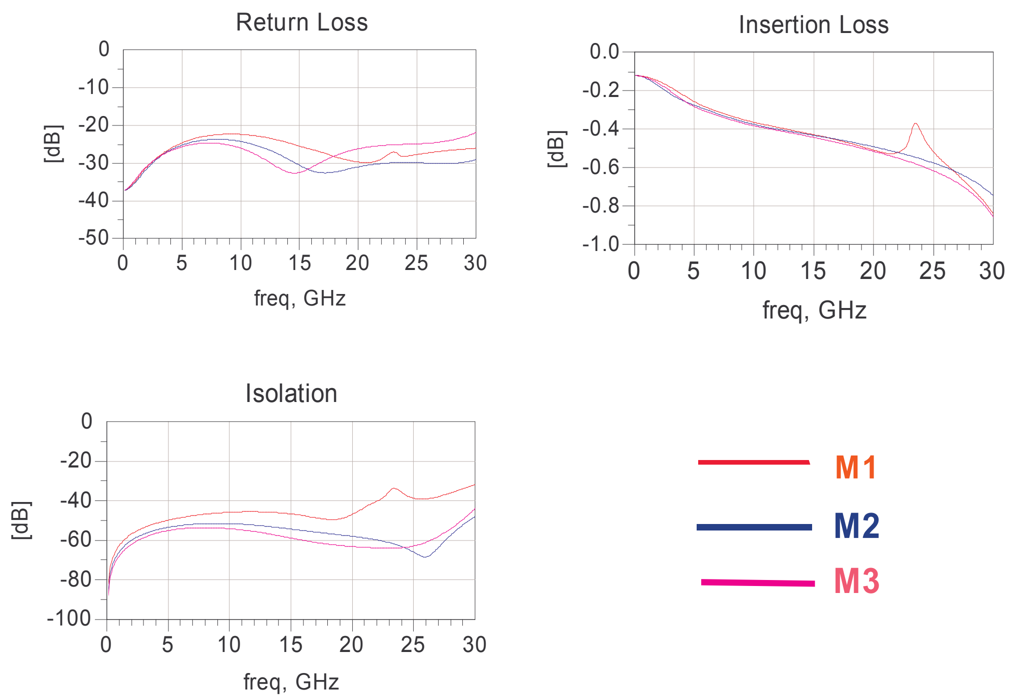


Fig. 9. 2x2 matrix electromagnetic simulations with an increased SPDTs distance

SWITCHING MATRICES PERFORMANCES

Four different 2x2 switching matrices were fabricated. Three of them (A-type in Fig.10) are based on series switches only and have implemented some variations in the dimensions of the slots hosting the bridge and on the distance to the T-junction in order to optimize the return loss. The last 2x2 switching matrix (B-type in Fig.10) employs an additional shunt switch in order to improve the isolation (see Fig. 3a). A reduced cut into the ground planes was implemented in order to allow the dicing of the matrices at the input/output line edges.
A return loss better than 20 dB at least up to 35 GHz, and in one case up to 40 GHz, is obtained on the A-type matrices, while the additional shunt switch do slightly worsen this performance.
The B-type matrix isolation is presented in both states, when the shunt switch is actuated and when the bridge is in the up-position (non-actuated). It may be observed that the difference between the two states is negligible. This is due to the fact that the distance between series switches is greater than in a SPDT. Furthermore, the layout variations needed to host it lead to a an isolation worsening at high frequency. On the contrary, using series switches only a better result on the isolation is obtained (> 40 dB up to 35 GHz).

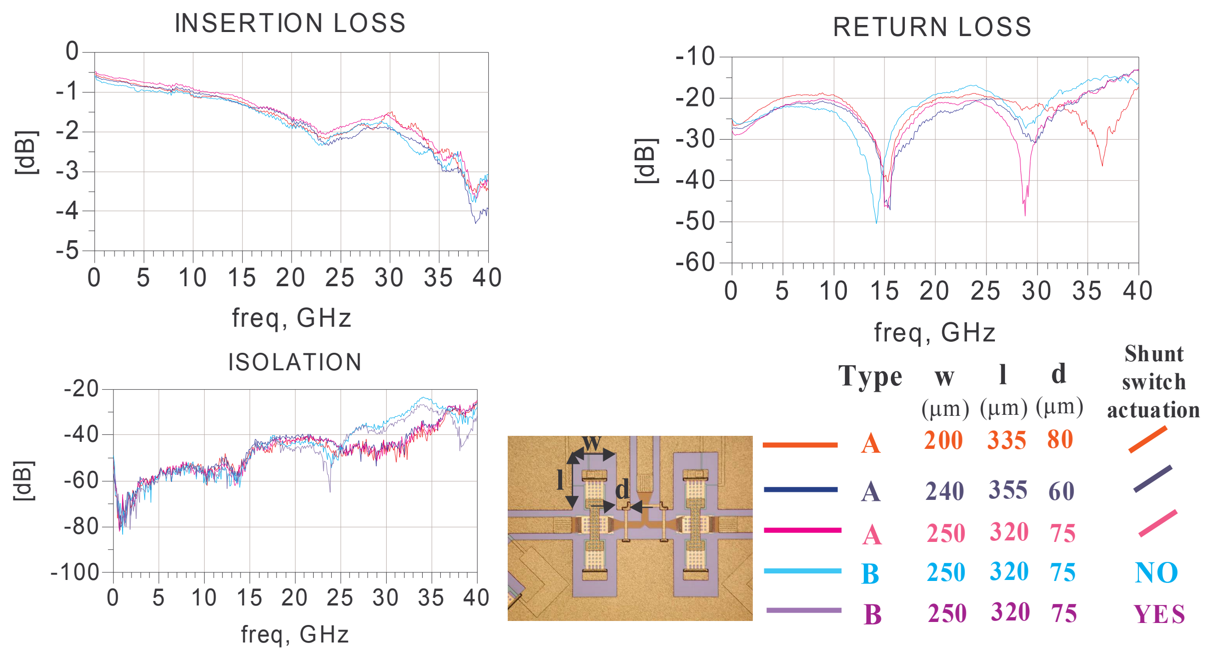


Fig. 10. 2x2 switching matrices performances

CONCLUSIONS

Results about Single Pole Single Throw (SPST) and Single Pole Double Throw (SPDT) MEM switches obtained within an ESA supported activity have been presented. Satisfactory RF-performances, close to the state of art, have been achieved on the exploited configurations.
They have been evaluated as suitable to be used for both, stand-alone devices, or eventually integrated in more complicated configurations for the RF signal routing. In this framework, two inputs-two outputs matrices have been developed starting from the very promising switches obtained until now, and the measured performances make them suitable to be used as building blocks for switching networks with a lot of possible interconnections. For the above reasons, a possible path from single switches towards very complicated switching networks has been proposed.

ACKNOWLEDGEMENTS

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