

# Satellite-on-a-Chip: A Feasibility Study

David J. Barnhart, Tanya Vladimirova, Martin N. Sweeting

*Surrey Space Centre, University of Surrey, Guildford, GU2 7XH, United Kingdom*

*Email: d.barnhart@surrey.ac.uk*

## ABSTRACT

“Satellite-on-a-chip” represents the idea of a completely functional satellite built as a monolithic integrated circuit that can be launched into space to perform a mission while communicating with a ground station. Mission applications, potential payloads, and subsystem architecture concepts are presented while integrating previous path-finding work in these areas. To strengthen the discussion, a first order conceptual design is developed. Concluding remarks are made that suggest the future route to make this space system engineering dream a reality.

## INTRODUCTION

This paper supports the continuing satellite-on-a-chip research at the University of Surrey [1]. The purpose of this paper is twofold: the first is to assess satellite-on-a-chip state of the art and related enabling technologies; the second is to determine the smallest practical and feasible theoretical design for the first satellite-on-a-chip mission.

The satellite-on-a-chip idea is obviously not a new one. The earliest mention dates back to 1994 [2]. Occasionally, the idea is referenced in space news articles as the ultimate goal in miniaturization [3][4]. Two commercial companies have announced that they are developing ideas similar to satellite-on-a-chip, however no published works exist or information is available to validate their progress [5][6]. One related patent exists, but to date none of the technology has flown [7].

There is general agreement among various authors on the classification of small satellites, based on mass [8][9]. Since the launch of Sputnik (84 kg) in 1957 and Explorer 1 (14 kg) in 1958 (both classified as microsattellites), the trend up until the 1990s has been to build increasingly larger satellites to meet complex space mission requirements [10]. Some satellites on orbit today exceed 4,500 kg.

However, due to increased academic, science, and amateur radio interest, there is a recent trend to return to smaller satellites, which is coupled to the rising cost and scarcity of launch opportunities. Dozens of nanosatellite (1-10 kg) missions have flown, with one of the more recent missions being the first to demonstrate earth observation with full attitude control and propulsive station keeping capabilities [11]. Very few picosatellite (0.1-1 kg) missions have flown, with the exception of the Orbiting Picosatellite Activated Launcher (OPAL) mission, where six picosatellites were launched from the host satellite, with two of them tethered to each other [12]. No femtosatellite (10-100 g) missions have flown to date. This is the most logical mass category for satellite-on-a-chip, as revealed in this paper.

The initial scope of this satellite-on-a-chip work is “the smallest possible satellite built as a monolithic integrated circuit that can be launched into space to perform a mission while communicating with a ground station.” This feasibility study reveals that the initial definition will have to change slightly, as discussed throughout the paper.

Some have suggested that satellite-on-a-chip should be an extension of this idea, where high density packaging is used to combine heterogeneous components creating a “system-in-package [18][19].” Others have proposed that entire satellites, including the structure, be fabricated entirely out of silicon, creating a silicon satellite [20][21]. More recently, glass and ceramic materials have been proposed to build spacecraft subsystems for picosatellites [22].

There are many advantages of the satellite-on-a-chip concept. The space segment cost, usually accounting for 75% of total mission costs, is drastically reduced [18]. In addition, the assembly, integration, and test process and launch costs, accounting for 7% of mission cost, are nearly eliminated. Launch costs, at thousands of euro per kilogram to low earth orbit (LEO), are also reduced as one launch vehicle could inject literally thousands of these satellites into their mission orbits. Production schedules are also reduced as the number of component interfaces has been reduced to a single level.

The paper is structured as follows. An analysis of candidate satellite-on-a-chip missions is presented first. With the selected mission in mind, the initial payload and subsystem designs are covered. Concluding remarks summarize the basic design of a satellite-on-a-chip.

## MISSION APPLICATIONS ANALYSIS

Missions, payloads, and orbits are inherently tightly linked in a multidimensional trade space. As stated in [13], “The payload is the combination of hardware and software on the spacecraft that interacts with the subject (the portion of the outside world that the spacecraft is looking at or interacting with) to accomplish the mission objectives.” So what missions would a satellite-on-a-chip be useful for? The basic mission categories are generally classified as communications, navigation, science/exploration, and remote sensing [10]. A brief survey of these mission areas is presented with a discussion for suitable satellite-on-a-chip application.

Communication missions are generally realized by connecting two or more points on the ground using multi-satellite clusters or constellations, which can be of three design types. Near-global coverage (excluding very high latitudes) missions at a reasonable cost utilize a minimum of 3 satellites evenly spaced in geostationary earth orbit (GEO) [14]. Regional and/or high latitude coverage can be obtained with at least two satellites operating in a Molniya orbit [14]. Many amateur radio, communication, and military satellites use this type of orbit. Truly global coverage with no user antenna pointing requirements or significant signal delays can be realized with a large number of satellites operating in a LEO constellation. It has been thought that clusters of small satellites operating in LEO will eventually be used to implement “virtual” satellite missions replacing larger monolithic telecommunication satellites [15]. Another viable proposal is to augment larger satellite missions with a constellation of smaller relay satellites [16].

Current navigation satellites in orbit have a mass of a little over 1,000 kg. Follow on satellites, designed with more RF power to overcoming intentional jamming, are predicted to have a mass of over 1,500 kg [17]. Because of the trend to field more powerful satellites, it is doubtful that a satellite-on-a-chip would ever be able to replace this capability given the current threat environment. Therefore navigation mission applications for satellite-on-a-chip do not seem promising at this time.

Science and exploration missions are so diverse and numerous that an adequate treatment cannot be given here. However, many potential satellite-on-a-chip missions have been proposed, with most of them employing a formation flying or swarm concept. The US National Aeronautics and Space Administration (NASA) has stated generically that the “spacecraft-on-a-chip” is their ultimate goal for widespread interplanetary exploration [23]. Some very good detailed proposals have been envisioned, covering many aspects of interplanetary exploration [24]. Others have proposed experimental missions to measure variations in magnetic fields around a spacecraft, visual inspection of a spacecraft exterior for signs of damage, rapid mapping of a small asteroid, or in-flight calibration of a communications beam pattern using deployable inspector spacecraft [25]. A proposed magnetospheric constellation mission that may reveal how the magnetotail behaves in response to solar wind variations, among other fundamental scientific data [26].

Remote sensing missions encompass a wide variety of specific missions operating over the full electromagnetic spectrum. Constellation design is similar to the communication mission options just discussed. Civil and military meteorological missions utilize satellites operating in LEO (polar or sun-synchronous) and GEO orbits to provide weather forecasters images and other data. They accomplish this mission by carrying visible, ultraviolet (UV), and/or infrared (IR) imagers. They usually are rather large satellites, but these capabilities have recently been demonstrated successfully with microsatellite-class systems performing a global disaster-monitoring mission, as the DMC programme [27].

Military and commercial imagery applications are also widespread where satellites take visible and IR images of specific regions of interest in the world. Commercial imagery is used for mapping requirements, agricultural data, disaster monitoring, and other generic requirements. Military systems are generally tasked to provide more detailed images or signals intelligence in regions of military conflict or strategic interest. There are also many proposed tertiary remote sensing missions, such as fire, earthquake, and volcano detection, radar, satellite inspection, and others too numerous to list.

Two student-built nanosatellite-class earth imaging missions have flown, one early in 2000 that proved some concepts [37] and another the same year that produced brilliant earth images and also performed a satellite inspection demonstration [38].

Can satellite-on-a-chip play a role here? Military signals intelligence and satellite inspection missions might be appropriate [28]. Distributed space-based radar missions have also been studied, but have reached no level of maturity [29]. This concept of using small satellites to perform larger missions is becoming quite popular, although the complications of formation flying [30][31][32][33] and intra-satellite communication [34][35][36] must be solved first.

## PAYLOAD DEFINITION AND SPACECRAFT CONFIGURATION

The Space Mission Analysis and Design (SMAD) process is used throughout for the first round of the satellite-on-a-chip design [13]. It is realized that some of these principles may not scale well for a satellite-on-a-chip. However, design guidelines for nanosatellite design now exist, some of which could be scaled to satellite-on-a-chip [39][40][41]. Unfortunately, the brevity of this paper does not allow us to highlight the equations used to achieve the results given.

The proposed orbit for this mission is sun-synchronous with a 686 km altitude and 98 degree inclination. That is the typical orbit configuration of remote sensing missions flown by the Surrey Space Centre. Ideally one of those missions could host a satellite-on-a-chip technology demonstration mission in the future.

Satellites are generally composed of a payload, which is designed to meet mission requirements within a given orbit. For the first satellite-on-a-chip mission, a simple Earth observation mission with minimal requirements is proposed, where a successful snapshot of the earth is taken within a day of deployment and sent to a ground station.

### Payload

Charge coupled devices (CCD) are typically used for imaging. However, they have some major disadvantages. They are built using non-mainstream semiconductor fabrication techniques, have a relatively high power requirement, and cannot be integrated with support circuitry monolithically with standard CMOS processes [42]. However, in the last decade, monolithic digital imagers built in CMOS have become a promising technology and may eventually replace CCD technology [43]. Not only is it convenient that we can build a CMOS imager right on the same wafer with the rest of the satellite, it is inherently low power and more sensitive, although the image quality is not quite as good. The chosen representative model is a recent work that only requires 80 mW per 13 K pixel image [44]. However, the selection of an imaging mission introduces the requirement of a lens system, perhaps an integrated microlens array [45].

### Spacecraft Configuration

With the payload defined, the most important thing to do first is to develop the spacecraft configuration. The “configuration” describes the physical relationship between the payload and subsystem components. Usually, the process starts with a simple sketch of the satellite, focused on the best location for the payload [46].

To make the idea more concrete, let us assume that a satellite-on-a-chip could be built on a modern semiconductor process available for prototype runs, such as the IBM 0.13  $\mu\text{m}$  mixed-mode process available through the MOSIS prototyping service [47]. The mass of a typical 200 mm (or 8 in.) diameter reference silicon wafer would have a mass of nearly 55 g, assuming a density of silicon of 2330  $\text{kg}/\text{m}^3$  and an average wafer thickness of 0.75 mm.

However, in the semiconductor manufacturing process, there is a limiting design factor called the reticle size. For this particular process, this means that the limit of a single design on the wafer cannot exceed 18 by 20 mm. The mass of a single 18 x 20 mm die would be less than 1 g, making it a “zeptosatellite,” which is impractical at this point due to tracking and communication issues discussed later in this paper. The application of wafer scale integration previously discussed allows use of an entire wafer for a single system. This idea is not new, however, as wafer scale integration has been widely explored in the 1990s [48]. By the end of the decade however, it was realized that wafer defects in manufacturing necessitate fault tolerance in wafer scale integration designs that has prevented wider adoption [49]. The limits of wafer scale integration will have to be better understood before proceeding.

Let us then confine the design of the satellite-on-a-chip to have a size no larger than a 200 mm diameter wafer. However, not all the area of the wafer can be used. Approximately sixty 18 x 20 mm die can be placed on the wafer. So instead of the full 314  $\text{cm}^2$ , only 216  $\text{cm}^2$  can be used on each side. The remaining area is lost to the edges of the wafer used for handling and the remaining space left over where a complete die cannot be placed along the circular edge.

## SATELLITE-ON-A-CHIP SUBSYSTEMS DESIGN

On average, the payload mass fraction is 26.7% of the spacecraft total mass. To support payload operation, there are various subsystems that must be in place. The spacecraft subsystems will make up the bulk of the mass (73.3% on average) and hence area of a satellite-on-a-chip, as in any satellite design. Spacecraft subsystems are responsible for pointing and navigation, data processing, generating and supplying power, and keeping all components within desired temperature ranges. In addition, the subsystems must hold the satellite together structurally, provide a way to receive commands and transmit data, and finally, meet requirements to maneuver in space with a propulsive device.

## Electrical Power Subsystem

The spacecraft Electrical Power Subsystem (EPS) typically provides four basic functions: power source, energy storage, power distribution, and power regulation and control [10]. We can confidently assume at this point that challenges in the power distribution, regulation, and control design can be met with basic wiring, switching, and regulation circuitry that can easily be placed on a wafer [50]. The challenge lies in implementing the power source and energy storage.

Integrating solar power with digital circuitry has not been of interest until recently, with efforts like “Smart Dust” [51] and other self-powered chip research [52][53]. Since solar cell fabrication on CMOS is fairly straightforward, we will assume an efficiency of at least 5% for this initial design based on results of other work. Drawing from results that will be presented in the communications section below, the total power needed for our design is approximately 16 mW on average. Using the SMAD rules of thumb with this result in our orbit, a solar array area of 7 cm<sup>2</sup> is found. A two-sided design has to be considered at this point, as there could be times in orbit when the inactive side is illuminated.

The solar cells will then provide power while the satellite is in the sun. But what about when it is eclipsed by the Earth? It is reasonable to assume that we will want some minimal system functionality, even if it is simply to keep the volatile memory intact. The only reasonable way to store energy in CMOS is with an integrated capacitor [54]. However, basic capacitance equations reveal that an on-chip capacitor would not have anywhere near the required capacity.

We could get around this issue by expanding the design space to allow a commercially available thin-film rechargeable battery to be placed between the wafers [55]. Ultra capacitor and nuclear batteries are other options but are out of the scope of the design. Most likely, confining operations to sunlit passes over the ground station will be the best option.

## Data Handling Subsystem

The data handling subsystem is basically the on-board computer for the satellite, responsible for several jobs. It receives, validates, decodes, and distributes commands from the ground, payload, or a subsystem to other spacecraft subsystems. It also gathers, processes, and formats spacecraft housekeeping and mission data for downlink or use on board. This subsystem is usually the most difficult to define early in the design due to the vague hardware and software requirements from the payload and subsystems.

In academia, some introductory thought has been given to miniaturizing flight computer components to a single chip [56]. More recent work has shown that image processing capabilities and a communications interface should be added as well [57]. There is also some complementary industry interest in the topic [58].

One major issue that plagues data handling systems operating in space is the natural radiation environment. The radiation environment is composed of ionizing radiation that causes gradual system degradation and high-energy particles, such as electrons, protons, and heavy ions, causing single event effects. For this short mission in LEO, we will only be concerned with the single event effects. Fortunately, the process of mitigating these effects is well understood [59] and has proven effective in previous CMOS designs [60].

## Communications Subsystem

An obvious challenge for a satellite-on-a-chip is the communications link between the ground and the satellite. It is not unreasonable to assume that the uplink will not be too difficult to implement, as transmit power from the ground can be increased to cover any shortfalls in the satellite limited only by governing regulations. However, the exact satellite position must be known to avoid pointing losses with the high gain antennas that must be used. This issue will be addressed in the next section. The receiver on the satellite would be implemented similar to previous work on integrated on chip transceiver and antenna designs [61].

Likewise, an integrated transmitter and antenna design would be used on the satellite, communicating with the ground station that would have a large gain antenna. The biggest issue in the communications link design would then be the RF transmit power of the satellite and the corresponding electrical power to drive it.

Using the appropriate worst-case parameters for a notional downlink frequency of 2.2 GHz, data rate of 300 bps, 3.7 m receiver dish, 3.4 cm on-chip transmit antenna ( $\lambda/4$ ), and binary phase-shift keying modulation (BPSK) with turbo decoding [62], we get a required output power of 1 mW, with a reasonable 5 dB margin. At this frequency, 1% efficiency is assumed, giving a 100 mW electrical input.

## **Attitude and Orbit Determination and Control Subsystem**

The Attitude and Orbit Determination and Control Subsystem (AOCS) is usually further thought of and divided into the attitude (ADCS) and orbit control (OCS) segments, with the former discussed first. To keep the spacecraft pointed in a desired direction to meet mission requirements, the current attitude must be determined with certain accuracy over a given range. Once the current attitude is known, it must be controlled to a specified accuracy, while meeting range, jitter, drift, and settling time requirements. In general, the payload, EPS, and/or the communications subsystem will drive the ADCS requirements. In our application, the imaging payload is the ADCS driver.

In general, satellite designers can meet pointing requirements by using active and/or passive means. Active techniques could be employed, thanks to advances based on MEMS gyroscope technology [63]. More stringent missions would use a combination of star sensors, differential GPS, or solid-state gyroscopes to determine attitude then control it with biased or unbiased reaction wheels, control moment gyros, or thrusters. However, for this size of mission with fairly relaxed requirements, a combination of passive magnetorquers and an aerodynamic shape can be used [64][65][66][67].

The OCS is a problem of navigation, guidance, and control (NGC). Ideally, once a satellite is placed in the desired mission orbit by the launch vehicle, it will stay there forever. However, there are many external forces that cause the simplified earth-satellite two-body system to behave in a non-idealistic fashion. The first contributing factor is the oblateness (i.e. it is not a perfect sphere) of the earth that affects all orbits. The second factor is the drag environment that is significant in orbits less than 1000 km in altitude. To maintain orbit, knowledge of where the spacecraft is at all times must be known. Virtually all space missions on Earth rely on orbit tracking data made public by the US Space Surveillance Network [68].

The size of our satellite-on-a-chip will be difficult for their sensor network to detect, especially on-edge. An initial set of Keplerian elements (a description of satellite position and velocity) can be obtained upon separation from the host spacecraft and/or launch vehicle, so we will have an initial idea where to look. Over time, we will slowly lose track of where it is if it cannot be detected. On-board GPS is promising [69][70], however, simple low-power applications like this one may use more simple methods, such as Doppler tracking to determine the satellite position [71][72]. Another possibility is to etch in corner cube structures onto the wafer to increase the radar signature.

## **Propulsion Subsystem**

Ideally, once a satellite is in a desired orbit, it will stay there forever. As mentioned previously, other non-ideal forces make this not so. A propulsion system of some sort is needed to maintain orbit. Surprisingly, much work has been focused on micro-propulsion. Solar radiation pressure has been looked at as a non-propulsive source of station keeping [73]. Exotic solar-thermal propulsion systems have been examined for satellites above 20 kg and above in the microsatellite class [74][75]. More traditional approaches have investigated simply miniaturizing current propulsion components using MEMS [76][77][78]. Another realistic concept is to use a solid-state laser to ablate fuel [79][80].

The most promising technology that is applicable to satellite-on-a-chip is the digital micro-propulsion effort [81]. This technology embeds discreet amounts of propellant in an array of sealed capsules on a silicon substrate. When the appropriate control lines are activated, then the propellant is heated and released. However, at present, this technology is not readily integrated on a CMOS wafer and can only deliver sub-millimeter station keeping for a 1 kg spacecraft orbiting above 100 km, which is somewhat less than what is needed.

## **Thermal Control Subsystem**

Thermal control is an important issue, even for something as small as a satellite-on-a-chip. This first order design simply looks at the steady-state maximum and minimum temperatures that the spacecraft would encounter. These two points will simply serve as bounds to the problem, knowing that dynamic sunlight-eclipse cycles will not allow time for either extreme to be met. Simple temperature data collection will be the heart of the subsystem itself.

The solar absorptivity constant ( $\alpha_{\text{solar}}$ ) for a silicon wafer is 0.48 and the infrared emissivity ( $\epsilon_{\text{IR}}$ ) is 0.46 [82]. This gives a steady-state maximum temperature of 96°C and a minimum temperature of -74°C. These extremes are concerning, as the temperatures are out of the range of most battery technologies (0 to +25) and electronics (-10 to +50). However, they do not accurately represent the true range due to the frequent eclipse cycles and thermal inertia of the satellite. These results would have to be verified in the laboratory and any problems would be solved using a passive thermal management substrate that the wafers would be adhered to in order to narrow the temperature range.

## CONCLUSIONS

The purposes of this paper were to survey the literature and to propose a realistic satellite-on-a-chip design. Overall, it seems that the technology has existed for some time to build a satellite-on-a-chip, however no one has attempted to build one yet. Instead, various research groups have chosen to develop in great detail individual subsystems that could be used in the future. If one were to implement a proof-of-concept satellite-on-a-chip, there are several challenges that must be addressed during the process, as follows:

- The first mission must be simplistic, with minimum requirements and lifetime.
- The configuration itself needs further research. The wafer scale integration (WSI) approach may introduce problems, either by wafer yield or the designer's access to an entire wafer.
- An imaging payload would require an optical structure to be added over the sensor circuit.
- Power storage is an issue to be resolved. Sunlit passes is the simplest approach, followed by adding a battery.
- The communication downlink needs to be designed with a large margin.
- Passive attitude control and tracking techniques needs further definition.
- The thermal environment needs to be more accurately modeled.

This paper has outlined a possible first order design of a satellite-on-a-chip. Along the way, our definition has evolved to "the smallest possible satellite built of two monolithic integrated circuits and a minimum of external components and assembly that can be launched into space to perform a mission while communicating with a ground station." A successful demonstration of this technology will open the door for distributed mission concepts.

The envisioned configuration of a "satellite-on-a-chip" would have the following properties: 200 mm maximum diameter (216 cm<sup>2</sup> total design space), less than 5mm thick, less than 100 g mass, and 100 mW peak power. The demonstration mission would be a simple earth-imaging mission where a snapshot of the earth would be taken and downloaded to a ground station using an imaging device with less than 20,000 pixels and an integrated or external lens structure. The satellite would be self-powered with integrated solar cells requiring a minimum area of 43 cm<sup>2</sup>. At the heart of the satellite would be a simple data handling subsystem hardened against single event effects, coordinating all the subsystems with a direct-connect star network configuration. The communication link uses a low data rate to achieve a 5 dB margin. Passive attitude control is used to stabilize the spacecraft. A two-sided design must be considered with an integrated passive thermal control and host spacecraft interface.

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