# SOI-CMOS TECHNOLOGY FOR THIN FILM SENSORS ON MEMBRANES

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## ABSTRACT

Silicon-on-Insulator (SOI) technology is emerging as a major contender for heterogeneous microsystems applications. In this work, we focus on the its advantages for realizing thin film sensors on membranes (gas-composition, gas-flow and pressure sensors). We demonstrate its simplicity by actual validated co-integrated realizations in CMOS-SOI technology.

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## INTRODUCTION

SOI (Silicon-on-Insulator) technology has now been widely demonstrated and recognized to be a mature and viable alternative to mainstream bulk silicon (Si) for the realization of high-speed, low-power digital [1] and analog/RF [2] CMOS circuits, as well as niche applications under extreme high temperature [3] or radiation operating conditions [4].

In this work, based on an extensive review of research results on the material, process and component properties, we aim at demonstrating that and how SOI processes can advantageously be used to directly co-integrate sensors on membranes with CMOS circuits on the same silicon die, targeting the development of single-chip harsh environment microsystems (Fig. 1). Such dielectric membranes are required as starting material to achieve a great thermal insulation of microheater based gas-flow sensors. It was demonstrated that thin dielectric membranes, only 1 μm thick, constitute the best option to consume very low heating power in order to be integrated in low-power smart gas sensors [5].

## SOI TECHNOLOGY

Silicon-on-Insulator (SOI) substrate is likely the best way to overcome the limitations of bulk technology. The insulating layer blocks charges transport between the active layer and the substrate, featuring this technology as the best one for radiation and high temperature environments, like outer space, military or industrial and automotive sectors. In addition, the reduction of parasitic capacitances and leakage currents allow better high-frequency performances and lower power consumption when compared to silicon bulk process.

Recently, SOI technology has also been applied to Micro-Electro-Mechanical Sensors (MEMS) [6, 7]. The buried oxide present in the SOI material can be very successfully used as an etch-stop layer for both the wet and dry bulk micromachining, either from the back or from the front side of the wafer. When releasing the silicon substrate from the backside of the wafer for instance, a stacked buried-oxide/silicon membrane can be obtained. The high quality of the top crystalline silicon film enables semiconductor devices such as temperature sensors, microheaters, MOSFETs, microwave circuits to be built within the membrane in order to get a better thermal or electrical insulation. This membrane can also play the role of support for mechanical sensors to sense pressure for instance.

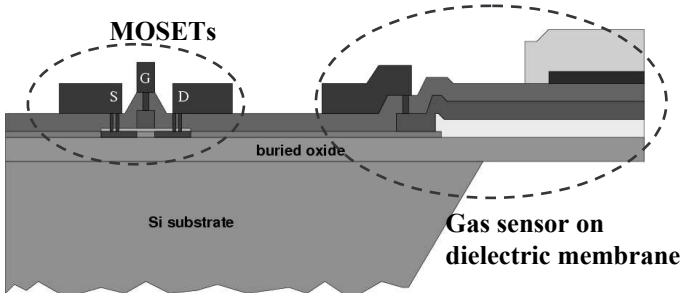


Fig. 1. Cross-section of the co-integration of MOS devices and gas sensor on dielectric membrane in SOI CMOS technology.

The use of SOI thereby appears as the best approach in processing of either circuits or sensors. In addition, it offers the unique advantage to save a great deal of design time and efforts in fabrication of microsystems, combining the electronics and the sensors on the same chip.

## MEMBRANE MICROMACHINING

The materials chosen for the membrane of the microhotplate have to combine low thermal conductivity (i.e. small thickness) with high mechanical strength (i.e. large thickness) [8]. While insuring compatibility with a micronic fully depleted (FD) SOI-CMOS process of interest for micropower or high-temperature applications [9], the 400-nm-thick buried thermal oxide of the SOI substrate can advantageously constitute the first part of the membrane. A second part of the membrane stack is composed of the densified PECVD oxide layer related to the interconnect dielectric between the polysilicon and aluminium layers of the CMOS process. For mechanical robustness, a nitride layer must be added and the thickness must be chosen to carefully compensate the high residual stresses of the deposited films. The thermal oxide usually shows a compressive residual stress of about 250 MPa and nitride a tensile residual stress of about 1.2 GPa. The total stress of the sandwich layer is calculated by (1) where $t_{ox}$ and $t_{nit}$ are the thicknesses of oxide and nitride, respectively.

$$\sigma_{tot} = \frac{t_{ox}\sigma_{ox} + t_{nit}\sigma_{nit}}{\sigma_{ox} + \sigma_{nit}} \quad (1)$$

The equation shows that the ratio between the two thicknesses would be 4 to have a strain-free membrane. But, in practice, the best choice is to take a ratio of about 2 to have a slightly tensile membrane and to take into account its high critical lengthening ($7.8 \times 10^{-3}$) [10]. In practice, based on stress measurements (Tab. 1), we selected thicknesses of 300 nm for the LPCVD nitride layer and 290 nm for the PECVD oxide layer for a total thickness of around 1 µm with low residual stress (80 MPa) and low stress gradient (0.78 %). Fig. 2 shows that with these parameters, we obtained an almost strain-free membrane (i.e., with no visible ripples).

Membranes were released at the end of the SOI CMOS process by etching silicon using a Tetramethylammonium Hydroxide (TMAH) based solution. In comparison with EDP and KOH alternatives, TMAH achieves CMOS compatibility and is easy to handle due to its low toxicity. Moreover, high selectivity is achievable versus all dielectrics

| **Layer** | **Average stress** [MPa] | **Strain gradient** [%/µm] | **Stress gradient** [MPa/µm] | **curvature** |
|---|---|---|---|---|
| **Thermal oxide** | -331 | 0.24 | 170 | + |
| **LPCVD nitride** | 860 | negligible | negligible | / |
| **PECVD oxide** | -172 | negligible | negligible | / |
| **Sandwich O-N** | 174 | 1.01 | / | + |
| **Sandwich O-N-O** | 80 | 0.78 | / | + |

Tab. 1. Summary of our stress measurements in mono and multi-layers.

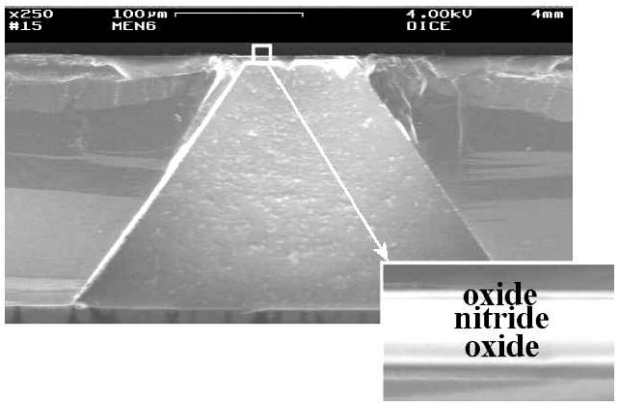


Fig. 2. Cavity profile under the membrane and detail of the three-stacked dielectric layers of the membrane.

(and aluminum after optimization). All these characteristics make this etchant very attractive to perform the final backside micromachining without special care to the integrated circuits on front side. In particular, selectivity versus aluminum is achieved when an appropriate amount of silicon powder (to decrease the pH of the solution) and diammonium peroxydisulfate (or APS, as oxidizer to improve the surface quality) are added into the solution. By this way, only 3 hours were needed to release clean membrane from 200 µm thick silicon wafers using a TMAH 10% solution heated at 90°C and doped with 35 g/l of silicon powder and 15 g/l of APS.

## MICROHOTPLATE DESIGN

The design chosen for the heater is a loop-shaped phosphorous doped polysilicon resistor (Fig. 1) optimized by finite element method (ANSYS software) to achieve low power consumption and high thermal uniformity. A 340-nm thick phosphorous doped polysilicon is used for the heater because it is the common material and thickness for the gate in CMOS and SOI-CMOS fabrication. The doping level is imposed by the IC process to have a resistivity of around 25Ω/square (the material resistivity expressed in /square is obtained by dividing the material resistivity in Ω.m divided by its thickness). Nevertheless, this value is a good trade-off between thermal uniformity and low-power consumption. In this case, the temperature coefficient of resistance (TCR) is positive and unfortunately leads to hot spots formation. At the opposite, a lower doping level would involve a more uniform temperature distribution but, due to the higher resistivity, the power consumption would increase.

Besides, the membrane dimensions have also a strong influence on the microheater performances. Increasing its thickness by a factor 2 will increase the power consumption by 30% at 400°C (Fig. 3), while using a membrane thinner than 1 µm leads to decrease in power, thermal uniformity and also in membrane robustness. On the other hand, large surface membranes allow a high thermal insulation (Fig. 4) but are also detrimental to their robustness. The active area of our membranes can be heated to working temperatures of 400°C with 25 mW, which is a competitive result in comparison with other recently published microheaters [5]. Thermal uniformity was confirmed by thermo-reflectometry measurements. Thermal ageing and reliability tests (deformation, high frequency switching and high temperature) were performed to validate the great robustness of the membrane.

## GAS-FLOW SENSORS

### Microheater Based Gas-Flow Sensors Design and Fabrication

This novel loop-shape polysilicon microheater was integrated on top of our optimized membrane in order to implement the basic heating cell of new simple SOI CMOS compatible gas-flow sensors. For gas-composition measurements, a gas sensitive layer (typically a metal oxide) as well as interdigitated electrodes need to be deposited on top of the microheater to sense the concentration of ambient gases, through the variation of the sensing layer conductivity (Fig. 5). For this purpose, the microheater needs to feature high thermal uniformity, high thermal insulation and maximum working temperatures. After packaging, an on-chip annealing is performed at 700°C for gas sensing film activation without damaging the associated electronic components.

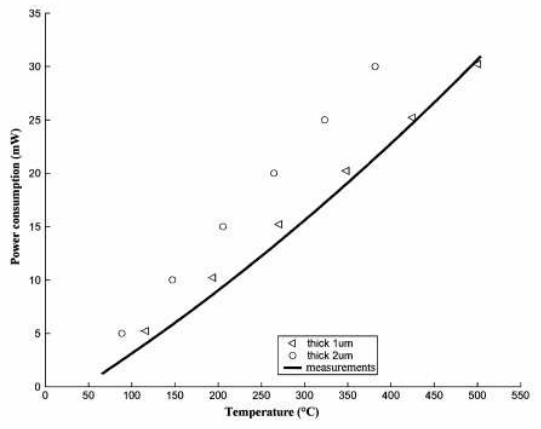


Fig. 3. Influence of the membrane thickness on the microheater power consumption versus membrane temperature (Δ and o are simulations results).

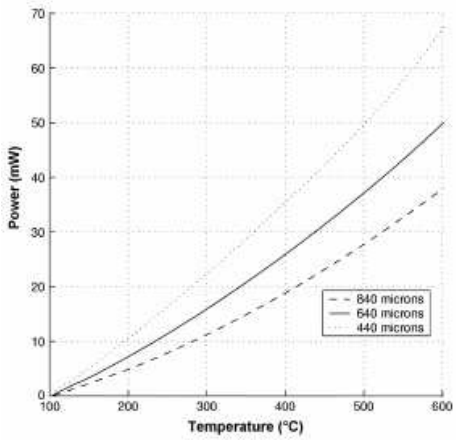


Fig. 4. DC Power consumption versus temperature elevation measurements for three different sizes of square membranes (840 µm, 640 µm and 440 µm on one side).

To achieve flow velocity measurements, the microheater needs to be integrated between thermopiles (such as Al/PolySi) to build a calorimetric flow sensor (Fig. 7). Many gas-flow sensors reported in literature were said "CMOS compatible" [11] but most of them used layers or processing steps which are not inherent in standard IC fabrication. Furthermore, only a few have been actually produced in standard CMOS processes. The originality of our design is that it is actually compatible with a standard SOI CMOS process, on the same wafer than integrated circuits. On the other hand, many different flow sensing principles can be found in literature and impose a difficult choice between low power consumption, high airflow rate range, sufficient flow rate sensitivity and compatibility with IC processes. Our sensor challenges most recent realizations by providing attractive trade-offs between these parameters for a large range of applications.
The sensor fabrication process was optimized in order to be integrated in intermediate- and postprocessing of a standard IC SOI CMOS fabrication. In comparison with the standard SOI-CMOS process, only 2 more masks are necessary for the intermediate processing: the first one to pattern silicon on the membrane location and the second one to etch the nitride layer (Fig. 1). This process therefore also requires 2 more photolithographies, 1 more deposition (LPCVD nitride layer) and 2 more etching (silicon film and nitride layer).

The standard and intermediate process steps are followed by the postprocessing steps. Pt/Ti interdigitated electrodes (200 nm thick) are first deposited by evaporation on the PECVD oxide layer on top of the microhotplate and patterned by lift-off (Fig. 5). It is well known that e-beam evaporation induces X-rays which introduce positive charges in the gate oxide and damage the electrical properties of integrated electronics. Forming gas annealing at 432°C during 30 minutes is therefore performed in order to remove the trapped charges and return electrical characteristics to normal.

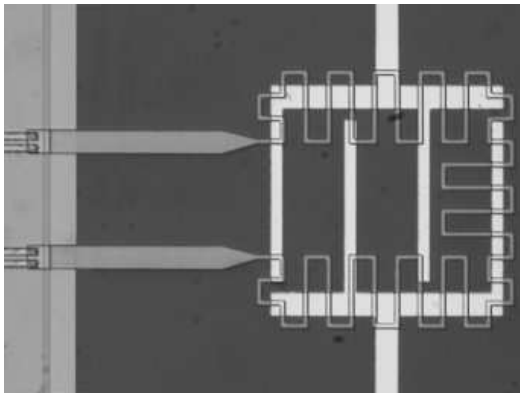

Fig. 5. Zoom on the gas sensor active zone before the gas sensitive layer deposition. Interdigitated electrodes can be seen on top of the microhotplate.

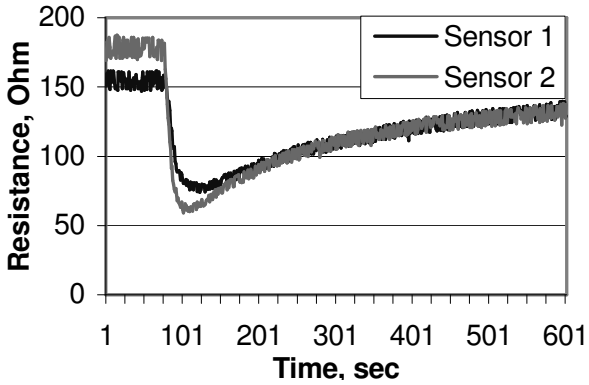


Fig. 6. Time response to ethanol of SnO2 drop-coated sensors.

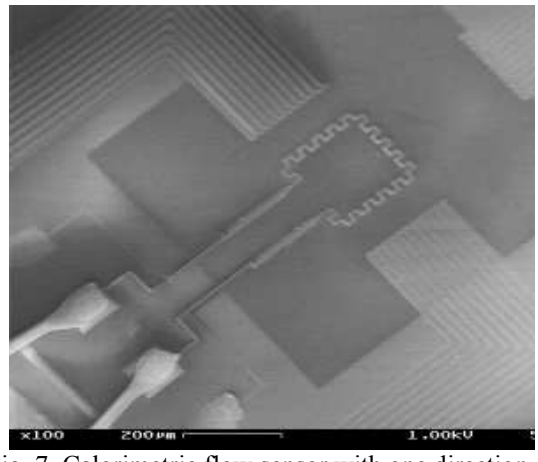


Fig. 7. Calorimetric flow sensor with one direction of detection.

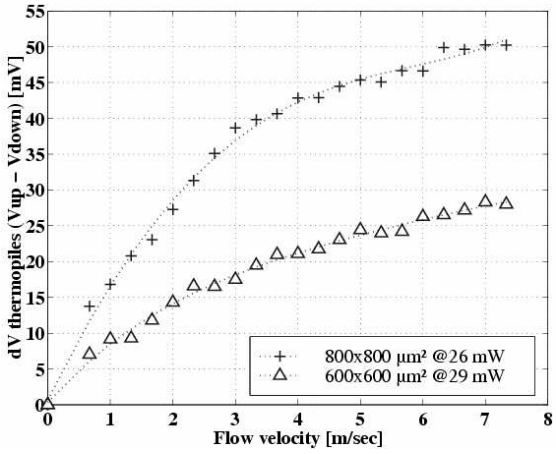


Fig. 8. Measured differential voltage across the thermopiles vs. the applied flow velocity for 2 membrane sizes.

The backside wafer is then thinned and mechanically polished to reach a thickness of 200 µm, more appropriate to a silicon wet etching. A 500 nm aluminum layer is evaporated on backside before its patterning using double side alignment. This layer advantageously plays the role of back gate contact for the integrated circuits and of mask to protect silicon during TMAH etching. This step is followed by the full immersion of the processed wafers into the doped TMAH solution during 3 hours. Finally, 600 nm thick sputtered gas sensing films (such as SnO2 and WO3) are deposited before the dicing and packaging while drop coated films (around 10 µm thick) are deposited on packaged sensors. Thanks to the great robustness of our membranes, dies with membranes as large as 800x800 $\mu m^2$ were packaged with a very good yield (around 97 %).

**Measurement results**

Measurements in presence of nitrogen flow revealed a good sensitivity on a large airflow rate range (0 to 8 m/s) for the flow transducer (Fig. 8). In comparison with recent published results, our design firstly offers the advantage to reach high temperature at very low power consumption, as well as a good response time (25 ms), which contributes to provide a great sensitivity to flows [12]. Unfortunately, our p++-PolySi/Al thermopiles do not feature sufficient sensitivity, but have the advantage to make our design simple and easy to integrate in a standard SOI CMOS process. A better sensitivity could be provided by doping the thermopiles and the microheater differently, using a second implantation mask. In comparison with the CMOS compatible sensors we can find in literature, our devices offer good results for a very simple design thanks to the great performances of our 1 µm thin dielectric membrane. Therefore, our flow sensor seems to present attractive trade-offs between the above-mentioned parameters for a large range of applications.

Finally, measurements in presence of gas revealed a good sensitivity to gases such as ethanol (Fig. 6), ammonia and nitrogen dioxide for the gas transducer [13].

**CO-INTEGRATION VALIDATION**

Various transistors (in size, type and doping levels), MOS capacitors and gated diodes were integrated on the same chip as the sensors and therefore processed in same time (Fig. 9). Measurements of these circuits after each post-processing steps allowed for validating the whole CMOS compatibility of our optimized SOI CMOS process as can be verified in Fig. 10.

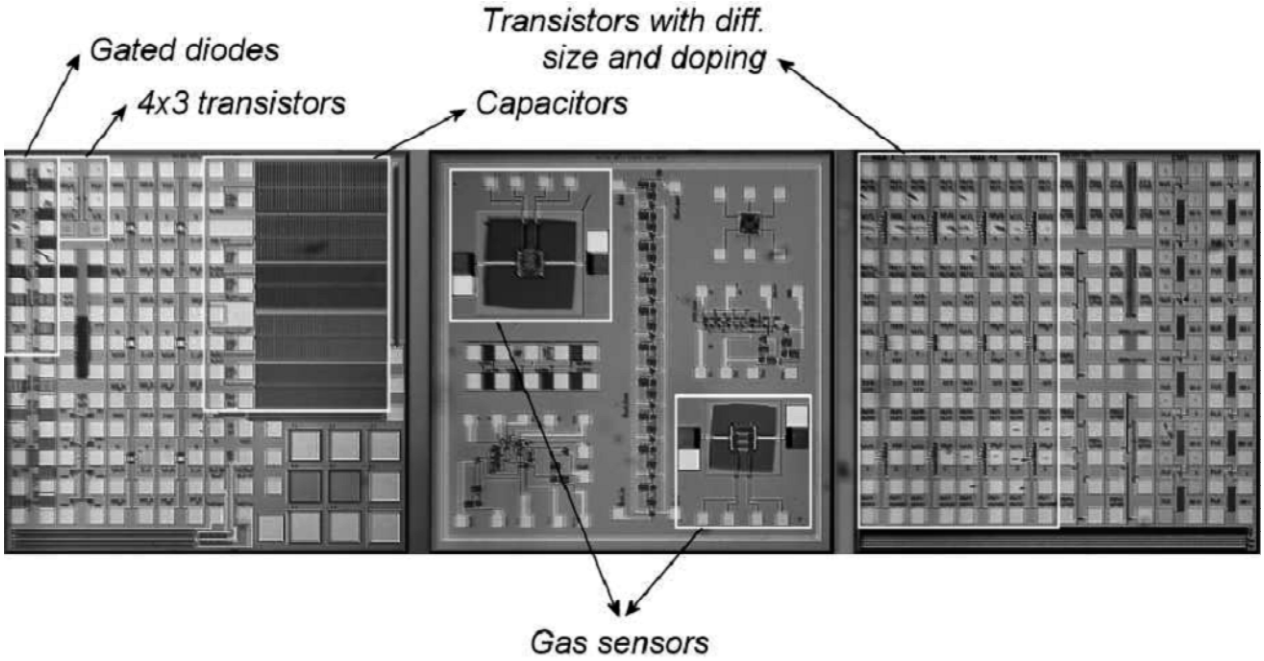


Fig. 9. Co-integration of integrated circuits and gas sensors in SOI CMOS technology.

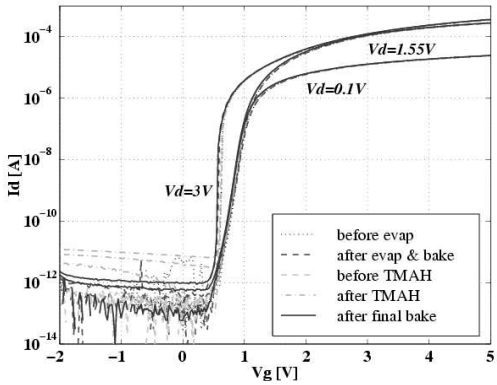


Fig. 10. Measured Id/Vg characteristic during the post-processing steps for 4x3 µm$^2$ n-transistors (back gate at 0V).

Finally, transistors integrated in small silicon islands located in the middle of our dielectric membranes were successfully fabricated as a concluding demonstrator of the co-integration in SOI technology. Such devices open the door to many new applications (such as gas FET and transistor-based pressure sensors) where integrated circuits and sensors are merged for higher performance in harsh environments.

**PRESSURE SENSORS**

We have recently demonstrated the great possibility to build transistors on released membranes starting from a SOI wafers and using a classical SOI MOS process. This new approach is now used to build pressure sensors: disposing transistors directly on membranes and using them as sensitive elements. Indeed, under mechanical constraints the membrane underlying the devices deflects and affects the mobility of electrons and holes in the SOI thin film. Replacing standard polysilicon piezoresistors by active devices will probably bring an easier signal processing and increase the sensor sensitivity.

As a first study we applied a vertical nitrogen flow just above devices placed at the centre of membranes. The strain induced by the dynamic pressure involves a deflection of the membrane resulting in an increase of the saturation current as well for n-type transistors as for p-type devices (Fig. 11 and 12).

Due to the centred position of the measured transistors, they where submitted to bi-axial constraints. According to Tab. 2, n-MOS transistor piezoresistive coefficients along both directions have the same negative sign. Therefore, they both have a positive influence on electron mobility in Si lattice. On the other hand, the centroid-shaped p-MOS transistor is also placed at the centre of the membrane. Hence, the strain applied on its channel has a central symmetry. The high increase of the saturated current let us think that this strain is mainly perpendicular to the current direction.

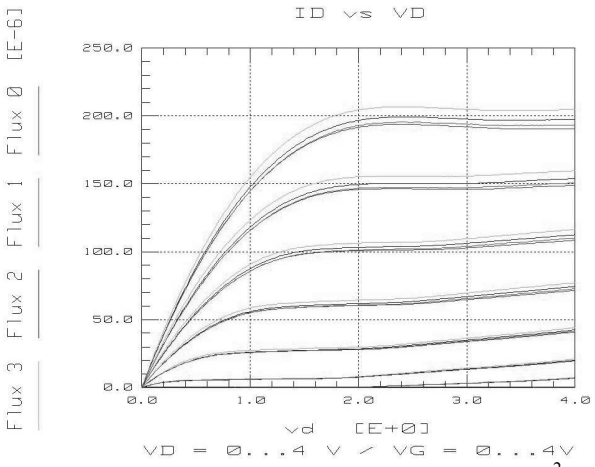


Fig. 11. Measured Id/Vg characteristic for 4x3 µm$^2$ n-transistor under nitrogen flows (0, 1, 2 and 3 l/min).

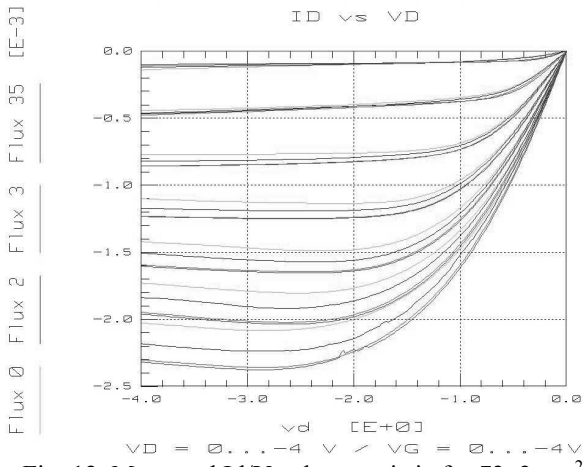


Fig. 12. Measured Id/Vg characteristic for 72x2 µm$^2$ centroid p-transistor under nitrogen flows (0, 1, 2, 3 and 3.5 l/min).

| n-MOS transistor | | p-MOS transistor | |
|---|---|---|---|
| $R_{//}$ (%/kBar) | $R_{\perp}$ (%/kBar) | $R_{//}$ (%/kBar) | $R_{\perp}$ (%/kBar) |
| -3.35 | -1.9 | +6 | -5 |

Tab. 2. Typical values of piezoresistive coefficients in MOSFET transistors <110> directions, (100) plane.

## CONCLUSIONS

It has been presented that and how the thin film SOI CMOS specificities can be interestingly combined to address the realization of intelligent SOI CMOS integrated sensors for special environments in a wide range of applications such as automotive, aerospace, gas detection, biomedical, quality control.

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