3D interconnect technology for space applications

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ABSTRACT

High-density integration of different technologies such as microprocessors, memory, imagers, sensors, RF circuits, ... is a challenge. Current integration based on wire bonding, results in limited interconnect density and often affects performance. Integration on a single substrate (System on a Chip) is technologically complex -if feasible at all- and often compromises system performance. A possible solution to both the hybrid integration limitations and the interconnect bottleneck is three-dimensional stacking of dies: "3D integration". The main advantages of such technology are: 1) size/volume reduction, and 2) a higher density of interconnects with lower capacitive and inductive parasitics. Moreover, it allows "seamless" mixing of different microelectronic technologies at the wafer level.

The range of possible space applications of 3D stacking is very broad. Particular examples of applications of 3D integration for space are (i) Advanced imagers using through-wafer interconnects and/or wafer thinning, for infrared, visible and X-ray detection, (ii) 3D RF modules, including RF passives and RF-MEMS components, and (iii) Highly miniaturized intelligent sensor nodes, incorporating sensors, read-out electronics, wireless communication and power scavenging.

There are generally speaking 3 possible approaches of 3D stacking: (i) 3D-"System-in-a-Package" (3D-SIP): This technique covers the stacking of multiple dies in a single SIP-package and/or the stacking of multiple SIP-packages. The technology is based on flip-chip using solder balls and therefore provides a low interconnect density (10 interconnects/mm2). (ii) 3D-"Wafer level packaging" (3D-WLP): A wafer level packaging technology that includes vertical electrical feedthroughs (vias) going through the (thinned) wafer and as such allows direct stacking of wafers or dies. The 3D interconnects are processed post chip passivation and allow low to medium interconnect density (10-100 int/mm2). (iii) 3D-"Stacked IC" (3D-SIC): The interconnects are processed post Front End and prior to Back End in a modified CMOS process. Using wafer bonding technology, a very high interconnect density (1000 or more int/mm2) is obtained.

This paper will present these approaches and their underlying technologies in detail. The relevance of these technologies for space (sensor) systems will also be discussed.

1 INTRODUCTION: 2D VS 3D

Heterogenous integration is very complex. Today's most widespread approach involves multiple-chips mounted side-by-side on a passive substrate (interposer or PCB). Interconnections between dies are made through wire bonding via the interposer board. Each die in itself is build up according to a 2D architecture with peripheral interconnections. Traditional assembly technology therefore has fundamental limitations in terms of area and performance since it suffers from large interconnection lengths as well as an interconnect bandwidth bottleneck.

Alternatively one can consider fully 2D monolithic integration in which different technologies are combined on the same die (vertically or adjacent). Following this route is not always possible due to the inherent incompatibility of some technologies (e.g. using different substrate types). In general, processing complexity will increase and trade-offs in performance have to be made. In any case, the interconnect hierarchy is not optimal since placing modules besides one another in 2D will increase the interconnect length. Moreover due to the increased design complexity and the increased number of process steps, the production cost of such a chip increases significantly while yield decreases.

A suitable 3D integration scheme addresses most of the above problems.

3D integration inherently carries the potential to combine different individually optimized technologies since tiles are made on separate dies, which are stacked on top of each other with a potentially very large interconnection density.

The main R&D driver of these new technologies is the ever-increasing performance demands placed on future mainstream chip technology. Today's technology advances are essentially achieved by scaling the devices. However, a large part of the performance benefit of scaling is lost in the interconnections between the devices. Due to their capacitance, inductance and resistance interconnections become limiting for the speed of the circuits. In addition, a lot of power is wasted in the interconnections, power which does not directly contribute to calculations. Last but not least, the thermal management issue is aggravated since part of this power generates heat in the resistance of the interconnections.

A typical example where 3D stacking can be useful is in stacking memory on top of logic circuits in a microprocessor (Fig. 1.). Memory is generally different in terms of technology than logic despite the fact that they use the same substrate type, so preferably you'd like to process them separately on individual chips, yet the interconnectivity between dies in a 2D scheme is low, causing a throughput bottleneck.

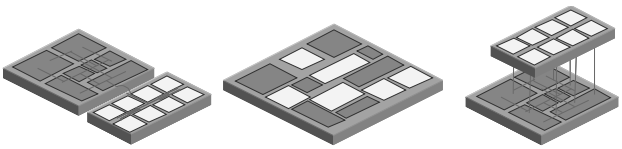


Figure 1: Different approaches for combining logic and memory circuits. Left: 2D interconnect between logic and memory die; Center: (2D-SOC) combined logic and memory device; Right: "heterogeneous 3D-SOC" stacking of a memory and logic device with 3D interconnects between individual logic tiles and memory banks.

Despite the significant advantages of a 3D approach, today's IC technology is still mainly a 2D world. This indicates the difficulty in conquering the challenges in implementing such a scheme. More in particular:

1. new technology needs to be developed and mastered in order to make chip stacking possible.
2. A large unknown exists in yield and reliability of a chip stack.
3. Furthermore, since the design constraints change, the entire design methodology needs to be reviewed, which is likely to give rise to completely different chip architectures specially adapted to fully exploit the potential of the 3D design environment.

A major roadblock, in the form of thermal management of the chip, still persists however, and is likely to become (or rather remain) the biggest design constraint (for high end chip technology).

2 3D STACKING APPROACHES

In literature one can find a very large number of different approaches to 3D stacking of die[3,4,5,6,7,8]. Generally these solutions address a specific problem in a specific technology. In order to promote a more generic 3D platform, the following division is made in 3D stacking approaches, based on the level of integration [3]:

- 3D-"System-in-a-Package" (3D-SIP): Integration on the package level.
- 3D-"Wafer level packaging" (3D-WLP): Integration on wafer level.
- 3D-"Stacked IC" (3D-SIC): Integration on IC foundry level.

2.1 3D-SiP

This relatively mature technology is the easiest to implement compared to 3D-WLP and 3D-SIC. In 3D-SIP multiple dies are integrated in the same package. The resultant packages are afterwards stacked on top of each other using flip chip technology. Interconnections between packages run via the PCB and are thus made by means of relatively large (300 µm diameter) solder balls. For vertical miniaturization the chip thicknesses are limited, however it is not necessary to go below 50 µm final thickness. The fairly large solder balls also imply a limited interconnection density of 2-3 per mm along the periphery or 5-10 per mm^2 area.

Fig. 2. shows a practical example of a 3D-SIP package from concept to realization [10,11]. What it represents is one single node, measuring no more than 1 cm^3, of a sensor network for medical EEG/ECG measurements. In this network, each node consists of a sensor with a wireless interface to a remote receiver. One of the benefits of this system is that it does not limit the mobility of the patient.

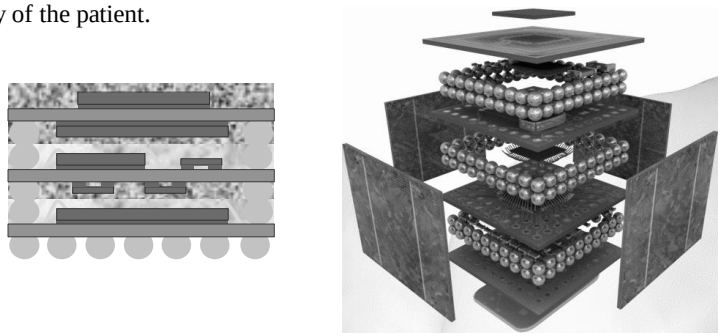


Fig. 2. Intelligent Wireless 3D Stack from concept to realization [11]

2.2 3D-WLP

In 3D-WLP, fully processed dies are stacked on top of each other at wafer level. Interconnections between the different chips are made either by thin film processing in which the chips are embedded in a large-scale back-end (Fig. 3.) [9] or by through wafer vias with a relatively large diameter of e.g. 150 µm (Fig. 4.). Both concepts use post IC processing techniques. 3D-WLP offers a medium interconnect density of 10-25 peripheral interconnections per mm or equivalently 10-100 interconnections per mm^2.

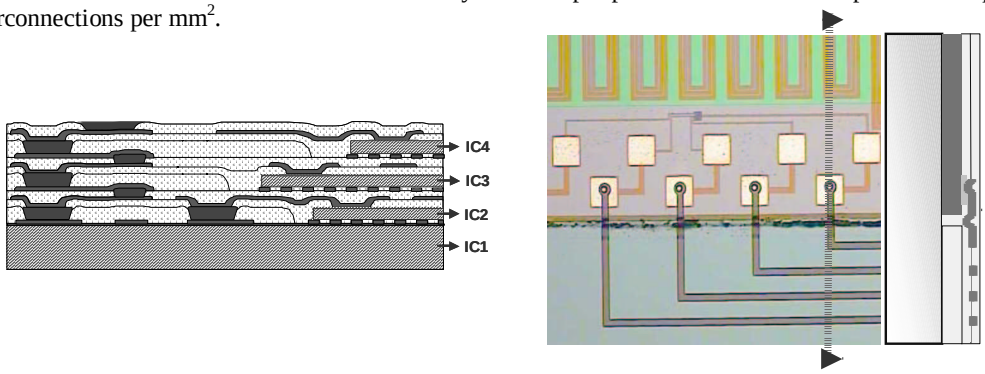


Fig. 3. Electrically connected 15 µm thin embedded die in post-IC large scale back-end: concept and realization.

Making through wafer interconnections requires multiple process steps. A typical process flow is as follows:

- Dry etching of the vias/holes using (D)RIE ((Deep) Reactive Ion Etching)
- Deposition of a dielectric isolation layer e.g. an oxide or nitride passivation.
- Metallisation of Si-holes by realizing a solid metal via-"plug". Typically bottom-up Cu electroplating is used for the via filling, followed by a CMP polishing step to remove the excess Cu plated on the wafer.
- Wafer thinning of the wafer down to 10-100 μm, exposing the Cu plug.

Depending on the application, wafer thinning can also be the first step while the vias can be processed from the back.

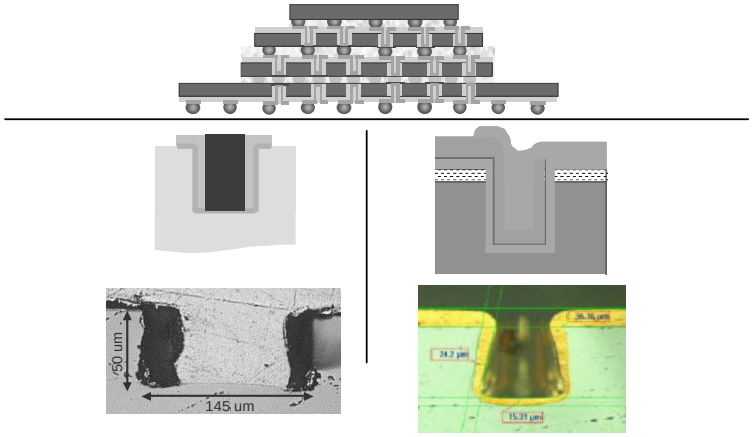


Fig. 4. Microbump hybridization using large through wafer interconnections filled using Cu electroplating. Top: concept of through wafer interconnections. Left: bottom-up Cu fill. Right: partial Cu fill + polymer core.

Very stringent requirements can be placed on micro bump interconnects. The main challenges here lie on plan-parallelism and maintaining alignment accuracy during flip chip bonding to achieve high yield and reliability especially for the smallest bumps with a pitch of 10 μm (Fig. 5.).

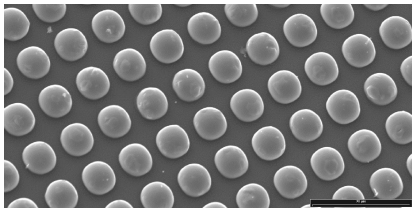


Fig. 5. Micro bumps with a pitch of 10 μm

2.3 3D-SiC

3D-SiC utilizes through wafer interconnections / vias, which are processed post Front End and prior to Back End in a modified CMOS process. In fact, processing of these vias is very similar to regular damascene processing and thus can be considered the first step of the Back-End. In this way, there is no reduction in the back end of line interconnection capability of above lying interconnection layers.

The process-flow set forward to realize 3D-SiC [12], as illustrated by Fig. 6. and Fig. 7., is as follows:

- Bonding the device wafer upside down to a temporary carrier
- Wafer thinning the back-side and expose the Cu-nails (remaining Si thickness: ~10μm)
- Backside processing of the thinned wafer (passivation) possible
- (Dicing)
- Wafer to wafer or die to wafer bonding merging the two Cu surfaces to make the interconnections

This process can be repeated to get multiple functional layers. A very high interconnect density can be obtained of 100 peripheral interconnections per mm or equivalently 10000 interconnections per mm^2.

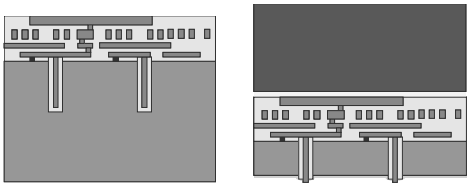


Fig. 6. Schematic representation of the "3D-SIC" Cu-nail via process. Left: Standard CMOS wafer with "Cu-nail" before the BEOL process. Right: Thinned CMOS chip on carrier chip with exposed Cu-nails.

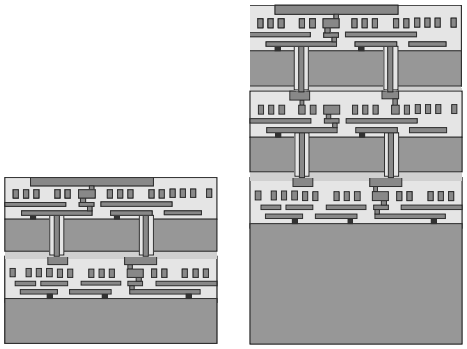


Fig. 7. Schematic representation of a 2and "-layer 3D-SIC stack using Cu-Cu bonding

Despite the apparent simplicity of the process-flow, several issues need to be resolved in order to have a working chipstack. Typical target dimensions for the vias are not standard e.g. 3 µm diameter / 15 µm depth (Fig. 8.), which implies the use of high aspect ratio etching while maintaining a good etch profile as well as barrier deposition and filling the via without the creation of voids. In addition, wafer thinning with a very good control over thickness variation is required both within wafer and from wafer to wafer. Thickness control of the carrier substrate is equally important.

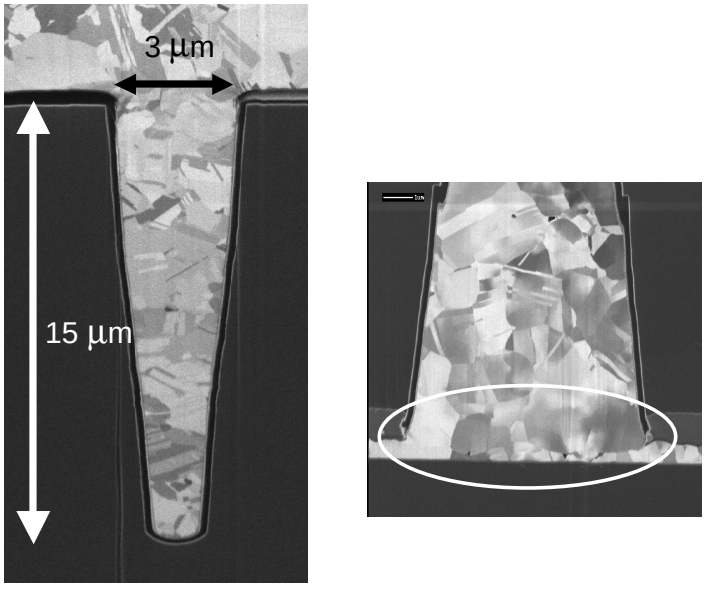


Fig. 8. Cross sectional SEM pictures showing Cu electroplated vias. Left: full profile of a via with positive slope. Conformal barrier deposition is observed. No voids can be seen. Right: Cu-Cu thermo compression bonding interface

3 GENERIC ENABLING TECHNOLOGIES

As already indicated, several non-standard key technologies are needed to realize a chip stack.

3.1 Wafer Thinning and Handling

Wafer thinning is the first key technology, required in all 3D approaches. Thinning technologies in itself are available and quite mature. However, when going to extremely thin substrates, several effects need to be carefully considered.

- First of all the wafers become flexible and very fragile at thicknesses below 100 μm. Handling is thus not straightforward. The best solution is to use a carrier as support during the entire further processing. Temporary adhesives are then needed to fix the thin wafer.
- Very thin wafers exhibit stress relaxation. Stress induced by the devices on the front side relaxes and consequently locally bends the wafer (Fig. 9.). Due to this relaxation, the stress equilibrium changes and as such can modify the device performance.
- A typical (extreme) thinning process consists of multiple steps amongst which are possibly grinding, polishing, CMP and etching. Damage done by grinding can extend several microns deep into the substrate and can ultimately affect the device performance or cause failures during further processing (like bonding). For bulk removal of the substrate, grinding is however the most economically viable approach, therefore it is always the first step in the thinning process. The second thinning step is usually incorporated for removal of damage (and associated stress) induced by the grinding.

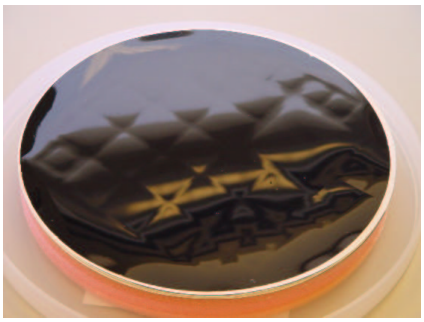


Fig. 9. A 200mm unsupported 40 μm thin device wafer, exhibiting local stress relaxation.

3.2 High Aspect Ratio Etching

To make the vias or through wafer interconnections a fairly deep hole (compared to its width) needs to be etched, the ratio of depth over width is called aspect ratio (AR). High aspect ratio etching (AR>2) is done typically by (D)RIE ((Deep) Reactive Ion Etching). When using DRIE, higher aspect ratios can be obtained, however the pulsed nature of this process can give rise to negative slopes. Negative slopes, however small they are, should be avoided since subsequent depositions (like PECVD or plasma enhanced chemical vapor deposition) might need a direct line of sight.

3.3 Wafer Bonding

Evidently wafer bonding technology is essential for a production worthy process. Little has been published on full wafer bonding. For wafer bonding, the main challenge is bonding uniformity and its effect on yield and reliability.

4 SPACE APPLICATIONS

Several key technologies used in 3D integration are also used for a variety of space applications. Multiple applications being developed at IMEC fit in the proposed 3D approaches or are using these technologies.

4.1 Hybrid Far-IR Detector (2D)

A first example considers the development of BIB (Blocked Impurity Band) detectors for ESA. This type of detectors works only at cryogenic temperatures in a regime where the impurities or dopants are not ionized by thermal energy. Ionization of impurities can however occur due to incident IR light, by which the channel resistance changes, which can be measured.

The investigated concept utilizes flip chip hybridization on a cryogenic ROIC using In micro bumps with 30 µm pitch (Fig. 10.). In operating mode, the detector is backside illuminated through a high resistivity –non absorbing– substrate.

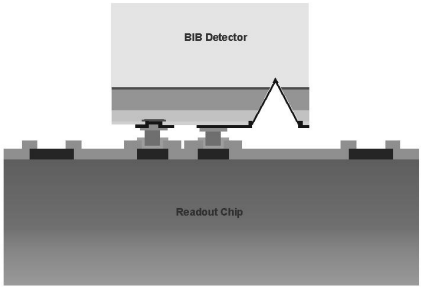
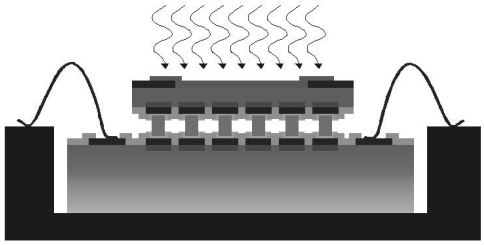


Fig. 10. Schematic representation of a hybridized linear BIB detector

4.2 Hybrid APS Sensor (2.5D)

In the field of CMOS imaging, a large gain in quantum efficiency can be obtained, using backside instead of frontside illumination. In this case, no light is lost due the Back-End of the imager (dielectrics as well as metal interconnections). But, backside illumination requires more complicated processing similar to techniques used in 3D integration. I.e. depending on the minority carrier diffusion length the sensor array needs to be thinned down to residual thicknesses of ~30 µm. By using an optimized ARC (Anti Reflective Coating), quantum efficiencies of 80-90% can be achieved over the entire visible spectrum. Thinning down the sensor array however, needs to be done with care. Any damage induced at the backside of the imager is detrimental for the quantum efficiency of the device since defects act as recombination centers for the light generated electron-hole pairs. Therefore, additional backside surface treatment after thinning and before ARC deposition is needed to reduce surface recombination.

One of the concepts being developed for ESA at IMEC in cooperation with Fill Factory (Cypress) and Galileo Avionica is schematically represented in Fig. 11. (Left). It consists of a thinned 1024 by 1024 pixel sensor array, flip chipped on top of a ROIC with 22.5 µm pitch In micro bumps. As seen in Fig. 11 (Right), the measured quantum efficiency on a diode with a non-optimized ARC is above 60% between 450nm and 800nm.



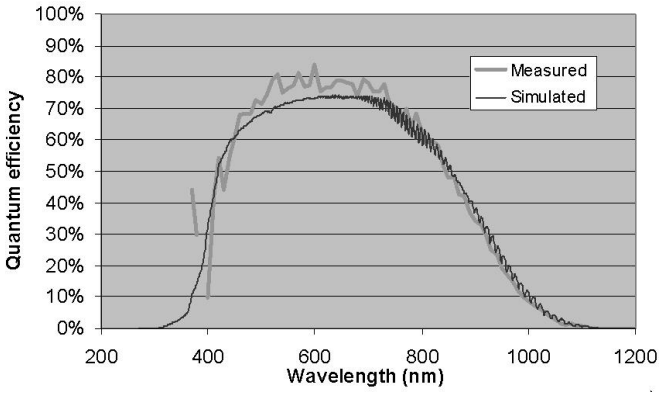


Fig. 11. Left: Schematic representation of a thinned hybridized imager wire bonded to its package. Right: Quantum efficiency as function of wavelength of a diode with surface treatment and a non-optimized ARC.

4.3 3D RF Circuits

For certain space applications, high quality miniaturized RF circuitry, incorporating discrete passive components, is needed. To be able to realize this, high performant, high frequency RF feedthroughs are required. In addition, through wafer vias and moderate wafer thinning are mandatory to connect ground layers located on different layers, hereby preventing parasitic modes and its associated coupling.

The RF feedthroughs have to be thought off as being an inherent part of the circuit and must be functional at frequencies in the GHz range and beyond.

5 CONCLUSION

3D integration offers solutions to the limitations of today's electronic systems. The technology has the potential to effectively reduce power consumption while simultaneously increasing performance and decreasing chip volume.

A variety of 3D integration approaches (3D-SiP, 3D-WLP and 3D-SiC) and technologies are being developed. One area benefiting from this research is the one of space applications. Especially wafer thinning and micro bumping technology are interesting in the field of imagers, 3D RF components, etc…

Although 3D integration has long been considered not a viable technology, it is gradually gaining momentum and is likely to become mainstream chip technology.

6 REFERENCES

[1] E.Beyne, "System driven approaches to 3D integration", *The 4th Intermational Symposium on Microelectronics and Packaging*, Seoul, S-Korea, September 28, 2005.

[2] *Proc. of the 1st and 2nd conf.* on "3D Architectures for Semiconductor Integration and packaging", *RTI international*, Burlingame, California, April 13-15, 2004 and Tempe, Arizona, June 13-15, 2005

[3] E.Beyne, "3D Interconnection and packaging: impending reality or still a dream?" *proceedings of the IEEE International Solid-State Circuits Conference, ISSCC2004*, 15-19 February 2004; San Francisco, CA, USA, IEEE, 2004, pp.138-145.

[4] Phil Garrou, "3D Integration: A status report", *proceedings "3D Architectures for Semiconductor Integration and packaging", RTI international*, Burlingame, Tempe, Arizona, June 13-15, 2005.

[5] Scott List, "The third dimension: fact or fiction?" idem [3]

[6] Albert Young, "Perspectives on 3D-IC technology" idem [3].

[7] A.Klump et al. "3D Integration of CMOS Transistors with ICV-SLID Technology" idem [3].

[8] Manuba Bonkohara, "Technologies for 3D assembly and chip level stack" *Proceedings of 2nd International Symposium on Microelectronics and Packaging, ISMP2003*, IMAPS-Korea, Seoul, Korea, September 24-25, 2003,, pp.85-90.

[9] E.Beyne, "Technologies for very high bandwidth electrical interconnects between next generation VLSI circuits", *IEEE-IEDM 2001 Technical Digest*, December 2-5, Washington, D.C., S23-p3, 2001.

[10] S. Stoukatch, M. Ho, K. Vaesen, T. Webers, G. Carchon, W. De Raedt, E. Beyne, J. De Baets, "Miniaturization using 3-D stack structure for SIP application", *Proc. SMTA (Surface Mount Technology Association) International Conference*, 21-29 September 2003; Chicago.

[11] T. Torfs, S. Sanders, C. Winters, S. Brebels, C. Van Hoof, "Wireless network of autonomous environmental sensors", *Proceedings of IEEE Sensors 2004*, Vienna, 24-27 October 2004.

[12] J.H.McMahon et al., "Wafer bonding of damascene-patterenced metal/adhesive redistribution layers for via-first 3D Interconnect", Proc. of the 55th ECTC, , Orlando, Florida, May 31-June 3, 2005, pp. 332-336