

## 5th ESA Round Table on Micro/Nano Technologies for Space

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### **NEW 3-D TECHNOLOGY FOR ULTRA LOW VOLUME MICROSYSTEM**

#### **PRESENTATION OF WALPACK TECHNOLOGY**

This new stacking technology in 3-D was part of an important EUREKA/PIDEA study from 2001 to 2004 in collaboration with following companies: ST Microelectronics, CEA/LETI, Schlumberger/Axalto, Thales, etc.

3D Plus launched this programme in order to keep an advantage with regard to 3-D stacking and particularly to this stack thickness parameter.

As far as the thickness of both the components and 3-D modules are concerned, the worldwide tendency is very strong.


Thanks to this study, we can stack any type of bare die as well as passive components. The objective of 8 levels per mm has been achieved and has already led to some applications.

Criteria, which have been retained for the building of ultra low profile cubes, are the same ones as those retained when we launched the 3-D technology in 1990, i.e.

- Use of standard components “COTS”
- Use of any type of components and not only memories (passive components, MEMS)
- Electrical test of each level prior to stacking

The applications of these principles led us to be in an opposite position compared to most of the 3-D thin stacking developments carried out in Europe, in the USA and in Asia: as a matter of fact, in order to get ultra low profile cubes, these people all started with wafer or thinned dice (several 10 µm or several 100 µm).

Of course, these dice do not exist (DDR SDRAM memories, microprocessors, FPGA, etc) and indeed especially not for small quantities, like for Aerospace, Medical and industry.



## MAIN CRITERIA RETAINED FOR WALPACK

We have utilised roughly the same criteria as those which allowed us to launch the 3-D technology about 10 years ago :

- Use of standard dice (no KGD)
- Use of standard thickness dice, and non thinned like with most of our Japanese and Asian competitors
- Wireless technology
- Electrical tests prior to stacking, contrary to the present trend to stack the wafers





Fig. 1 Main criteria retained for WALPACK

## WALPACK TECHNOLOGY APPLICATIONS

Two applications have been launched:


### Memory applications


. 8 SRAM memories are stacked in a cube of 1.3 mm thickness with the balls included.




### 3D APPLICATION – Demonstrator

- ✓ Memory: 2Gb
- ✓ 35 In/out
- ✓ Size : 1,8 x 6.5 x 1.3mm<sup>3</sup>





Stacking of 8 SRAMs






Fig.2 Micro stimulator

. Medical application of a micro stimulator for Alfred Mann Foundation in California, which chose 3D Plus among 100 companies worldwide: 5 ASIC are stacked in a thickness of 0.7 mm, the whole in a 3 mm<sup>3</sup> volume.

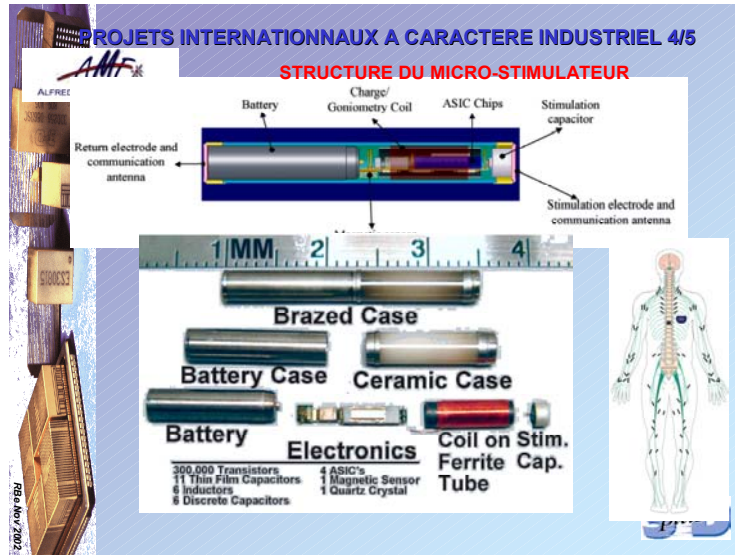


Fig. 3 Industrial oriented international projects

## **MEMS COMPATIBILITY WITH WALPACK TECHNOLOGY**

MEMS or actuators integration brings very specific problems :

- hermeticity, in order to avoid humidity as well as outgazing products of organic materials
- no continuity, no stress should be applied to these structures.

These 2 very strong constraints can be perfectly mastered in the 3-D stacking process.

### **Protection against humidity**

We have a double approach depending on the requested hermeticity level:

#### Partial hermeticity approach:

It is possible to locally protect this type of component against humidity, thanks to a SiO<sub>x</sub> inorganic deposition. As a matter of fact, a thin coat of around 0.5 μm of this pseudo plastic material allows to make a barrier to water and gaz in general (oxygen, azote, etc).

Two applications are presented:

. Application to gyro:

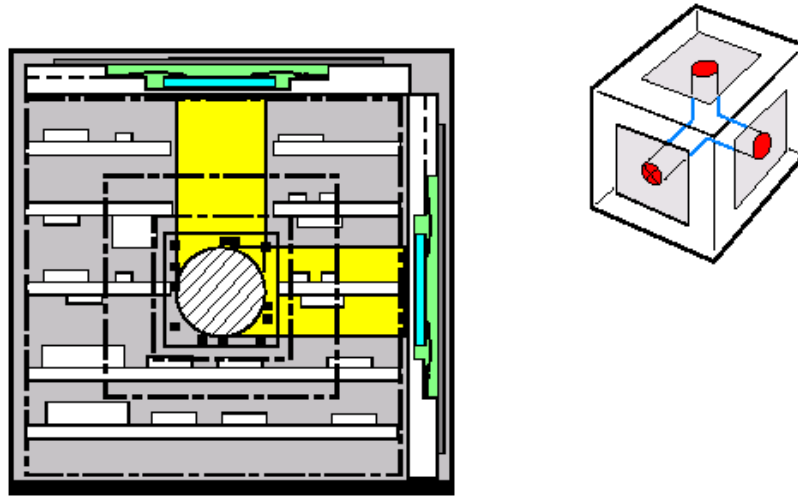


Figure 1 : Avec chip carrier céramique

Fig. 4 Application to Gyro

. Applications to MEMS wafers (wafer level process) : Fig. 5

### Ruggedizing of the MEMS / Chip Size Package (wafer level process)

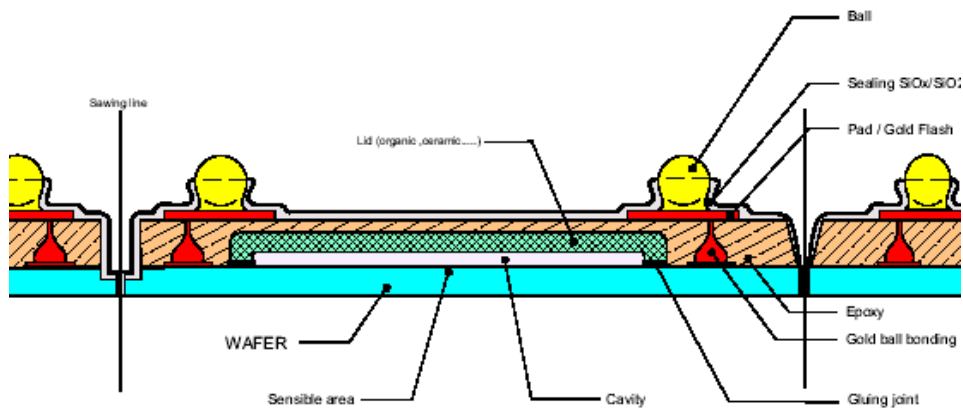


Fig. 5 : Wafer level process

It can be noticed that the sensitive part of the MEMS is protected by a lid of low thickness, the mineral coat being deposited after partial dicing of the wafer.

Fully hermeticity approach

In order to be sure that we do not have any outgazing and to guarantee a full hermeticity, we use what has been named "Opposite twin cavities technology". We can observe that the HTCC, even LTCC ceramic technologies are used in order to obtain 2 perfectly opposite cavities, which leads to zero stress (Fig. 6)

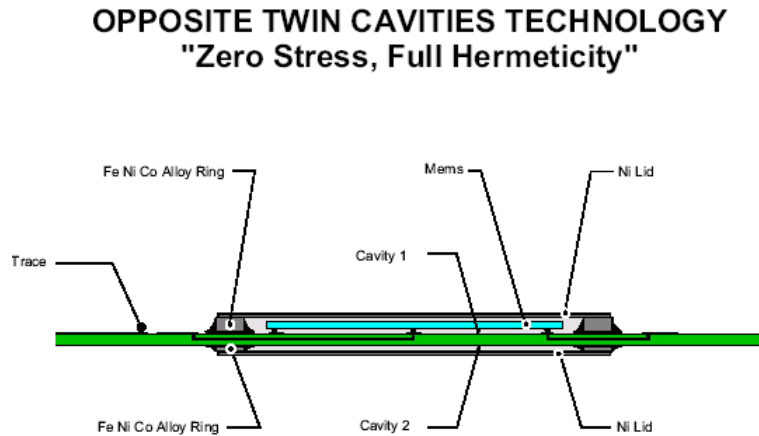


Fig. 6 Opposite twin cavities technology

We represented on Fig.7 the 3-D integration of the protected MEMS :

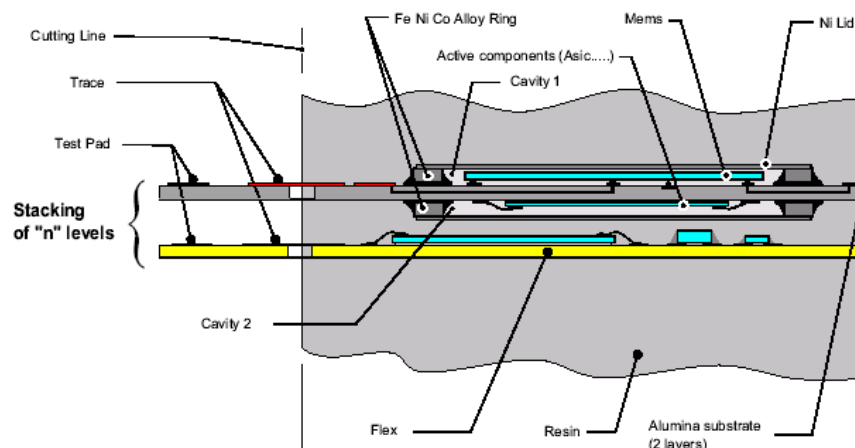


Fig.7 3-D integration of the protected MEMS

It is obvious that the stresses induced by the moulding of the 3-D cube will have no effect on the MEMS.

Several MEMS can of course be stacked associated with their associated electronics.

## **CONCLUSIONS AND PERSPECTIVES**

This very dense stacking technology allows to make a significant advance in MEMS integration.

We have observed that it was possible to build complex micro stimulators in 3 m<sup>3</sup>, which leads to the building of functional bricks of several mm<sup>3</sup>, which will lead us to propose a Satellite in a Cube.