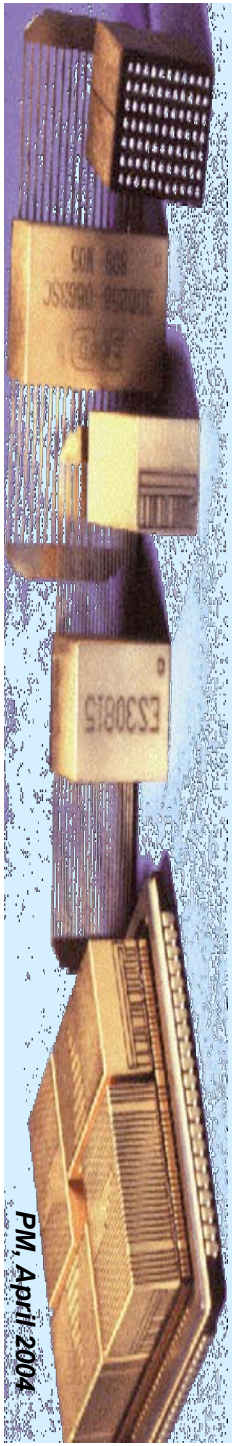
3D PLUS stacking Technology:

ESA/CNES capability approval and Main 3D Products dedicated to Space Applications

28 April 2004 – ESTEC - Noordwijk
Technical presentations Day on
Microelectronic Packaging technologies

www.3d-plus.com
641, Rue Hélène Boucher
78532 BUC - FRANCE



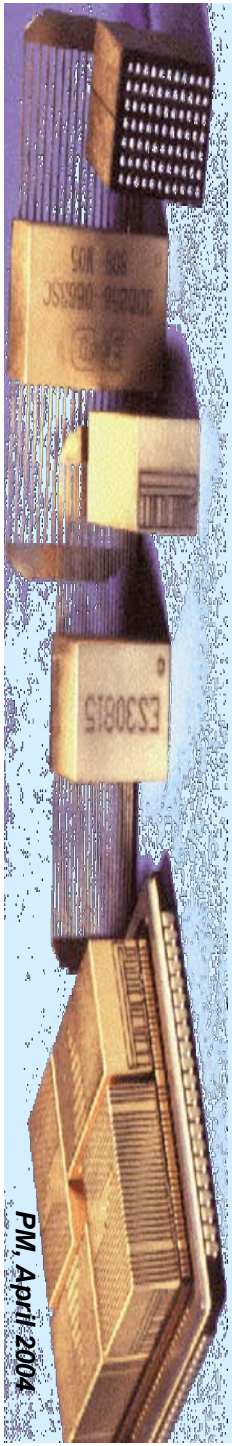
Capability approval of 3D Plus for the manufacturing of 3D modules

1. Introduction
2. Evaluation Phase
3. Approval Phase
4. Process Identification Document (P.I.D.)

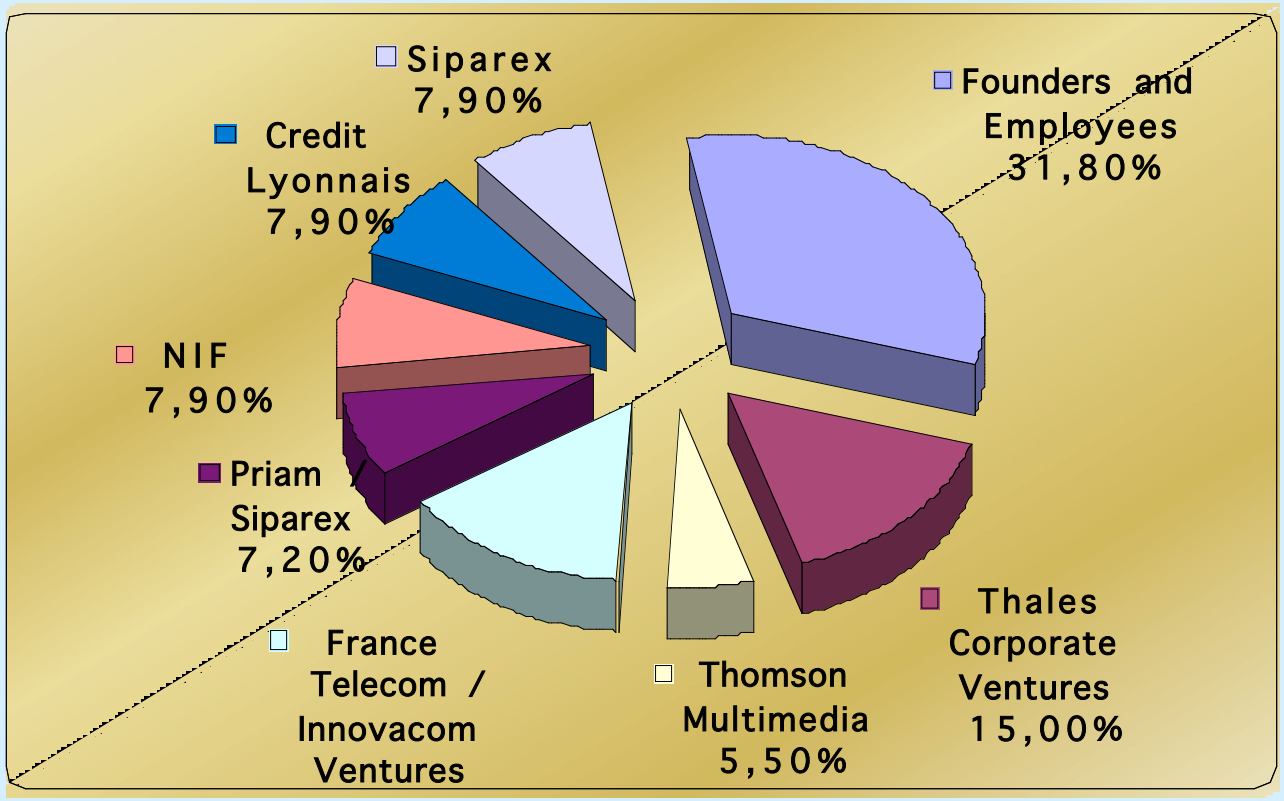
1. Introduction

3D Plus Presentation - Milestones

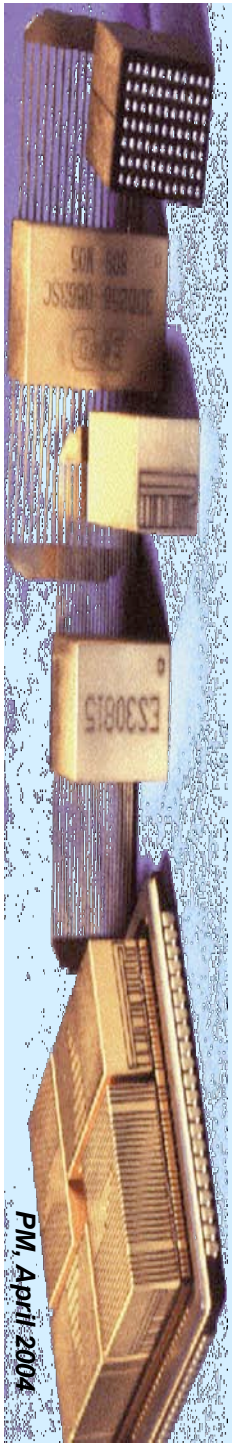
- 3D Plus mission statement is to design, manufacture and sale 3D products according to its patented vertical stacking technology.
- 1995: Company creation by C. VAL who was previously member of scientist and technical council of Thomson Group
- 2001: 3D Plus set up a sales subsidiary in Mc Kinney, Texas, USA.
- 2001: The Hi-Rel production Line was successfully evaluated by CNES, ESA and NASA.
- 2002, 3D Plus released an increase of capital and built a new manufacturing plant in BUC, France for medium series manufacturing.
- 2003: ISO 9001-(2000) certification
- 2004: Many modules in Orbit: Memories (Cluster 2, Envisat,…), Micro-cameras (Rosetta, Proba, …), Micro-Computers (Mars express, Rosetta, …), …



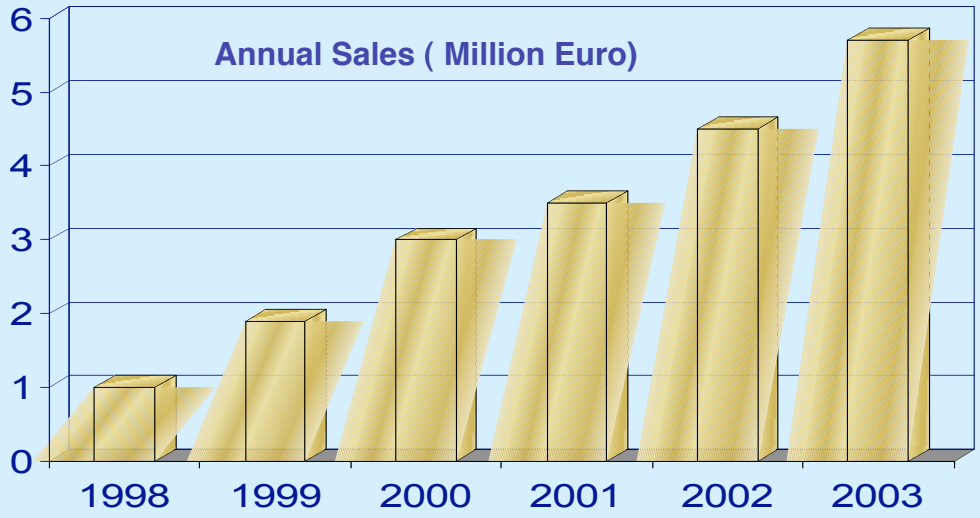
Company – Shareholders



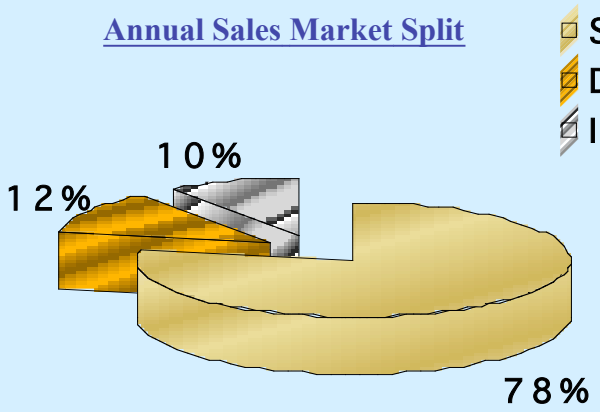
- **Capital : 1 139 780 Euros**
- **3D PLUS is an independent Company**



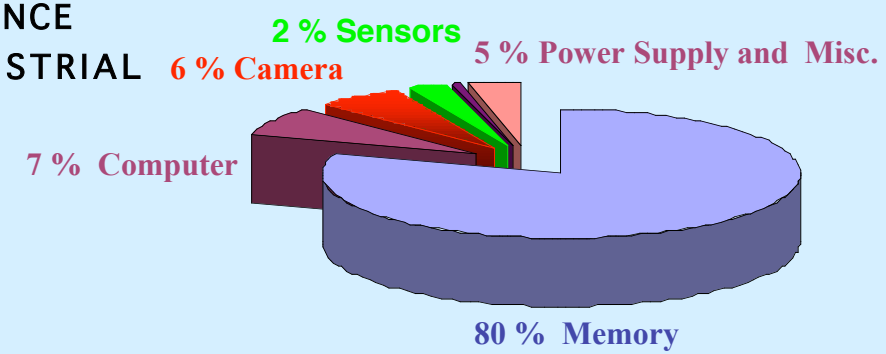
Company – Key figures



Annual Sales Market Split



Annual Sales Product Split



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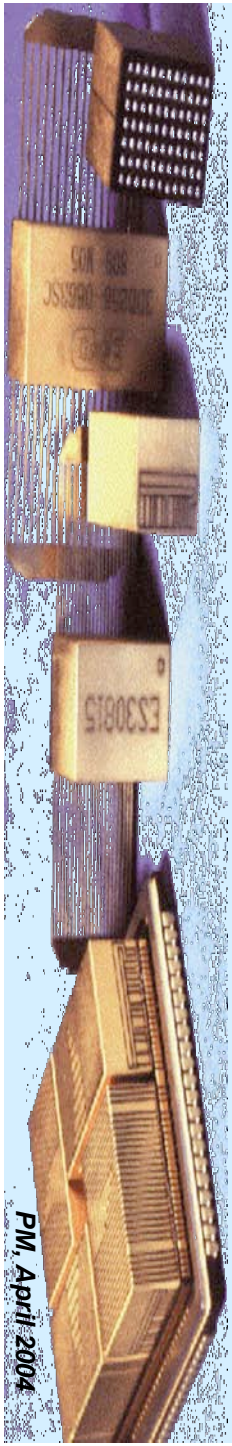


Company – Locations

3D*plus* Head-Office,
Design and Technology Center,
High Rel. Manufacturing line qualified for Space Applications :

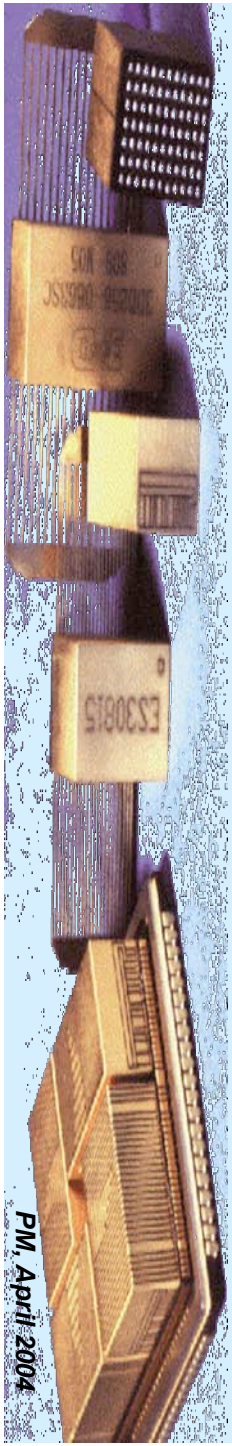
641, rue Helene-Boucher
78532 Buc, France

3D*plus* Medium Series Manufacturing Line :

423, rue Audemars
78532 Buc, France

3D*plus* USA :
Marketing and Sales Office for North America

2570 Eldorado Parkway, Suite 150
McKinney, TX 75070, USA



Company – Organization Chart

Hi-Rel Business Unit Organization

Business Unit Hi-Rel

Responsibility:
Inc. Statement of the Business Unit

P.Maurice

Quality Assurance Group

D. Blain

New Projects Group

Resp. J.F.Goupy
M.C. Vassal

Design & IT Group

R. Bocage

Hi-Rel Process & Purchasing Group

F.Soufflet

Hi-Rel Manufacturing line

P.Prieur

Test Group

T.Dargnies

Rattached to sales Group

Hi-rel Sales Group

Responsibility:
Hi-Rel Booking - Non USA

R.Frank

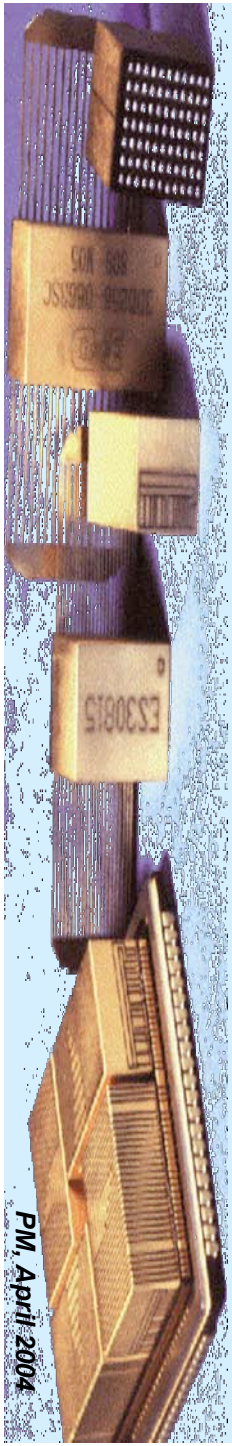
3D+ USA Hi-Rel activity

Responsibility:
Hi-Rel Booking - USA

J.Quinn

Total : 60 persons

Company – Our Rep Network



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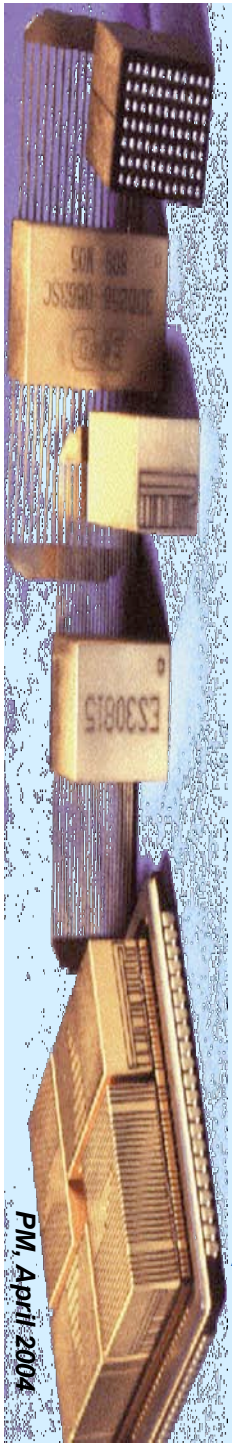
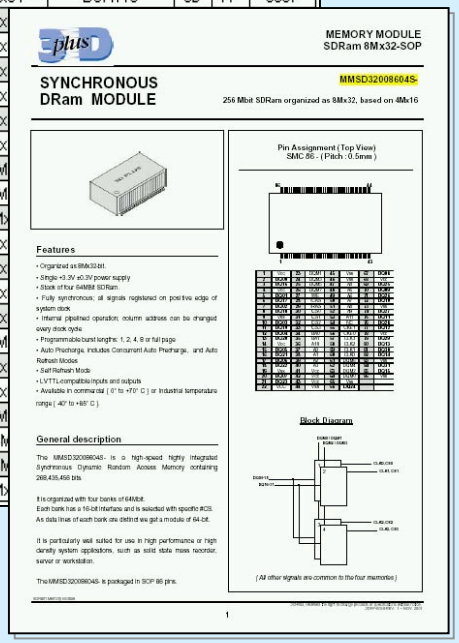


3D PLUS Standard Products

SDRAM MEMORY							
3DSD256-083	256 Mbit SDRam based on 8Mx8 - SYNCHRONOUS	32Mx8	SOP54	3D	FP	0009
MMSD32008604S-	256 Mbit SDRam based on 4Mx16 - SYNCHRONOUS	8Mx32	SOP86	3D	FP	0050
4004604B-	256 Mbit SDRam based on 4Mx16 - SYNCHRONOUS	4Mx64	BGA119	3D	FP	0032
4604Q-	256 Mbit SDRam based on 4Mx16 - SYNCHRONOUS	4Mx64	QFP126	3D	FP	0042
	512 Mbit SDRam based on 8Mx8 - SYNCHRONOUS	64Mx8	SOP54	3D	FP	0006
04B-	512 Mbit SDRam based on 8Mx16 - SYNCHRONOUS	8Mx64	BGA119	3D	FP	0034
8B-	512 Mbit SDRam based on 4Mx16 - SYNCHRONOUS	8Mx64	BGA119	3D	FP	0035
Q-	512 Mbit SDRam based on 4Mx16 - SYNCHRONOUS	8Mx64	QFP126	3D	FP	0043
Q-	512 Mbit SDRam based on 8Mx16 - SYNCHRONOUS	8Mx64	QFP126	3D	FP	0044
S-	512 Mbit SDRam based on 8Mx16 - SYNCHRONOUS	16Mx32	SOP86	3D	FP	0051
	1 Gbit SDRam based on 64Mx4 - SYNCHRONOUS	128Mx8	SOP54	3D	FP	0007
6Q-	1 Gbit SDRam based on 8Mx16 - SYNCHRONOUS	16Mx64	QFP126	3D	FP	0045
08B-	1 Gbit SDRam based on 8Mx16 - SYNCHRONOUS	16Mx64	BGA119	3D	FP	0037
6004Q-	1 Gbit SDRam based on 16Mx16 - SYNCHRONOUS	16Mx				
16604B-	1 Gbit SDRam based on 16Mx16 - SYNCHRONOUS	16Mx				
2032604S-	1 Gbit SDRam based on 16Mx16 - SYNCHRONOUS	32Mx				
072016605B-R	1 Gbit SDRam based on 16Mx16 - SYNCHRONOUS	16Mx				
3DSD1280-323H	1,28 Gbit SDRam based on 16Mx16 - Hermetic package	40Mx				
MMSD32064604S-	2 Gbit SDRam based on 32Mx16 - SYNCHRONOUS	64Mx				
3DSD2048-083	2 Gbits SDRam based on 64Mx8 - SYNCHRONOUS	256M				
MMSD08256404S-	2 Gbits SDRam based on 128Mx4 - SYNCHRONOUS	256M				
3DSD2048-163	2 Gbits SDRam based on 32Mx8 - SYNCHRONOUS	128Mx				
MMSD64032608B-	2 Gbit SDRam based on 16Mx16 - SYNCHRONOUS	32Mx				
MMSD64032604B-	2 Gbit SDRam based on 32Mx16 - SYNCHRONOUS	32Mx				
MMSD640326080-	2 Gbit SDRam based on 16Mx16 - SYNCHRONOUS	32Mx				
MMSD640326040-	2 Gbit SDRam based on 32Mx16 - SYNCHRONOUS	32Mx				
MMSD08256808S-	2 Gbit SDRam based on 64Mx4 - SYNCHRONOUS	256M				
MMSD64064608Q-	4 Gbit SDRam based on 32Mx16 - SYNCHRONOUS	64Mx				
MMSD64064608B-	4 Gbit SDRam based on 32Mx16 - SYNCHRONOUS	64Mx				
MMSD08512808S-	4 Gbit SDRam based on 64Mx8 - SYNCHRONOUS	512M				
MMSD04102408S-	4 Gbit SDRam based on 128Mx4 - SYNCHRONOUS	1024M				
MMSD04102408S-E	4 Gbit SDRam based on 128Mx4 - SYNCHRONOUS	1024M				
MMSD321606200-	5.12Gbit SDRam based on 64Mx16 - SYNCHRONOUS	160Mx				



MEMORY MODULE
SDRam 8Mx32-SOP

SYNCHRONOUS
DRam MODULE

MMSD32008604S-

256 Mbit SDRam organized as 8Mx32, based on 4Mx16

Features

General description

Block Diagram

MEMORY MODULES,
COMPUTER MODULES,
CAMERA HEADS,
SENSORS,
DC/DC CONVERTERS.

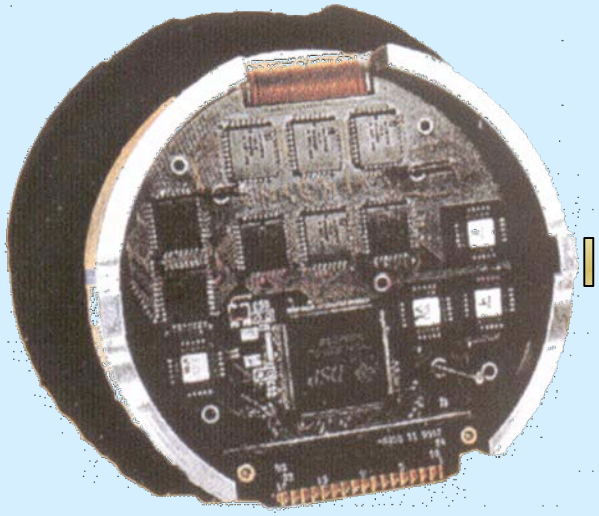
CD-ROM Menu: Standard Product List, Flyers, Data sheets, User guides, Applications Notes, Starter Kits…

PM, April 2004

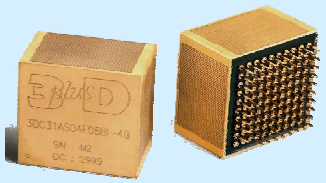
Custom, semi-custom Products

- **Custom and Semi-custom Products**
  - **System In Package (S.I.P)**
    - **Hight density packaging with interconnection in 3 dimensions.**
    - **Drastic size, volume, weight reduction**

Micro-computer in SMT Technology

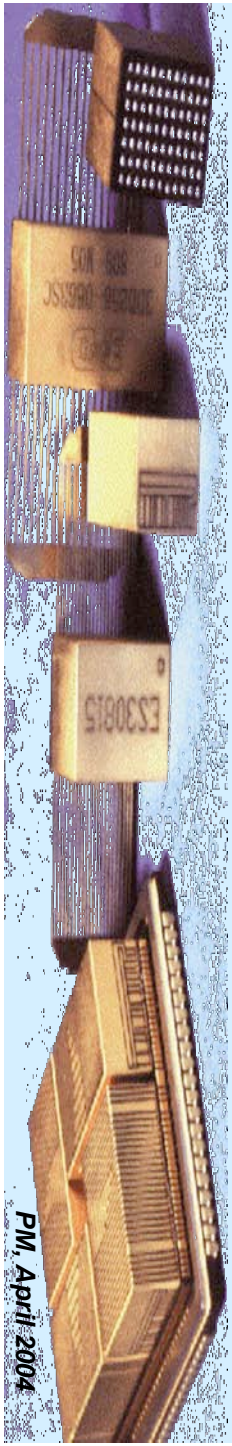


Micro-computer in 3D Technology

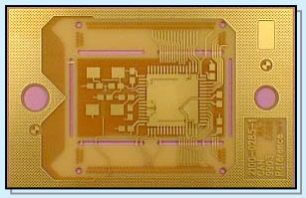


On this example, gain of : 14 times in weight ,
16 times in volume

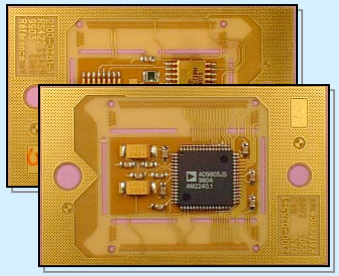
Technology Flow Charts (Flex Stacking Process – Flow 2)

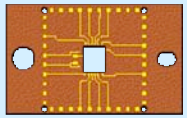


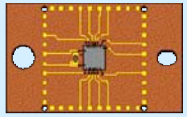
1) - Flex Design

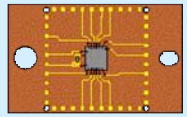


2) – Components attachment



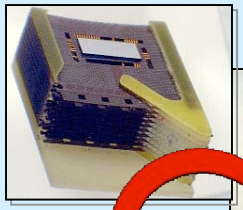




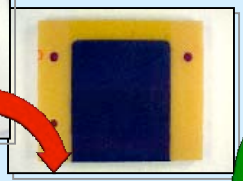


3) - Circuit Test & Screening

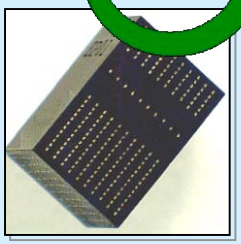
4) – Layers Stacking



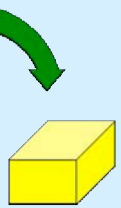
5) – Cube Molding

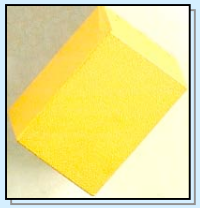


6) – Cube Sawing

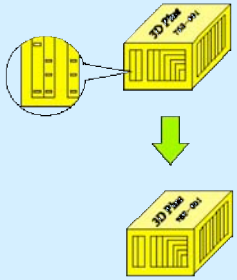


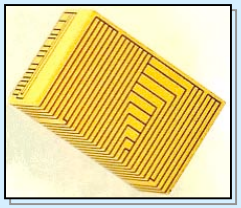
7) – Cube Plating (Ni + Au)



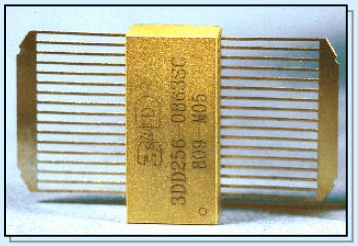


8) – Circuit interconnection by laser grooving





9) – Cube Test & Screening



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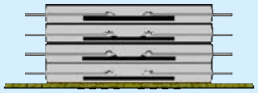
Technology Flow Charts (TSOP Stacking Process – Flow 1)

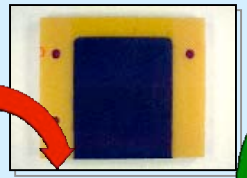
1) – Package Selection and Procurement (TSOP, …)

2) – Component Pins de-bending

3) – Components Stacking



4) – Cube Molding



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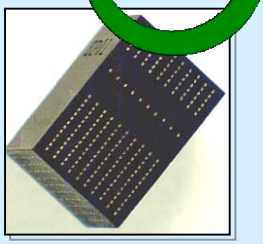
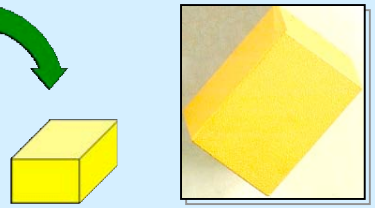
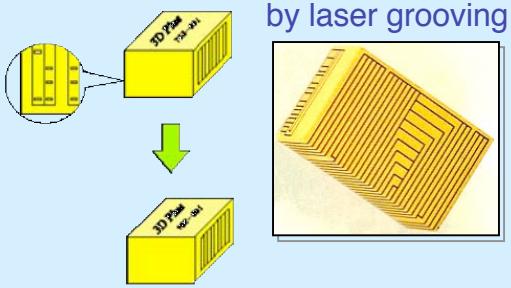


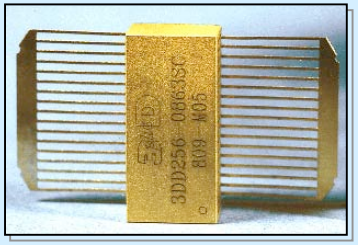
6) – Cube Plating (Ni + Au)



7) – Circuit interconnection by laser grooving



8) – Cube Test & Screening



plusD

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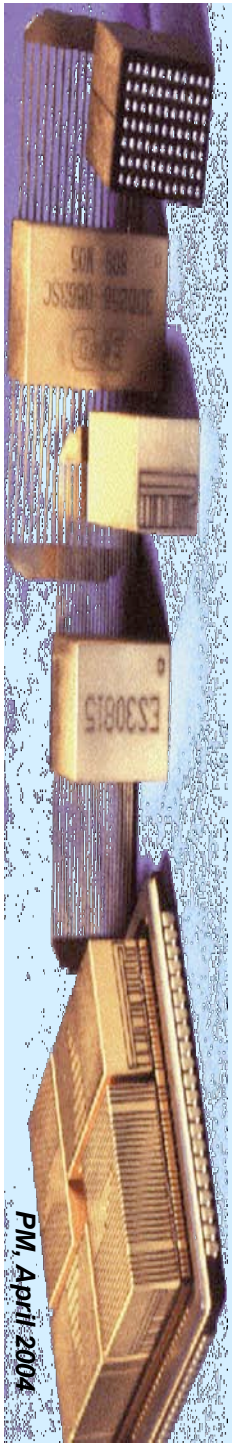
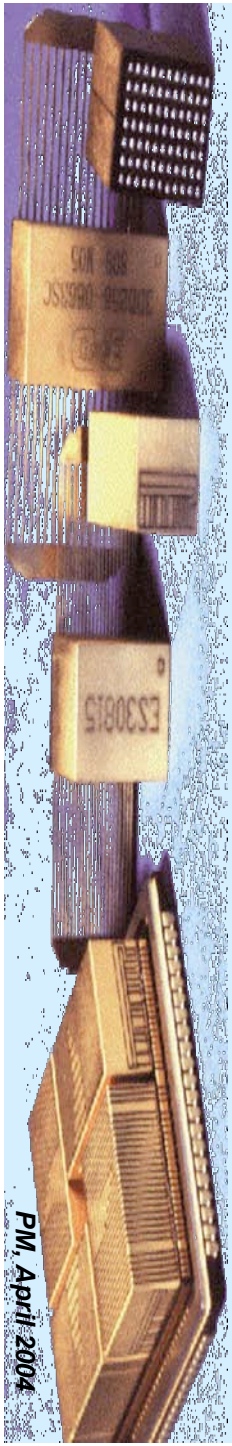


Main Features and Benefits

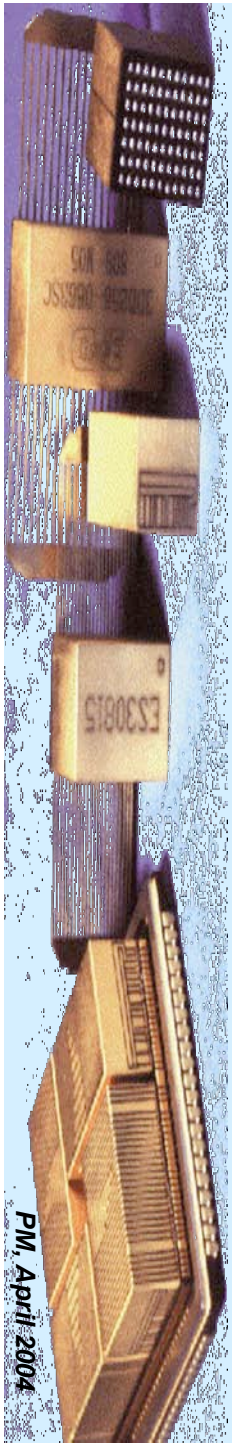
The components are stacked up	→	Size reduction on the PCB, weight savings for the application.
The components are fixed into resin	→	High mechanical resistance (vibrations, shocks, …) Humidity resistance enhancement Each epoxy resin lot is tested “Known Good Resin”
The interconnection is reduced and simplified	→	Higher electrical performance, electrical signal integrity
The components are shielded	→	Parasitic effect decrease, EMI enhancement
Simplified Manufacturing processes	→	Flexibility and short development time of new designs Cost effectiveness, short manufacturing lead times due to the use of simple and well proven technologies



ESA/ CNES Space certification Methodology

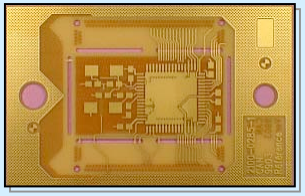
- **The capability Approval sequence of events:**
  - **-Evaluation testing phase**
  - **-Process Identification Document (PID)**
  - **-Approval testing phase**

- **Implementation with the 3D Plus stacking technology: a coordinated effort of ESA and CNES**
  - **-Evaluation phase and PID Draft completed in august 2001**
    - *** Definition of material and processes to be evaluated**
    - *** Design of the test structure and PID draft**
    - *** Manufacturing of test structures and Evaluation testing**
  - **-Approval phase started in September 2001**
    - **•Manufacturing of test structures according to PID (completed feb. 2004)**
    - **•Testing phase (completed april 2004)**
    - **•Completion of PID and associated procedures (outstanding action)**

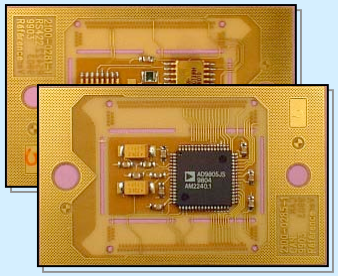


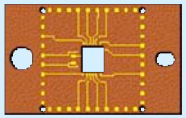
2. Evaluation Phase
2.1 Technological Domain

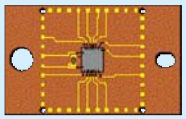
1) - Flex Design

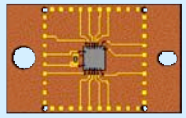


2) - Component assembly



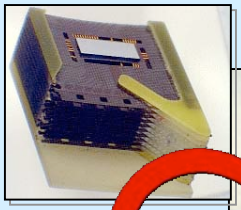




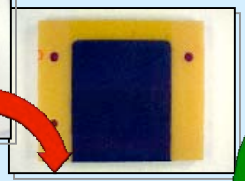


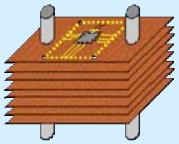
3) - Circuit Test & Screening

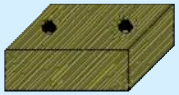
4) –Flex Stacking

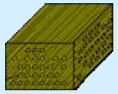


5) – Cube Molding

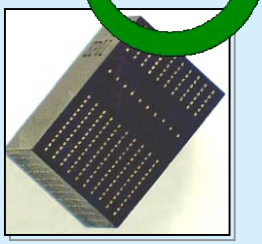




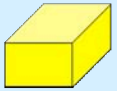


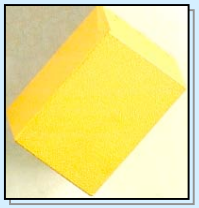


6) – Cube Sawing

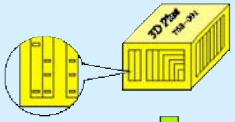


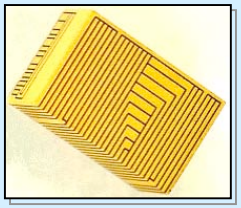
7) – Cube Plating (Ni + Au)



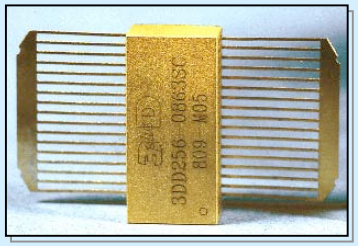


8) – Circuit interconnection by laser grooving

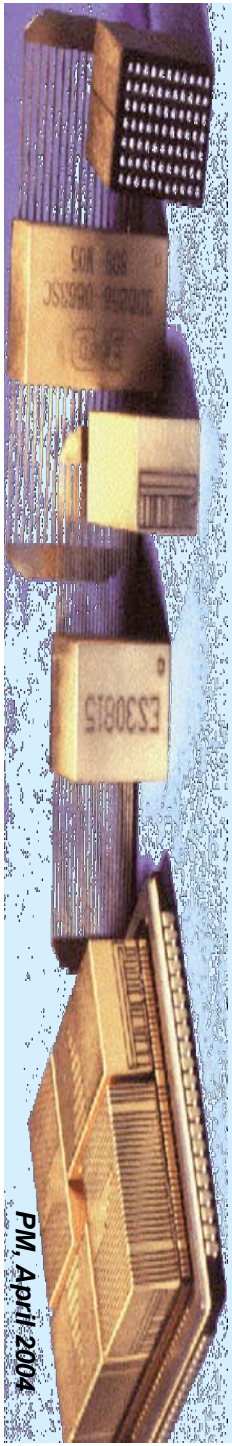




9) – Cube Test & Screening

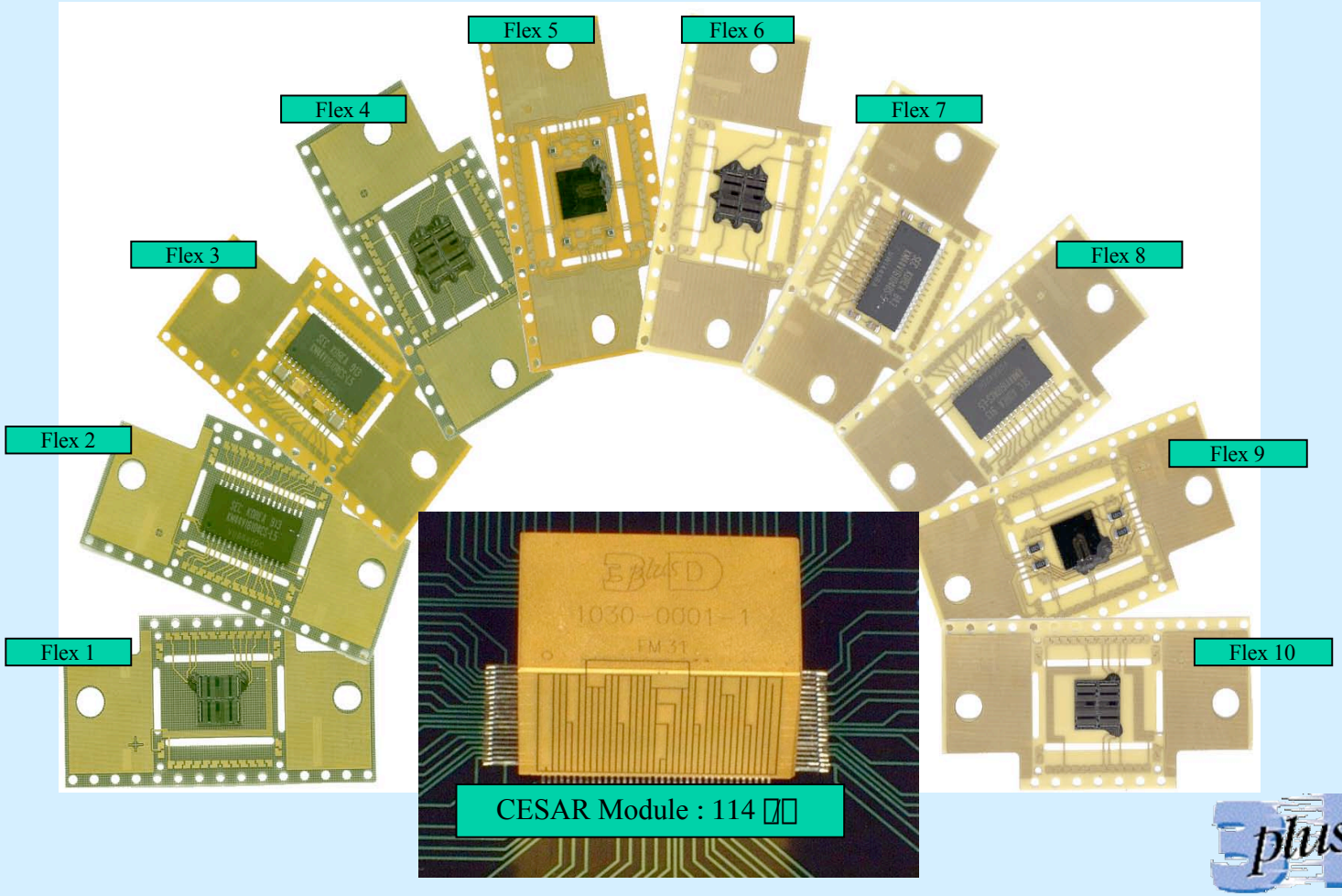


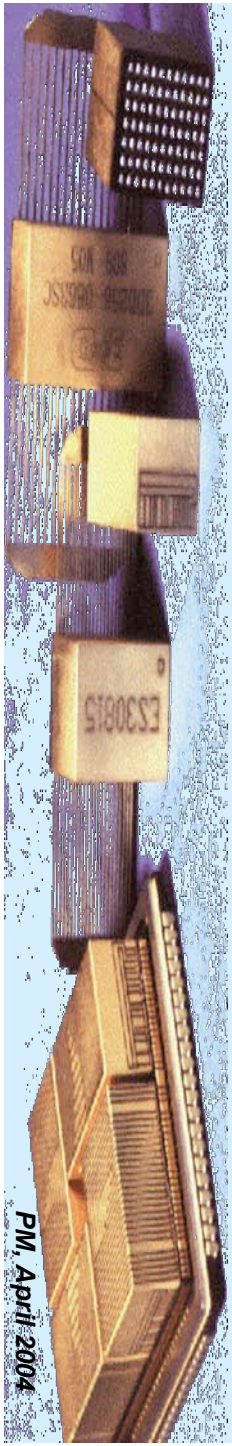
PIM, April 2004



2.2 Evaluation Test Structure

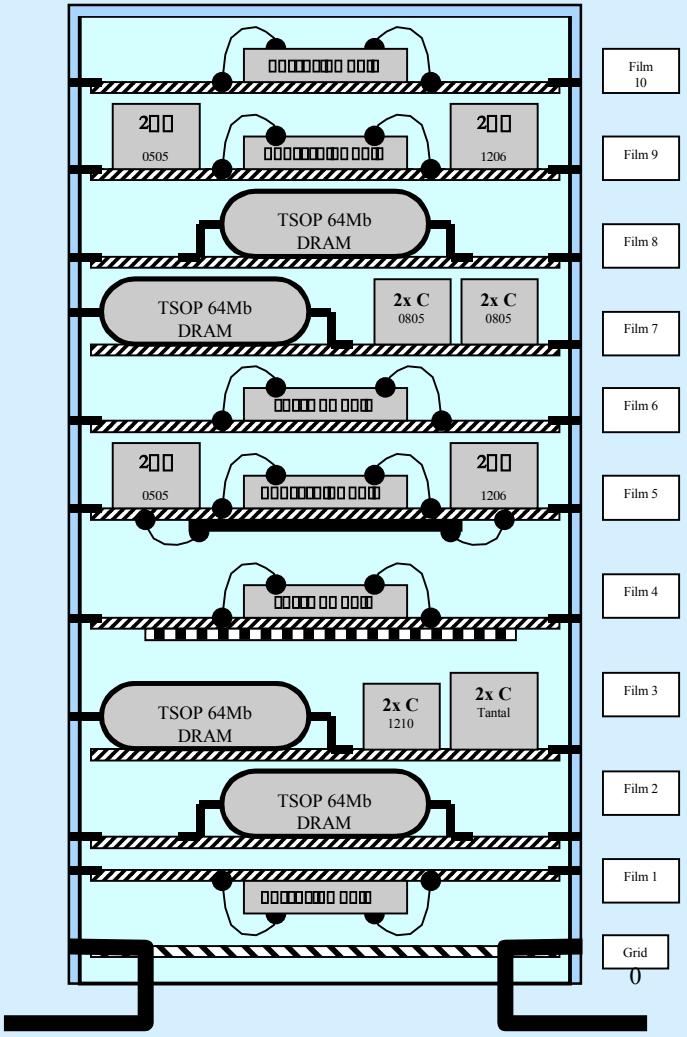
- **CESAR= Cnes ESA thRee d-plus**





CESAR Definition and Cross Section

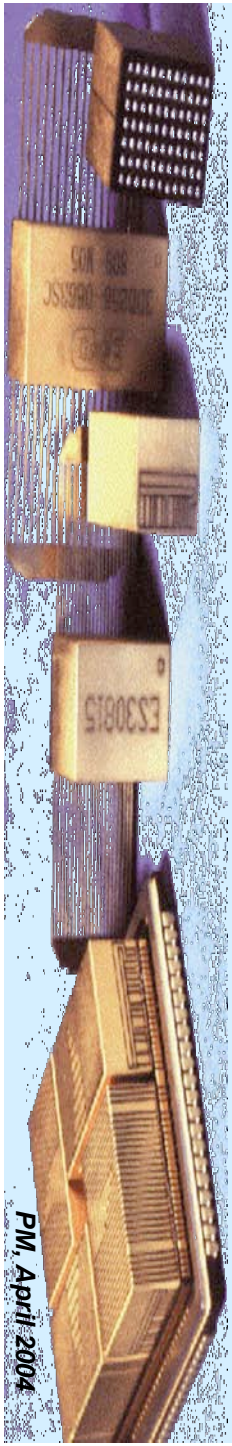
- Module : test vehicle integrating 4 TSOP 64 Mb, 8 chip capacitors, 8 chip resistors, 2 thermal sensors, 2 mechanical constraint sensors.
- 10 internal layers + Leadframe layer
- Dimensions : 26 * 15 * 16,2 mm
- Number of I/Os : 114
- Flex assembly technologies involved:
  - * Epoxy attach and Wire bonding
  - * hand soldering
- EEE Components packages involved:
  - * Bare silicon die (PMOS4 test chip and ACM Strain gauges)
  - * TSOP type II (64Mb DRAM EDO)
  - * Ceramic and Tantalum capacitors
  - * Resistors chips



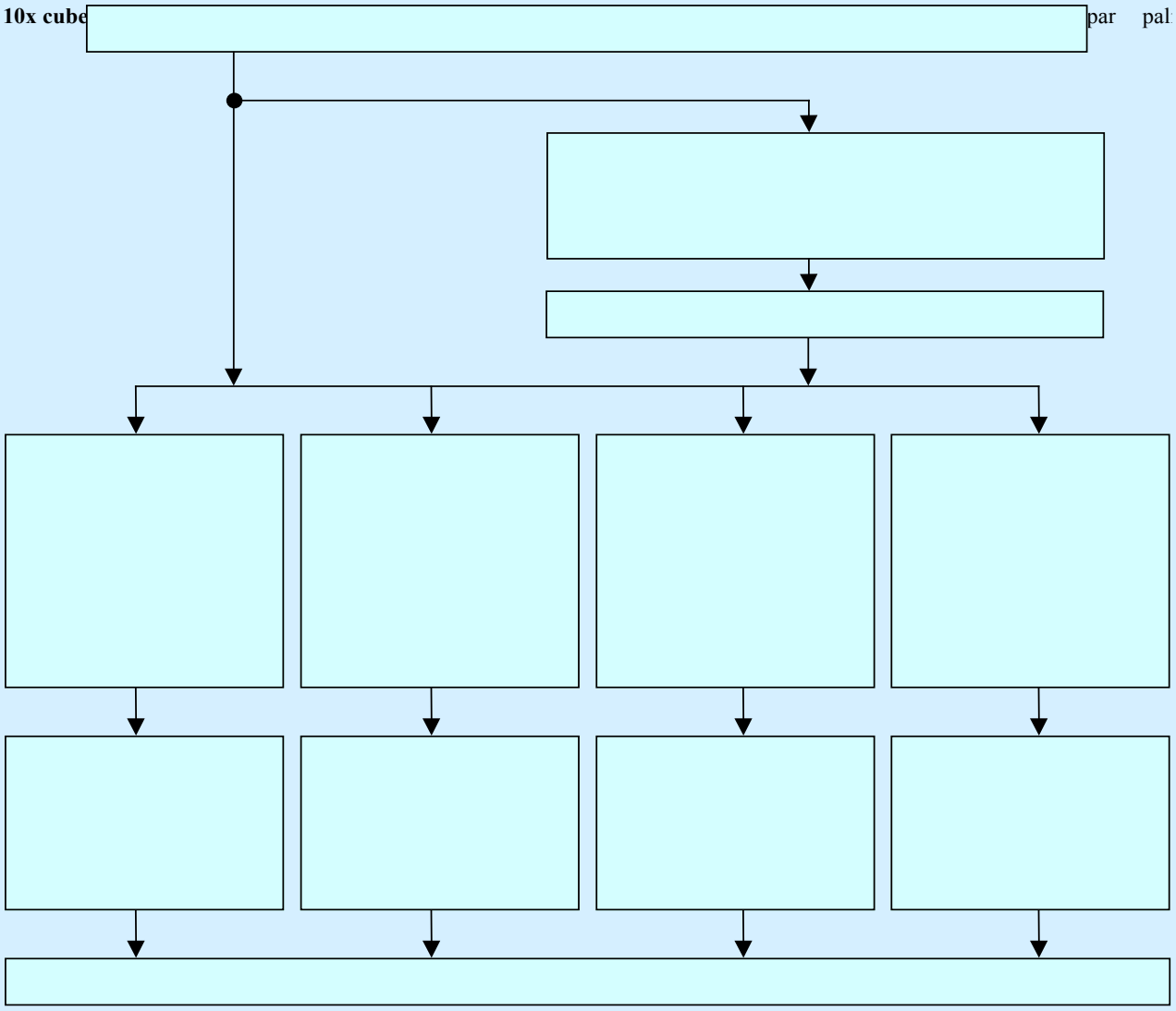
Tests and measurements patterns on CESAR Module

- 64Mb DRAM EDO memory :DC parameters (Icc1 to Icc6), Vol&Voh, Iil&Iih, Iol&Ioh) & Functional at Vcc min.
- Sensors corrosion monitoring (PMOS4) – Triple tracks (resistance and leakage between tracks) – Top & bottom of the module
- Contact continuity measurement (4 points method) between film copper conductors (flying leads) and cube plating
- Capacitors values – Tantalum TAJ-A and B: 2.2 and 10µF

  Ceramic 1210 and 0805: 10nF, 22nF and 100nF
- Resistors values – Chips 0505 and 1206
- Power dissipation with 2 heaters of the PMOS4 chip and temperature measurements with 3 diodes of the die (V_F and I_R)
- Impact on temperature measurements of an AlN heatsink glued below the heaters
- Thermo-mechanical effect measurements with Strain gauges (ACM)
- Daisy chain (200 wires – Au 25µm) resistance



2.3 Evaluation test Plan



Tests and measurements results - Highlights

- Track Resistance on PMOS4: Maximum variation of resistance less than 4% andleakage current between tracks : Less than 1nA at +12V/-12V
- Contact continuity between flying leads and plating: Successfull
- 64Mb DRAM EDO: Functional at Vcc min at all steps – DC Parameters within the specifications – One Memory failed before the 100 TC step→ Failure analysis
- Capacitors values : Less than 2nF variation for a serie of 2 ceramics 100nF and 2 Tantalum of 2.2 and 10µF respectively. 10% variation for a serie of 4 ceramic capacitors of 10nF (x2) and 22nF (x2)
- Resistances values: Less than 1% variation
- Heater resistance on PMOS4: Maximum variation within 1%
- Diodes V_F and I_R on PMOS4 : Maximum drift of 2% and 1,8nA respectively
- Strain gauges X and Y: No change of resistance values at the exception of one module (#36) subject to a 500_ increase → Failure analysis
- Daisy chain resistance (200 wires): Less than 5% variation

Evaluation Phase – Failure Analysis

- Failure analysis performed by LCIE / CNES (Toulouse – France)
- 2 parts under FA (FM n°4 and FM n°36)
- FM n°4: Functional Failure on one DRAM
  * Failure is localized at the RAS input pin (Very low impedance measured).
  * Cause of failure: Electrical Overstress applied to the protection diode of the RAS pad (external cause).
- FM n°36: Increase of resistance (500_) value of a strain gauge
  * Cause of failure: bad adhesion of one metal pad which creates a discontinuity in the gauge pattern. The pad has disappeared after chemical etch.

Evaluation Phase – General Conclusions (1/2)

- The evaluation testing did not produce any catastrophic failures of the 3D stacking interconnection technology
- The measurements performed on the CESAR at high and Low temperatures (+125°C and –55°C) gave correct results
- It is noted that the 10 modules submitted to a preconditionning test of Thermal Vacuum under standard satellite testing conditions:
  * Did not show any failures
  * Did not behave differently from the 10 other modules without any preconditionning
- All the 64Mb DRAMs (80 memories) passed all tests except one (see FA on FM n°4)
- The passive chips incorporated into the modules did not show large parameters variations or catastrophic failures.

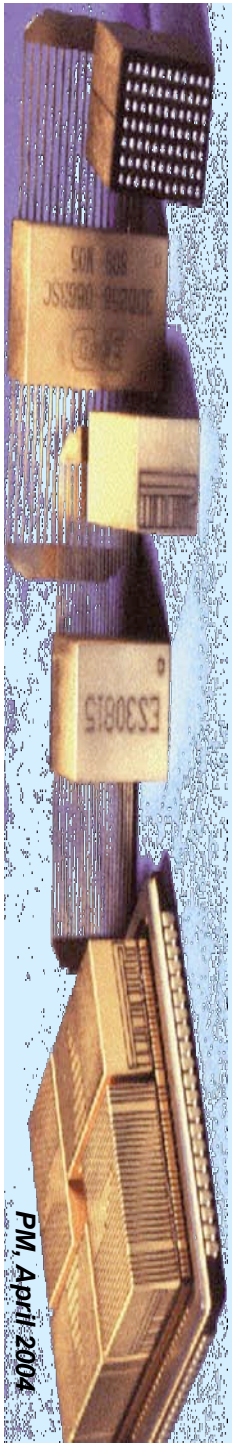
Evaluation Phase – General Conclusions (2/2)

- The parameters of the PMOS4 bare chip did not show large variation during tests. In particular, the corrosion sensors of the chip did not show any degradation after 1000hrs THB. The heater resistance values remain stable. The diode Vf and Ir measurements showed very little variations.

- The continuity measurement of the contacts of the film copper conductors (flying leads) and the cube external metallisation confirmed a stable behavior of this technology whatever the environmental stress applied

- The measurement of the X and Y values of the resistance of the strain gauges did not show permanent stresses in the cube after environmental tests.

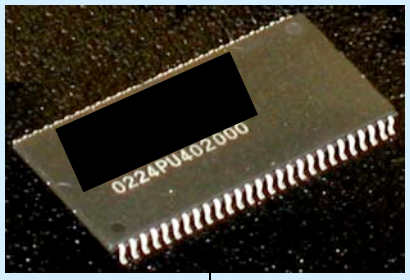
- The 200 Wires bonded on the flex and interconnected in a daisy chain did pass all environmental tests. Total resistance changed less than 5%



3 Capability approval phase
3.1 Three Test Vehicles were used

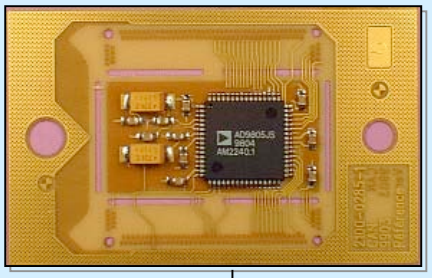
TV1 – TSOP stacking
Flow 1

Memory Modules



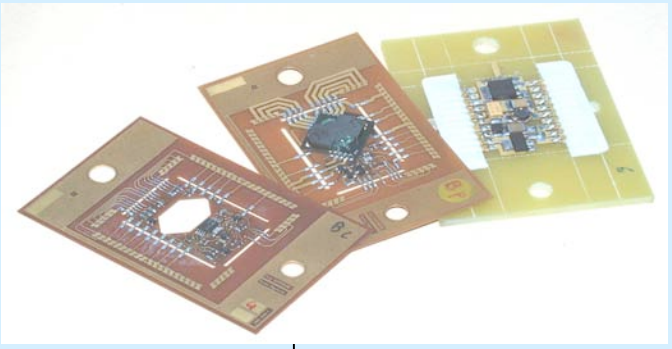
TV2 – Flex stacking
Flow 2

System In Package (S.I.P.)



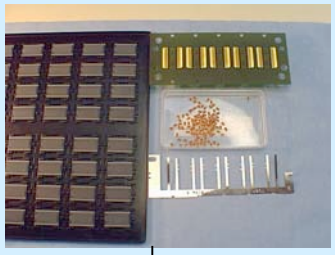
TV3 – Flex/leadframe
stacking Flow 2

Power module
(4W DC/DC Converter)



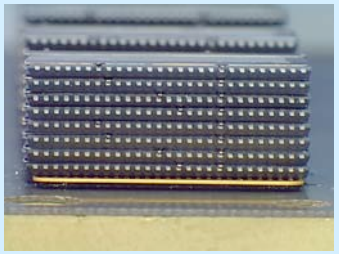
3D Module Assembly – Test and
screening

TSOP Stacking process – Flow 1

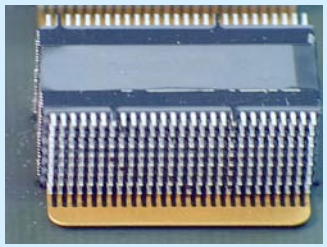


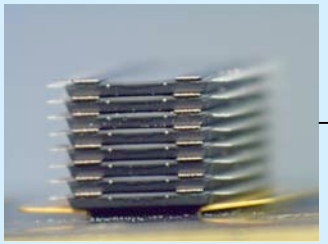
Memory TSOP

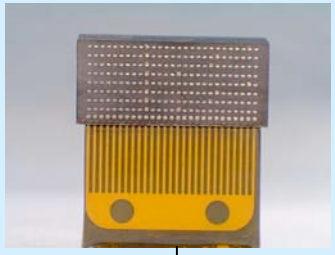
Straps

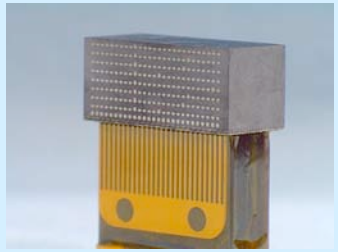


TSOP's and straps Stacking on n levels

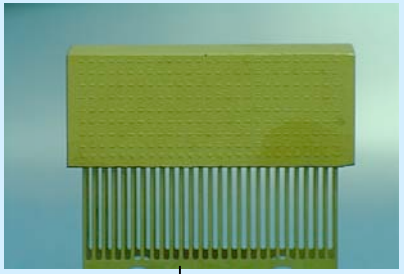




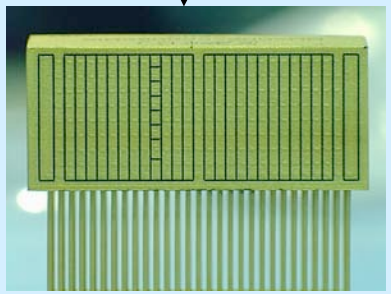




After moulding and sawing, the connections are exposed



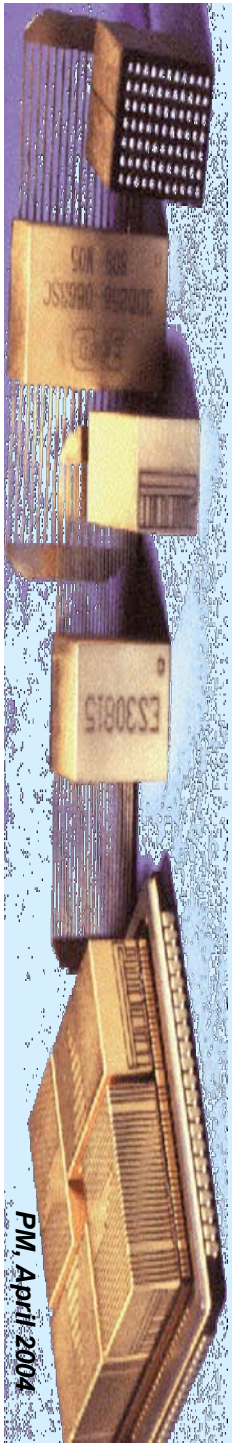
Plating Ni+Ni+Au



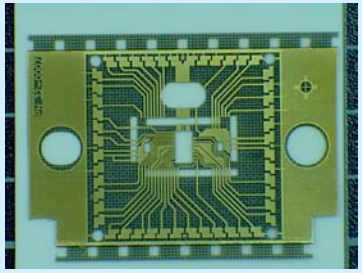
Laser engraving

Electrical Testing and Screening

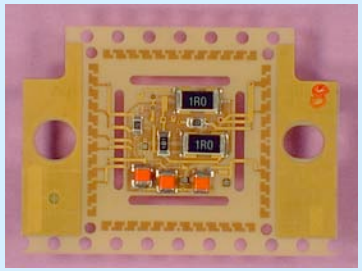
PIM, April 2004



Flex Stacking process – Flow 2

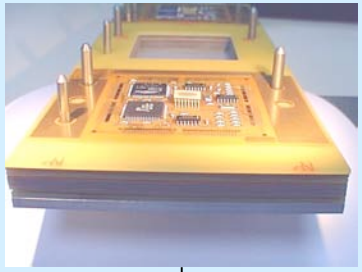


Flex Design:
- design
- procurement

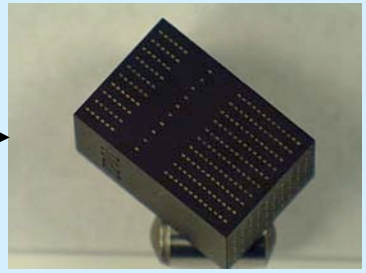


Components Assembly

Flex Testing

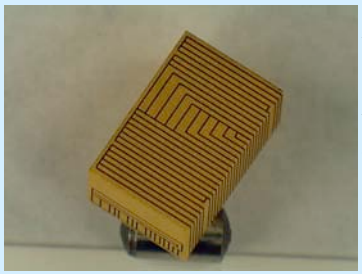


Flex Stacking on n levels



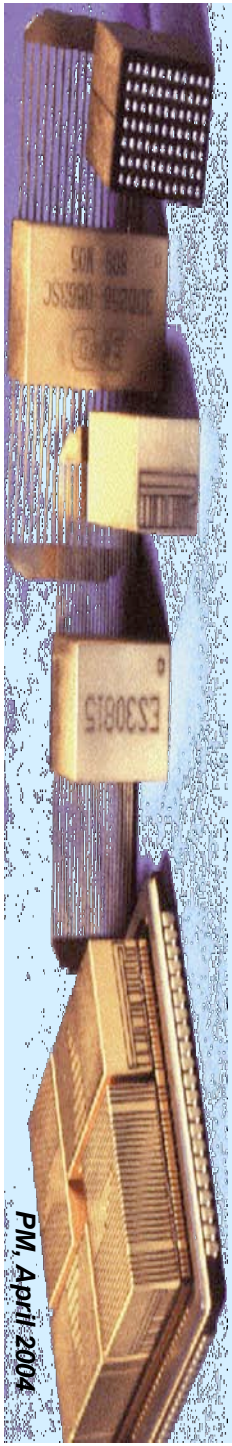
After moulding and sawing the connections are exposed

Plating Ni+Ni+Au



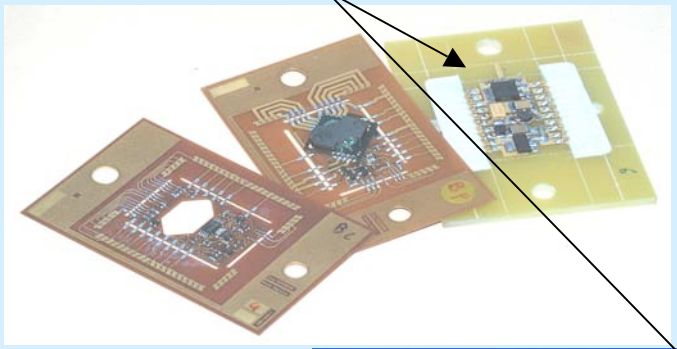
Laser engraving

Electrical Testing and Screening

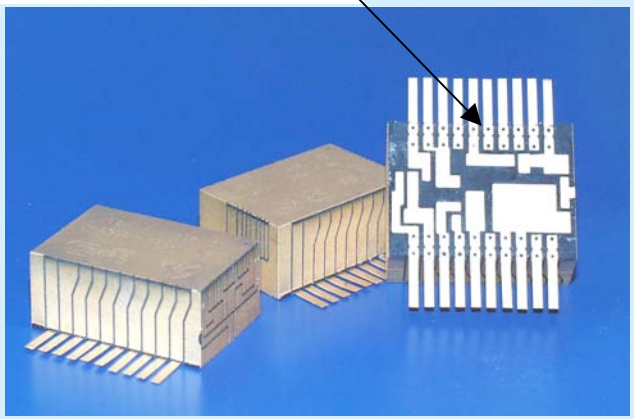


Flex / Leaframe Stacking process – Flow 2 Applied to Power Module

Levels stacked
- *Flex PCBs*
- ***Leadframe with assembled Components***



Plating Ni+Cu(25µm)+Ni+Au



4W DC/DC Converter

application spatiale

In red: Modifications with the standard flow 2 process

3.2 Test Vehicles

TV1 – TSOP stacking Flow 1

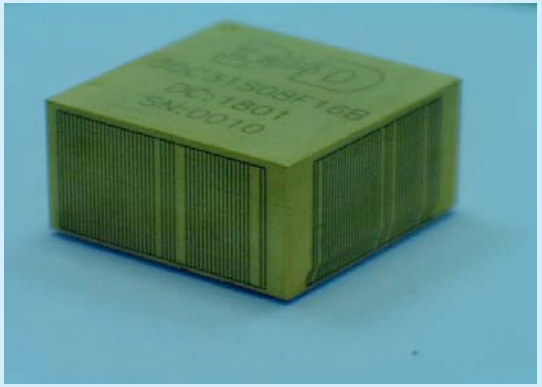
Memory Modules

2Gb SDRAM
SOP Package – 54 leads
Stack of 8 x 256Mb
SDRAM Memories
50Krads Tolerant

Dim.(mm) : 25.6x11.0x11.9
Weight: 7.0gr

TV2 – Flex stacking Flow 2

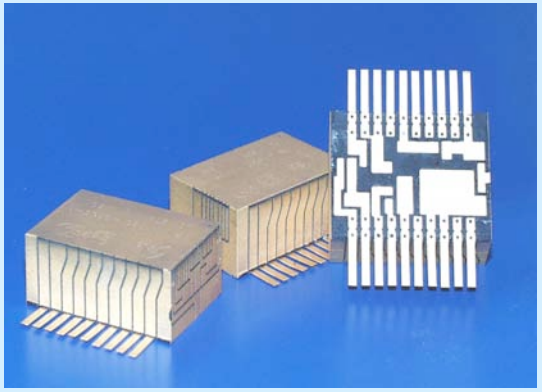
System In Package (S.I.P.)



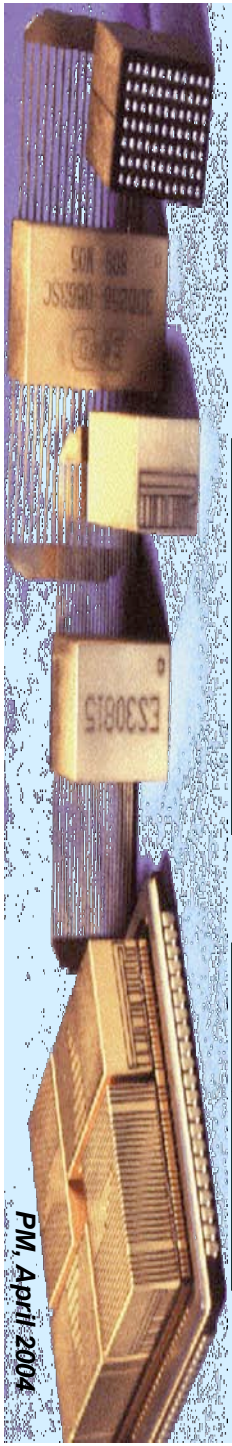
Micro-computer – 4 layers
BGA Package – 204 balls
DSP TMS320C31
EPLD EPM7064S
8Mb SRAM : 16Mb FLASH
40MHz oscillator
Dim.(mm) : 30.0x30.0x15.0
Weight: 26.0gr

TV3 – Flex/leadframe stacking Flow 2

Power module
(DC/DC Converter)



DC/DC Converter 4W
Leadframe package- 20 leads
3 active layers
22 to 37 VDC input voltage
3.3, 5.0,12.0V output voltage
Output regul. 0 to 100% load
Efficiency 70%
Dim.(mm) : 31.0x20.4x11.0
Weight: 21.0gr



3.3 Approval testing Plan (1/3)

Manufacturing and screening of 12TVs per type according to PID

1TV/type kept as reference

File N°1 (3TVs / Type – 2V/1NV)
Environmental tests
Defect allowed (1)

- Thermal cyles –55°C/+125°C
- Moisture Resistance
- Electrical test Tmin, Tamb, Tmax
- Visual inspection
- Final DPA (1TV/type)

File N°2 (1TV / Type – 1NV)
Workmanship tests
Defect allowed (1)

- Workmanship tests
- Marking permanency
- Lead integrity
- Solderability
- Final DPA (1TV/type)

File N°3 (1TV / Type – 1NV)
Construction analysis
ESTEC prestation

TV: Test Vehicle
V: Varnish MAPSIL 213B
NV: Not Varnished

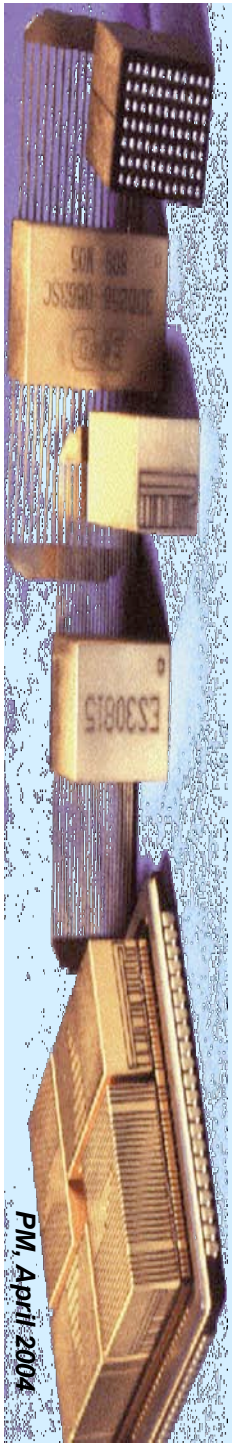
Note: For TV3 (DC/DC Converter), this plan covers both evaluation and approval

File N°4 (3TVs / Type – 1V/2NV)
Endurance tests
Defect allowed (1)

- Dynamic life test 2000hrs +125°C
- Electrical test Tmin, Tamb, Tmax
- Visual inspection
- Final DPA (1TV/type)

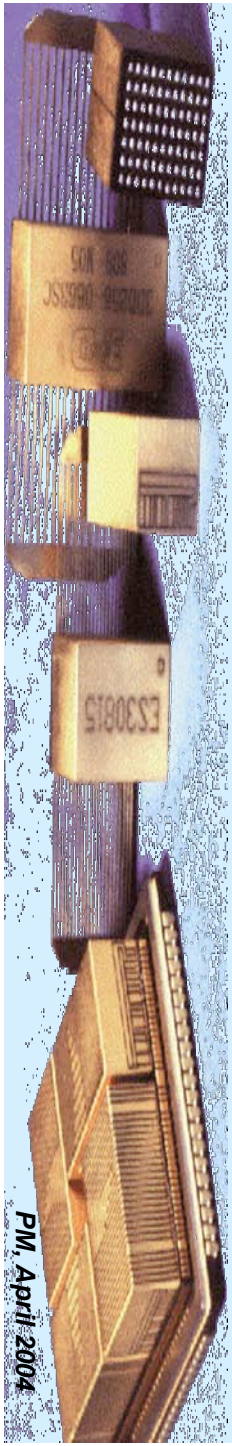
File N°5 (3TVs / Type – 2V/1NV)
Endurance tests under humidity
Defect allowed (1)

- THB test 1000hrs 85%, +85°C
- Electrical test Tmin, Tamb, Tmax
- Visual inspection
- Final DPA (1TV/type)



Approval testing Plan (2/3)

Test	Method	Conditions
Electrical Test Tmin, Tamb, Tmax	According to detal specifications for each TVs *TV1; 3DPA0450-2 (Functional, DC & AC parameters) *TV2: 3DPA0470-2 (Functional, DC et AC parameters) * TV3: 3DPA0760-1(Functional, DC parameters)	
Workmanship Test •Radiography •Ext. visual inspection •Dimensions measur.	 2012 2009	According to Design files for each TVs
Temperature & Humidity under Bias (THB)	*1000hrs +85°C & 85°C under bias •Electrical test at T0 (Tmin, Tamb, Tmax) , T0+240hrs & T0+500hrs (Tamb.), T0+1000hrs (Tmin, Tamb, Tmax) * Drift calculation at Tamb	
Life test	1005	* Life test Bias and patterns According to Detail spec. for each TVs * Electrical test at T0 (Tmin, Tamb, Tmax) , T0+168hrs, T0+500hrs & T0+1000hrs (Tamb.), T0+2000hrs (Tmin, Tamb, Tmax) * Drift calculation at Tamb
Thermal cycles	-55°C/+125°C Dwell time = 15mn ramp=10°C/mn	* TV1 & TV2: 50 cycles * TV3: 500 cycles * Electrical test at Tamb after thermal cycles
Moisture resistance	1004	* Lead integrity is the initial condition of this test



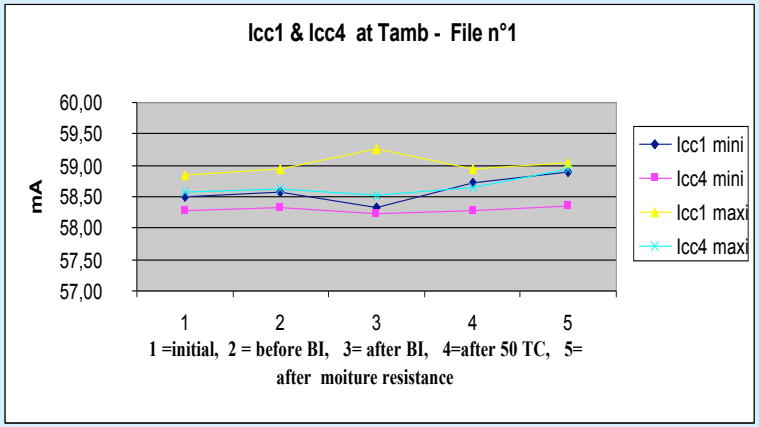
Approval testing Plan (3/3)

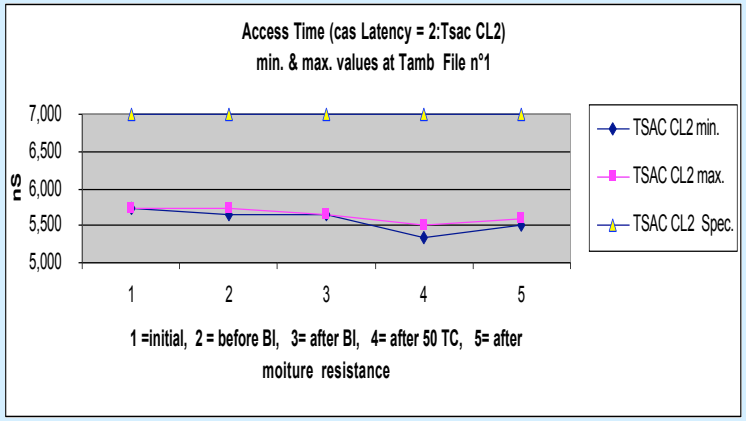
Test	Method	Conditions
Lead integrity	2004	Condition B1
Solderability	2003-7	
Marking permanency	2015-11	Condition 2-1a
Final DPA		According to 3D PLUS Procedure 3DPF2290
Visual Inspection		According to 3D PLUS Procedure 3300-0776

3.5 Approval tests results -TV1 (1/2)

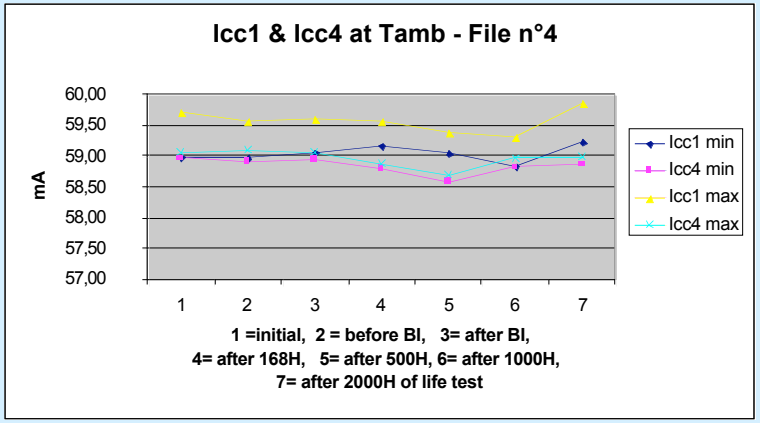
TV1- 2Gb SDRAM : All the tests were successful – The 3D Packaging does not degrade the electrical performance of the memory. MAPSIL coating passed the qualification tests.

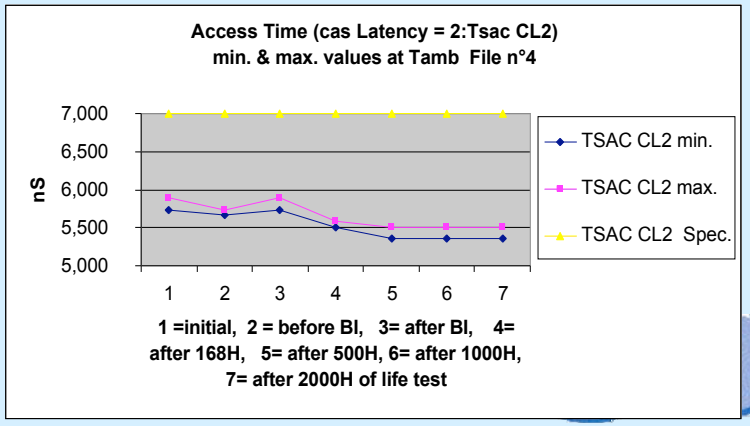
File N°1 – Environmental Tests (50 TC + Moisture resistance)





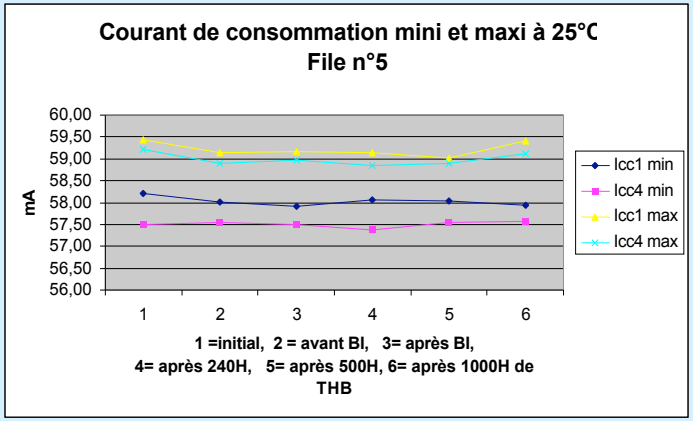
File N°4 – Endurance Tests (2000hrs Life Test)

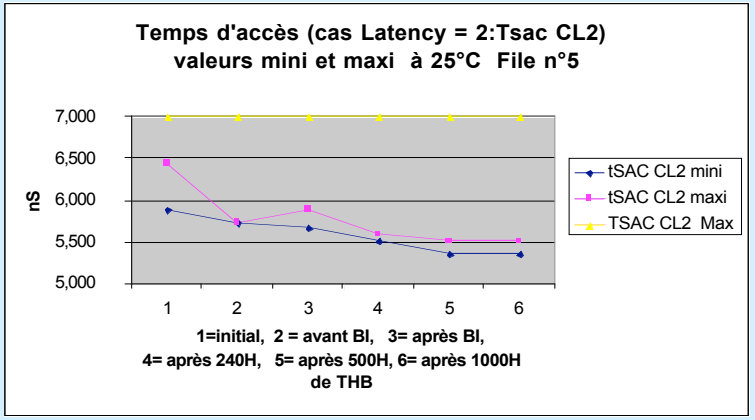




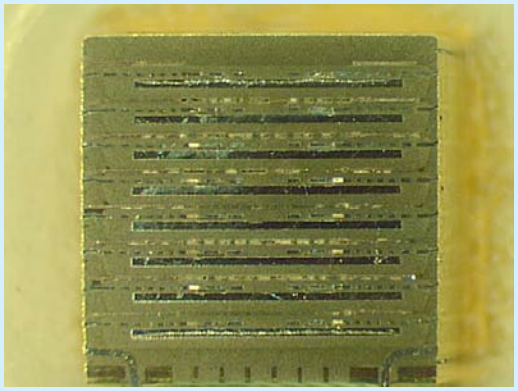
Approval tests results -TV1 (2/2)

File N°5 – Endurance Tests under Huminidty (1000hrs THB 85%, +85°C)

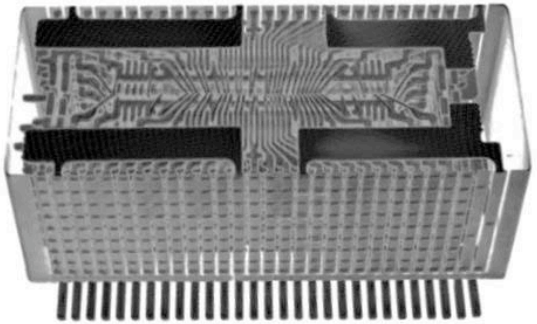




File N°4 - Final DPA – Cross section



File N°3 – Radiographic view



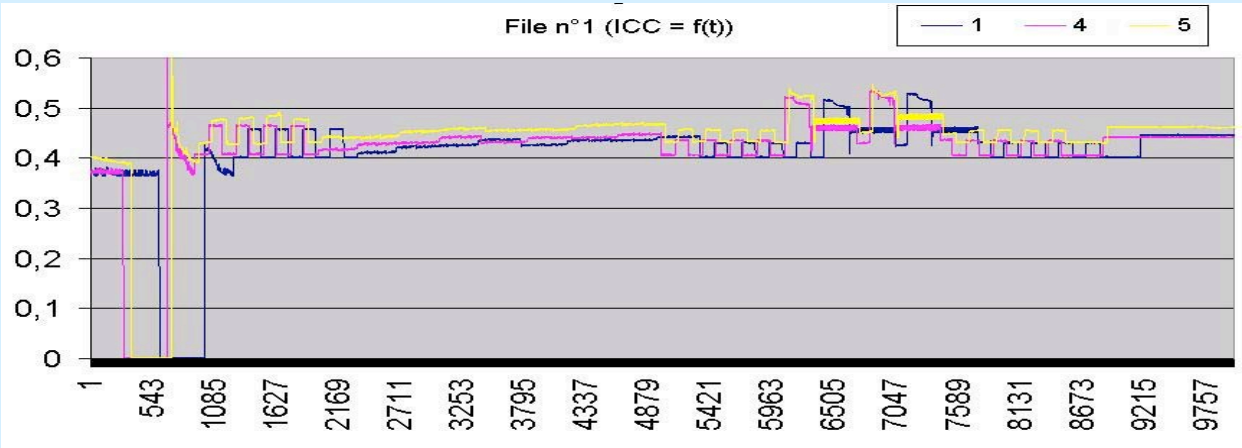
Approval test results –TV2 (1/2)

TV2- Micro-computer : All the tests were successful

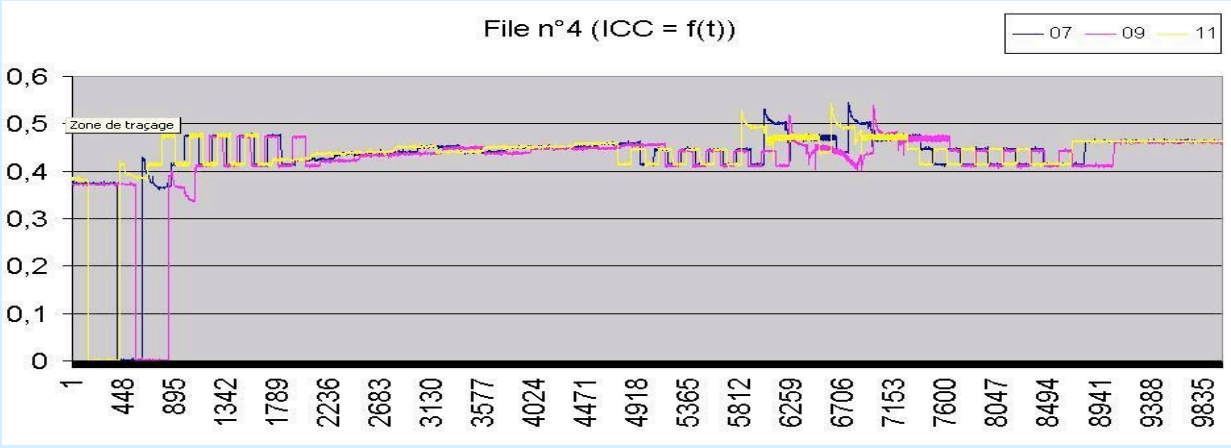
Functional tests are perfomed with auto-test embedded software

File N°1 – Environmental Tests (50 TC + Moisture resistance)

For the graphs : Final results at Tamb. X = V(Shunt) in Volts with Rshunt = 2.2 Ohms / Y = time (scale = 1 sample / ms)

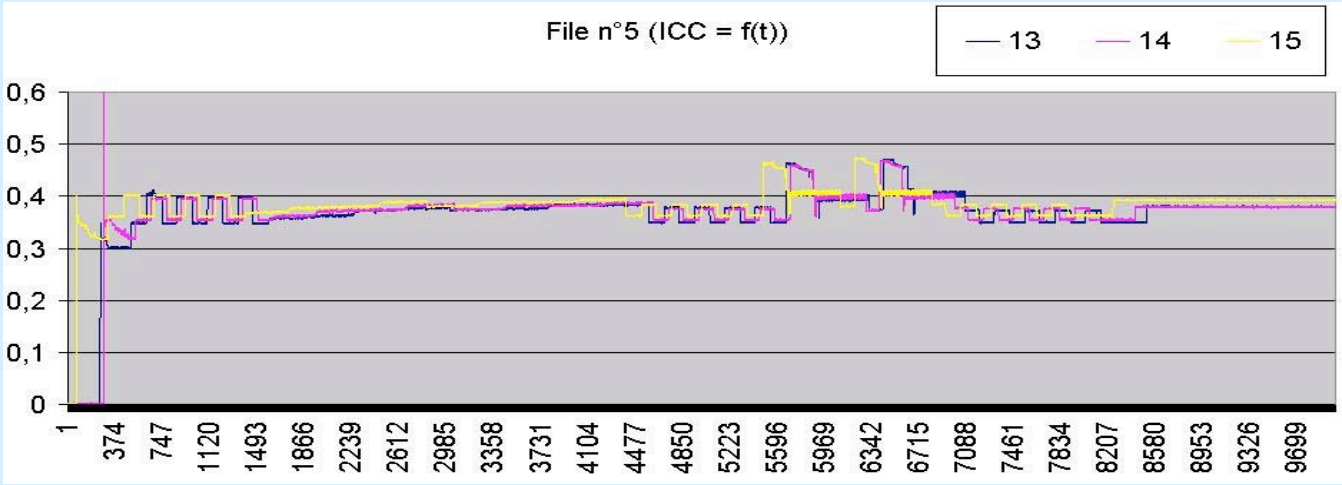


File N°4 – Endurance Tests (2000hrs Life Test)

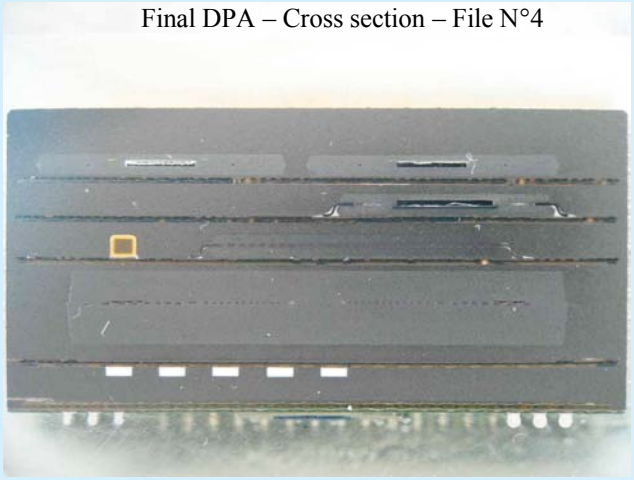


Approval test results –TV2 (2/2)

File N°5 – Endurance Tests under Huminidty (1000hrs THB 85%, +85°C)



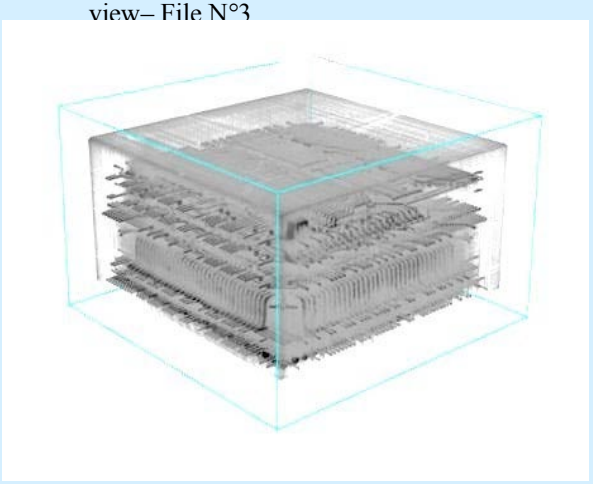
Final DPA – Cross section – File N°4



Flash
SRAM
EPLD

DSP
BGA

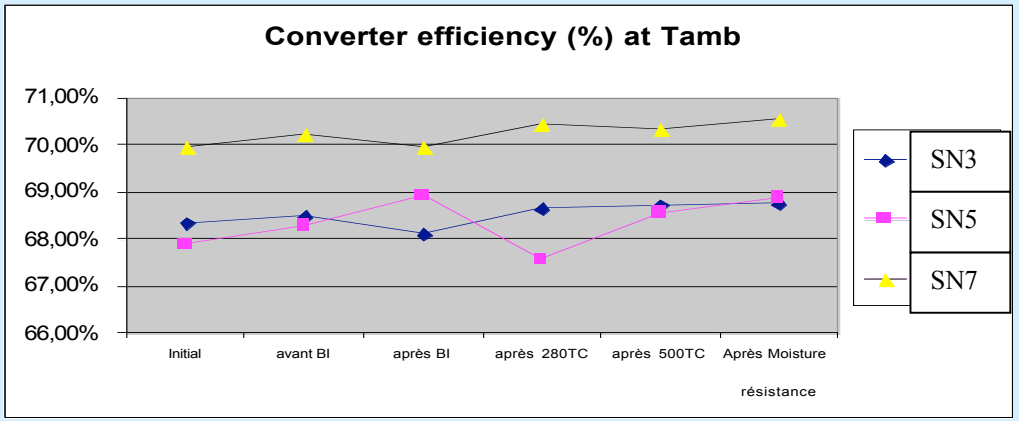
Construction analysis – Radiagraphic view– File N°3



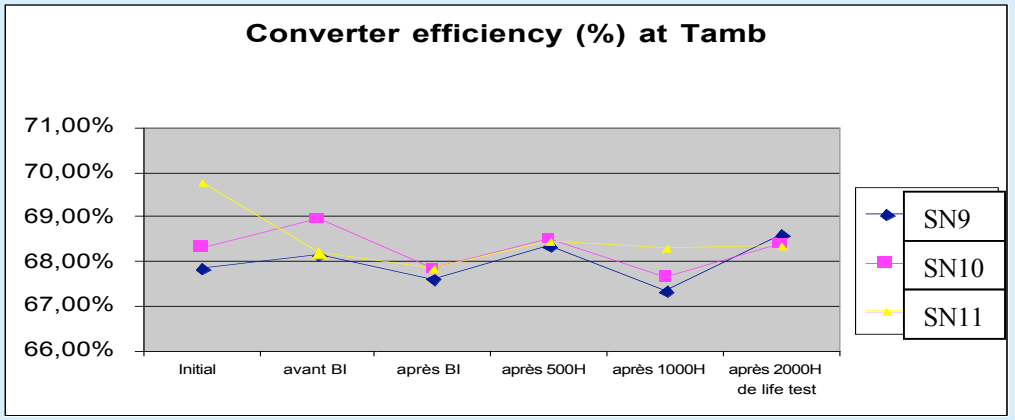
Approval test results–TV3 (1/2)

TV3- DC/DC Converter 4W : All the tests were successful – Converter efficiency is not affected by the different tests.

File N°1 – Environmental Tests (50 TC + Moisture resistance)

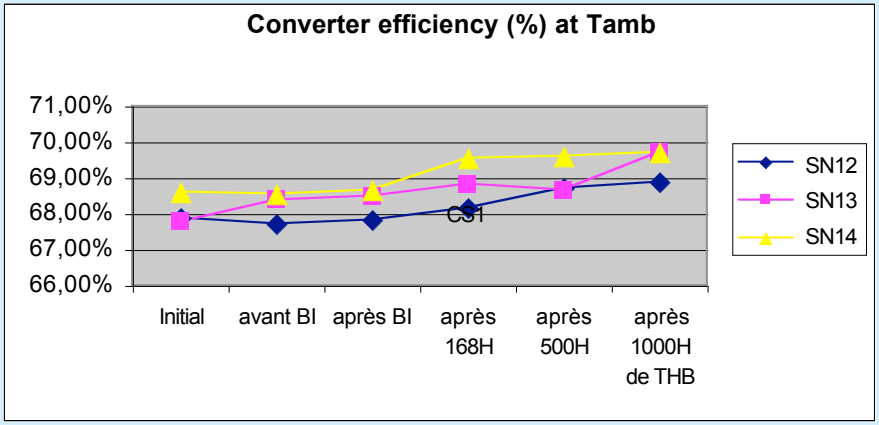


File N°4 – Endurance Tests (2000hrs Life Test)



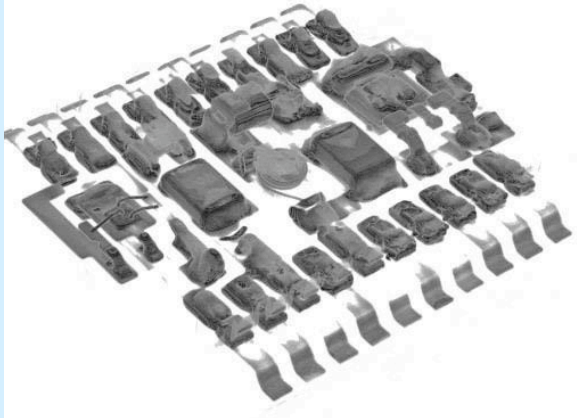
Approval test results–TV3 (2/2)

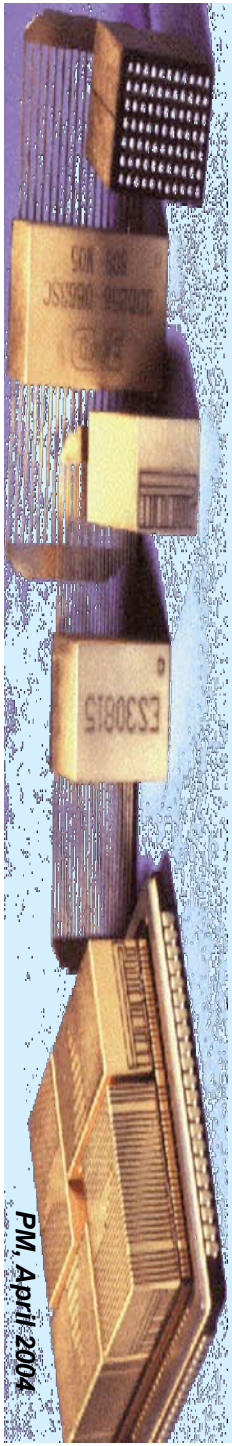
File N°5 – Endurance Tests under Humidity (1000hrs THB 85%, +85°C)



File N°4 - Final DPA – Cross section

File N°3 – Radiographic view – Power level





Approval test results–Conclusions

- 3 Test Vehicles were used in the approval testing plan:
  - TV1: 2Gb SDRAM → Flow 1 (TSOP stacking)
  - TV2: Micro-computer → Flow 2 (Flex stacking)
  - TV3: 4W DC/DC Converter → Flow 2 (Flex / leadframe stacking)

- Approval tests were all successful, including the 500 Thermal Cycles for TV3 (considered as an evaluation test).

- The performances of the modules did not deteriorate nor shift during the various electrical tests performed.

- Mapsil 213B varnishing option was validated

- The technology weaknesses (known by 3D Plus and revealed by ESTEC construction analysis are):
  - Presence of SiC inclusions in the junction lead/surface plating. “Nailheading” effect
  - The external laser grooves are vulnerable to particles. Potential risk of short-circuits between the conductive lines on the surface of the modules

4. Associated Documentation
Process Identification Document (PID)

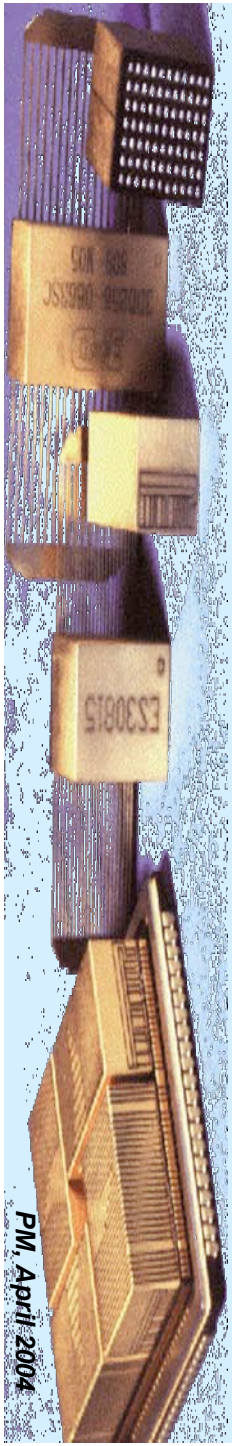
4.1 Flow charts

•Two different manufacturing Flow charts corresponding to 2 different types of stacked layers:

- •Flow 1: TSOPs stacking Process → Memories in TSOP package
- •Flow 2: Flex Stacking Process → Systems in Package

•For these two different manufacturing flows the selection, screening and lot acceptance for both EEE components and modules follow the same methodology:

- •EEE Components Lot Acceptance Tests
- •3D Modules Manufacturing and screening
- •3D Modules Lot Acceptance Tests (including DPA)



4.2 Approved Domain – Main limitations (1/2)

Packaging

- Flow 1 & Flow 2
- Max dimensions: X,Y: 31mm – Z:16.2mm
- Nbr of layers: 10 + lead out
- Space between layers: 0.8mm min. and 5.5mm max.
- Nbr of I/Os: 204 max
- Lead out pitch: 0.5mm min.
- Lead out type: SOP (58 leads) , QFP (114 leads) , BGA (204 Balls) , Power leadframe (20 leads)
- Optionnal MAPSIL 213B Varnishing of module

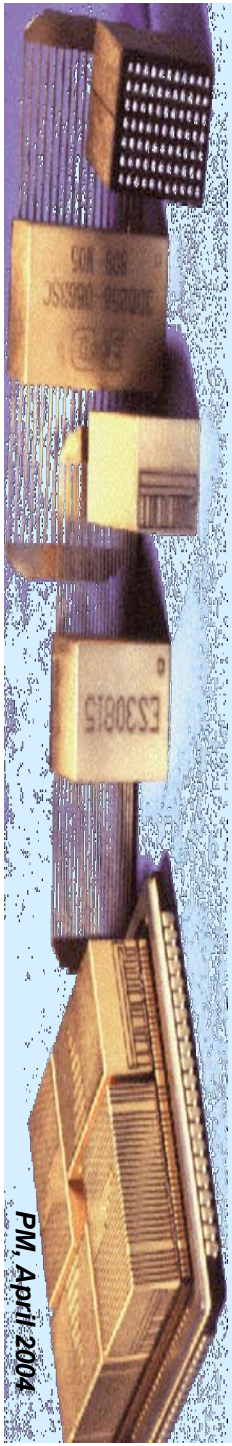
Approved Domain – Main limitations (2/2)

EEE Components

- Resistors 0402 to 1206
- Ceramic capacitors 0402 to 1206
- Tantalum capacitors TAJA to TAJC
- Self : SMD Devices – values 4,7µH to 10µH
- Magnetics: Planar (10 layers)
- PEM: TSOPII-32, TSOPII-54, PQFP132, TQFP100, SO-8, SOT-23, …
- Bare die (Evaluation only – not covered by approval program)

EEE components assembly technologies

- Flow 2: Hand soldering Sn(62)Pb(36)Ag(2) of active and passive components
- Flow 1: TSOPs gluing with Epoxy



4.3 Documentation

Process Documentation

PID: 3300-0546-3

Modules Quality Levels (3DPA0850)

Incoming inspection Methodology (3DPE1160)

Procurement & Inc. Inspection Specification:

- EEE Components (3DPA0350)
- Printed Circuit Boards (3DPA0460)
- Epoxy resin & Glue (3DPA0040)
- Mechanical parts (3DPA0050)
- Plating - subcontracted step (3DPA0090)
- MAPSIL 213B (3DPA1170)
- Solder alloy (3DPA1200)
- Solder balls assembly (BGA) on module – subcontracted step (3DPA1160)

Design Procedures (3DPIxxx)

Manufacturing Procedures (3DPFxxx)

Test & Control Procedures (3DPCxxx)

QA Procedures (3DPQxxx)

Product Documentation

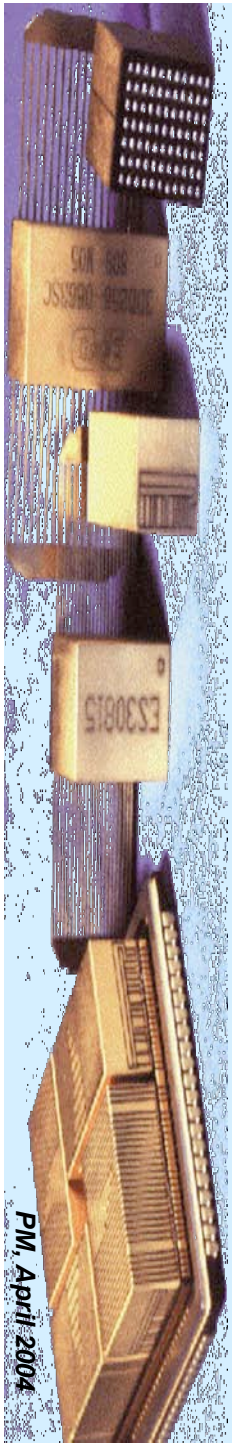
Detail Specification (3DPAxxxx)

Design File (3300-xxxx)

End Item Data Package (3300-xxxx)

LAT report (3300-xxxx) – components & modules

Technical analysis (thermal, reliability, radiations, …) (3300-xxxx)



4.4 Development Methodology (Flow 2 / Custom case)

In Red: Customer input
In Green : 3D PLUS Output
In Blue: Manufacturing steps

Customer Schematic Diagram, part list and design recommendations

Flex Design

Module Design

Detail Specification (send to customer for approval) / Design File → PDR

Flex electrical Test patterns

Electrical Test tools & method

Module Prototyping (Qty=5)

Covered by PID

Yes

Circuit Type Approval (x4pcs)
•Life Test 1000hrs
•DPA (1pc)

No

New subtechniques evaluation & Product validation

Prototypes characterization & Shipping with CTA/Eval/Valid. data → detail specification revision and CDR

Module Manufacturing

4.5 Modules Quality Levels

3 quality levels are defined in 3D PLUS PID and described in the document 3DPA0850 :

CCommercial => Breadboard & Prototypes

IIndustrial => Engineering Models for Space applications

SSpace=> Flight Models for Space applications

4.6 EEE Components Selection flow

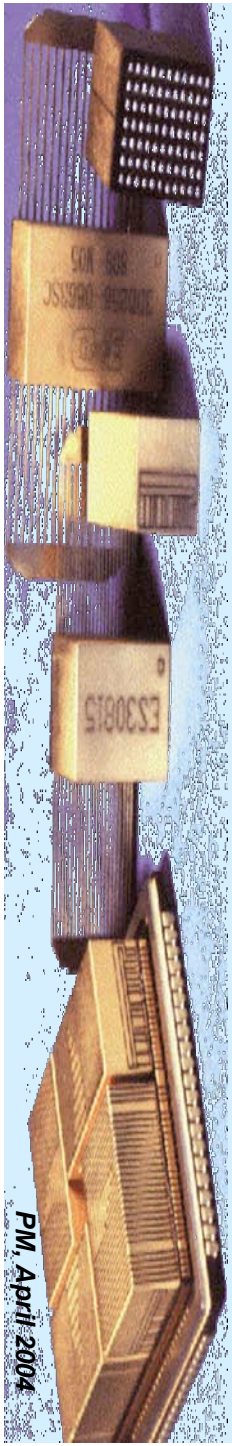
Incoming and Selection tests are described in 3D PLUS Procedure 3DPA0350

For each component lot, the sequence of tests is the following:

- Documentation Review
- Visual Inspection
- Solderability test
- User Lot Acceptance LAT (1000hrs life test, 3 Temp. test, Drift)

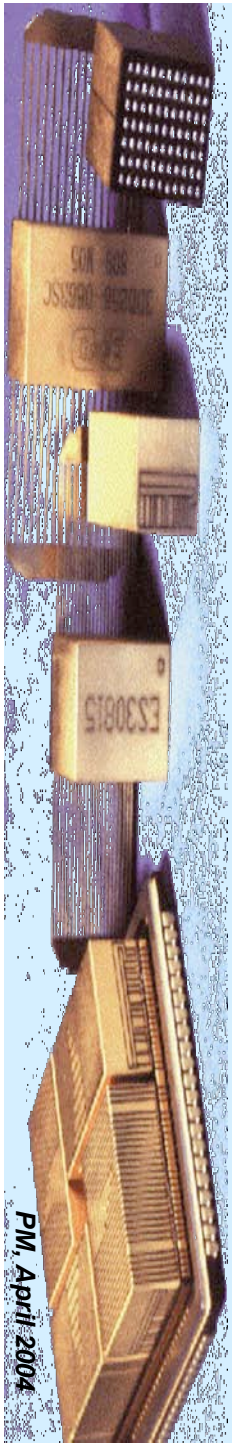
Each test content depends on :

- the module quality level (Commercial, Industrial, Space)
- the EEE component quality level (Commercial, level2, level1)
- the manufacturing flow (Flow 1, Flow 2)
- The type of EEE Component (Passive, Encapsulated Active Devices)



4.7 Module Screening flow

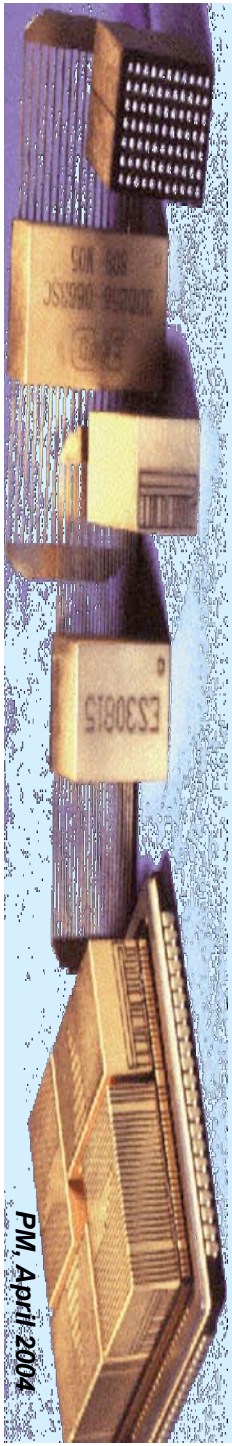
Screening flow	Quality levels		
	Commercial	Industrial	Space
Electrical test at +25°C	X	X	X
Stab. Bake 72 hrs. +125°C		X	X
Thermal cycles (x10) –55°C/+125°C		X	X
Electrical test at +25°C before burn-in with R&R			X
Burn-in 168 hrs. at +125°C		Option 2 (Note 2)	Option 4 (Note 4)
Electrical test 3 Temp. after burn-in		X (GoNoGo)	X (R&R)
Parameters drift calculation at +25°C			X
P.D.A. Calculation			X (Note 6)
Final visual inspection	X	X	X
Dimensional measurement (3 modules)	X	X	X



4.8 Module LAT flow

Module LAT	Quality levels		
	Commercial	Industrial	Space
• Life test 1000hrs. +125°C			X
• Electrical test 3 Temp. after life test with R&R			X
• Parameters drift calculation at +25°C			X
• Final visual inspection			X
• Final DPA (1 module)			X

Module Lot Size	Sampling, First Lot	Sampling, subsequent lots
1 to 25	2	1
26 to 50	3	2
51 to 90	4	3
>90	5	4



Special thanks are extended to the many people who made this evaluation and capability approval possible and specifically:

- **Alberto Boetti – ESTEC**
- **Marc Billot - CNES**