

NPT

(New Packaging Technologies)

INVESTIGATION INTO ADVANCED AND HIGH PIN COUNT CHIP ASSEMBLY TECHNOLOGIES

ESA Contract No: 16479/02/NL/PA

- **PHASE 0** Summary reporting of previous work on Flip Chip technology
- **PHASE 1** Materials and technology selection and procurement
- **PHASE 2** Manufacturing and reliability testing of test samples

1

PHASE 3 - Recommendations for testing methods and inspection techniques

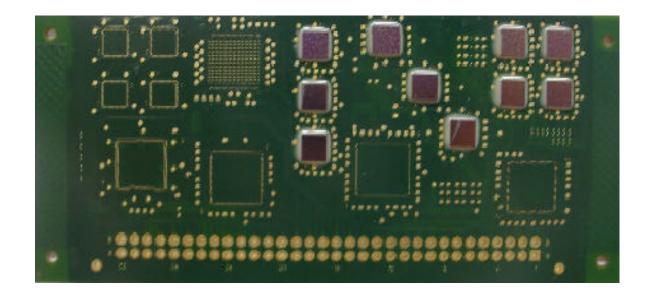




PHASE 0

Summary reporting of previous work on Flip Chip technology

 During Phase 0, All relevant experience, both derived from own previous efforts and other organisation, was collected and a summary report on State of the Art of the Technology was produced.





PHASE 1

Materials and technology selection and procurement

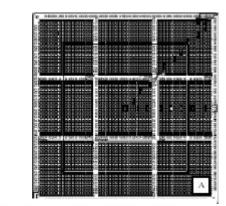
Phase 1 is targeting on material and test set-up selections of the project. All the selections made should be based on the potential suitability for space applications.

• (WP 1) Selection of Flip Chip Test Chips

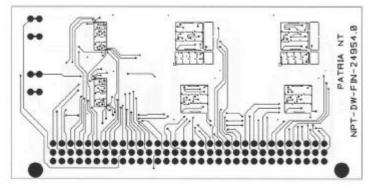
- Three different chip's were selected
 - A -die (8,3x8,3mm, 260 bumps)
 - C -die (2,8x8,3mm, 210 bumps)
 - E -die (12x12mm, 600 bumps)

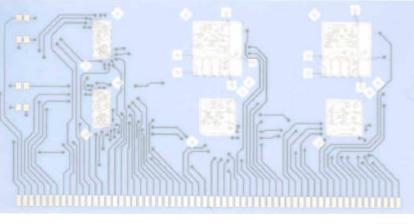
• (WP 2) Selection of Test Substrates

- Two substrate materials was selected
 - Multilayer polyimide PCB
 - Multilayer thick film on Alumina
- (WP 3) Selection of Underfill Materials
 - Two different underfill materials was selected
 - Thermoplastic
 - Thermosetting



Patria







TEST CHIP

• Test chips were planned to serve flip-chip packaging technology and include electrical and thermal test structures for reliability testing

(daisy chain, heaters and a temperature sensing diodes).

• Eutectic tin/lead bumps

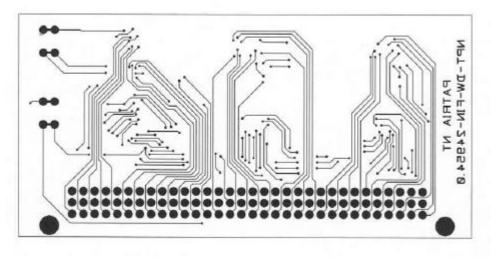
SUBSTRATE

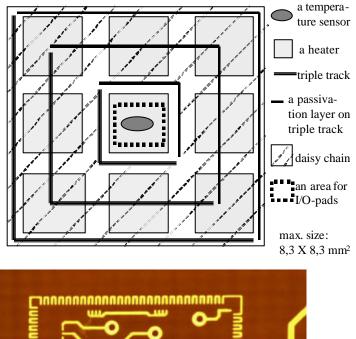
• Test substrate included measuring points for electrical testing and continuous monitoring of Daisy Chain contact resistance during environmental testing.

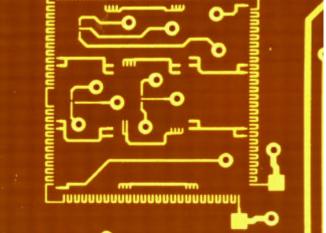
UNDERFILL

4

• Material selections were made with potential suitability for future space applications.









PHASE 2

Manufacturing and reliability testing of test samples

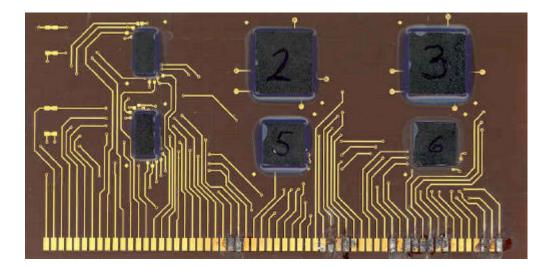
Reliability testing included Thermal cycling and Temperature humidity bias testing (THB).

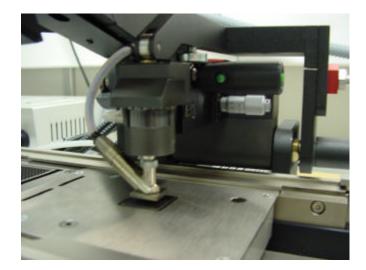




ASSEMBLY PROCESS

- Flux dipping with Fineplacer
- Alignment with Fineplacer
- Feflow with REF-reflow oven
- Underfilling with dispencer
- Underfill curing with oven
- Visual inspection with microscope
- Contact resistance measurement with multimeter.











ENVIRONMENTAL TESTING

Tested with continuos monitoring by data-logger and PC.

Temperature Cycling

7

Thermal cycling test included 1000 cycles, -55 °C to +125°C (MIL-STD-883, Method 1010)

Temperature Humidity Bias Testing

Temperature Humidity Bias test included 85°C/85%/RH, 1000 hours under bias.

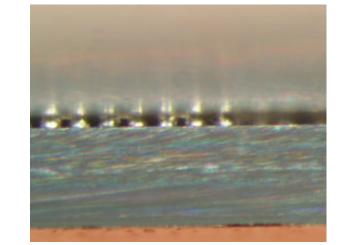




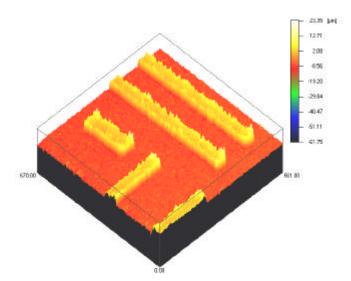


QUALITY ASSESMENT TEST

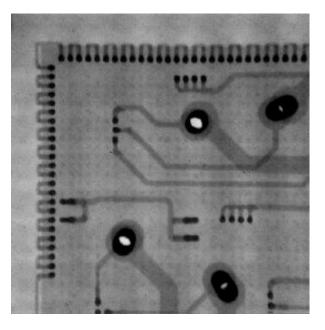
- Samples were submitted to QAT after the assembly and after the Environmental Testing.
- QAT includes:
 - external visual inspection,
 - daisy-chain and contact resistance measurements,
 - radiographic inspection (X-ray, to solder joint integrity),
 - scanning acoustic microscope inspection (SAM, to underfill integrity)



Patria



000	00	00	X	20	R	R	P	R	0	R	R	R	9	Ŕ	õ	9	Ö	Ø	9	2	0	0	Ö,	ğ	0	9	R	2	3
200	00	8	8	0	0	0	ğ	ō	ö	ò	ġ	0	ø	ğ	ò	9	•	•	ģ	8	•	0	0	ò	0	0	¢	0	
500	00	8	9	ю	6	6	8	8	8	8	8	6	8	8	8	8		•	ä		6	6		8	8	8	0	0	
	00	100	8	20			Q				2	9	0				Ω	Ω			2	2		P	2	9		2	
200	22	5	8	22		2	8	R	Я		R	2	Я	Я	Я	Я	Я	Я	Я		R	R	Я	R	я	Ħ		2	
566	88	20		58			a	x	б	ъ	ъ	ъ	в	в	ъ	ы	ы	Ы	в		6	в	ы	F	8		6	ŏ	
200	00	e c	x	50	ō	ō			o	o	o		o	o	o	o			o		0	0	o	b	ð	o	ō	0	
20	0	88	25	28	Q	Q		Q	Q			2	0	2	g	Q	Q	Q	Я		2	2		Q				2	
225	22	86	δ	8	Я	R	2	8	Я	R	R	R	R	R	Я	R	я	g	Я		R	R	R	R	Я	Я	Я	я	
968	88	88	9	93		Н	В	8	Н	Ы	В	В	В	ŏ	а	8	ð	М	s		в	5	н	Ы	В		в	ы	
000	00	88	x	50					o	ö	ō	ö	õ	ō	a	ō	ē	Ö	э	6	Ö,						o	0	
		15	25	20										R	g	ģ	2	Q	9	2	0								
200	88	35	č,	22	Я	Я	8	Я	Я	Я	Я	Я	Я	Я	Я				Я	2	2	2	ю	Я	Я	Я	Я	ы	
		82	9								2								ö	3		۲							
200	00	56	3	20	2	2	q		9	ç	p	0	2	2	я	0	0	٥	۰	2	0	٥	9	0	2	0	0	0	
000	00	00	2	00	0	Ó	0	0	Ó	0	0	C	Ó	Ö	ð	6	ð	6	0		0	6	0	0	Ó	Ó	C	0	
200	00	00	23	20	o	Q	0	0			Q					o				Q	2	0						0	
		25																										52	









RESULTS

THERMAL CYCLING TEST

• All samples with Thermosetting underfill passed test with no failures

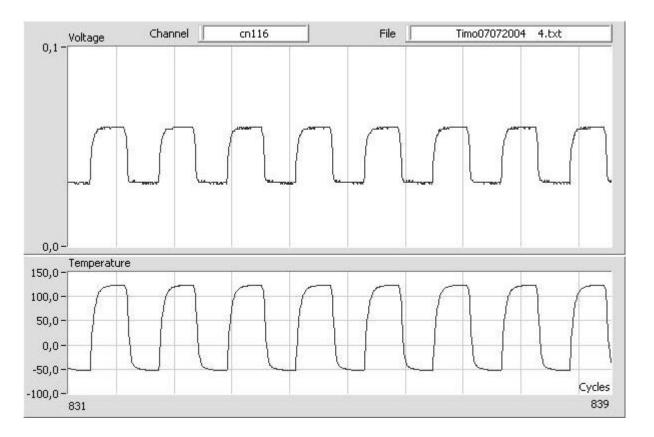
• All samples without underfill and with Thermoplastic underfill failed in the test.

THB TEST

• All samples with Thermosetting underfill passed test with no failures

• All samples without underfill were still electrically connected after test, but the value of contact resistance was >10 times higher than before test.

• Some of the samples with Thermoplastic underfill failed the test





RESULT SUMMARY

10



- All samples with Thermosetting underfill passed test with no failures
- All samples without underfill and with Thermoplastic underfill failed in the test.

In this project results divided along with underfill material type (thermosetting versus thermoplastic), but conclusion that all thermosetting underfill's are good and all thermoplastic are bad is wrong. There are also good results with thermoplastic and many bad results of thermosetting materials detected in earlier studies with small pitch and high pin count assemblies.

In the assembly process of advanced and high pin count attachments, there are many essential things to handle, to make a successful electrical connection between die and substrate. (alignment accuracy, bump material, self alignment of the die, flux type, amount of flux, right reflow profile for different component size and substrate material, etc.)

After the successful soldering result and electrical connection of the component, only significant matter for reliability of Flip Chip assembly is the selection of the right underfill material





PHASE 3

11

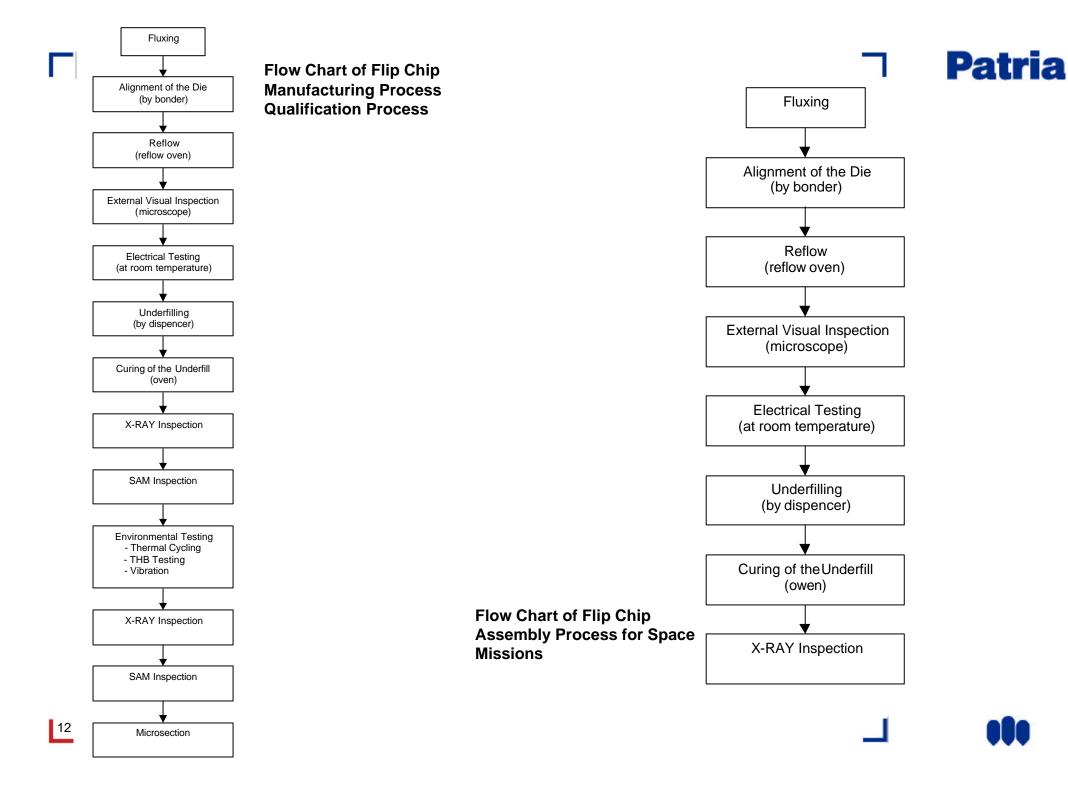
Recommendations for testing methods and inspection techniques

At the end of the Phase 3 a report containing recommendations and draft specifications for the inspection and process verification of Flip Chip technology was delivered.

In spite of the development and all the effort from electronic industry, for the better and more reliable inspection methods for area array joints, there is not one inclusive method available for flip chip testing or inspection.

Combination of the right tests has to be found for process verification and reliability testing, and inspections for the instruments to be used in space missions.

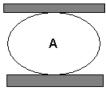
different inspection combinations for the process qualification and unit or module testing during space missions.



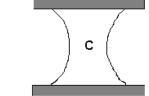
External Visual Inspection for Assembly Process Quality Assessment

Different bump shapes of the area array components.

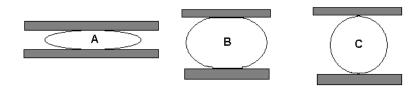
- A) Normal ball shape
- B) Column shape
- C)Lifted ball shape

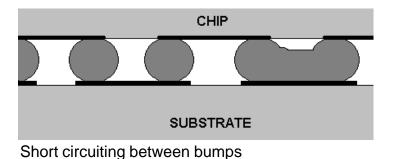


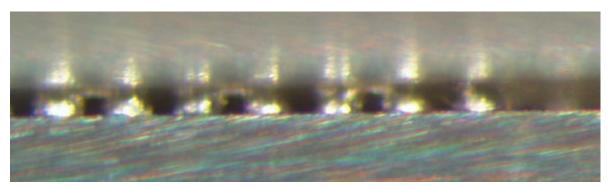




- Bump shape qualification
- A) Too flat / collapsed bump
- B) Good attachment
- C) Gold joint / bad vetting





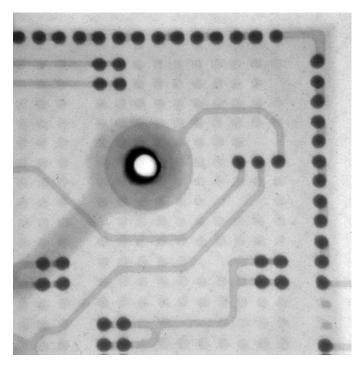


Good connections



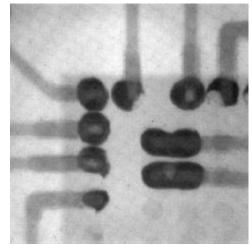


Radiographic Inspection (XRAY) for Quality Control

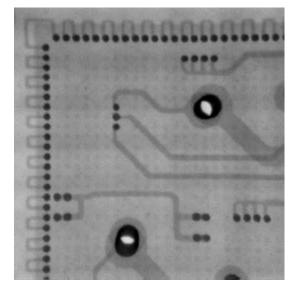


X-ray was the first choice for BGA inspection when area array devices were first introduced, and is commonly used in the industry today.

Missing of the solder ball / shot circuiting between solder joint could be detected quite easily from the pictures, but deep interpretation of the X-ray pictures needs experience of the common mode failure mechanisms of the area array components.



Bad connections



Bad alignment



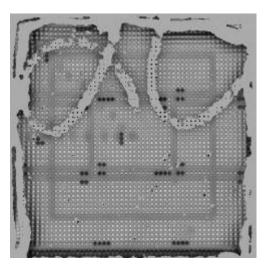
Good connections

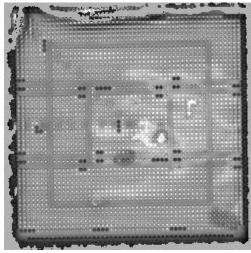


Scanning Acoustic Microscope Inspection (SAM) for Quality Control

000000	
00000	
00000	
00000	
00000	
2 22	
0000	0 000
00000	
00000	
00	

- Purpose of the SAM inspection is to detect the underfill layer between die and substrate.
- Lot of information available if the focus of the right layer could be reached.
- Making conclusion out of the pictures is quite same with SAM than with x-ray pictures: "Everyone can find some of the most obvious failures from the picture, but deep analysis of the SAM –imaging still needs experience of the common failure modes of the area array components."

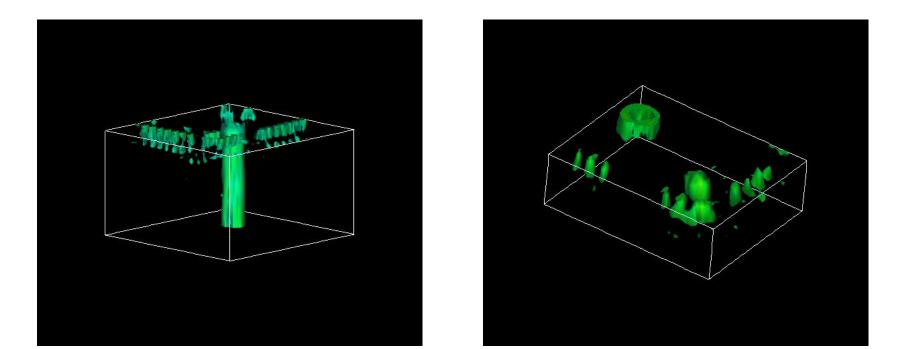








3D - XRAY



? Not Ready for Flip Chip Inspection (more accuracy/resolution needed)



Thank You!

- Alberto Boetti ESA
- University of Technology of Tampere
- TEKES (National Technology Agency of Finland)
- Companies
 - Tellabs
 - Nokia Mobile Phones
 - Elcoteq

17

• Aspocomp

