3D Microwave Module Packaging

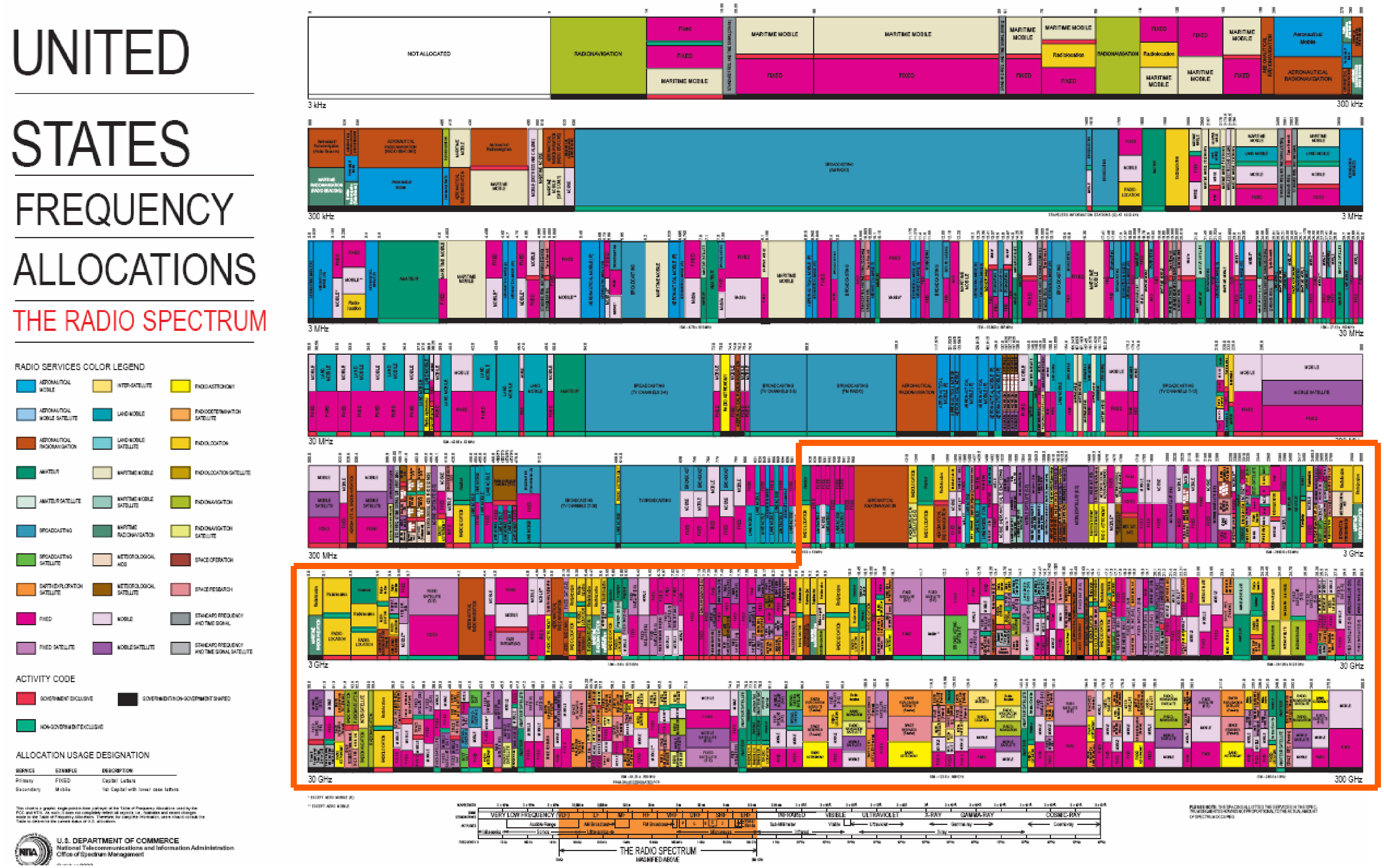
Geert Carchon, PhD
Program Manager Heterogenous RF Systems
IMEC

Outline

- Introduction
  - Why 3D
  - Various 3D flavours
- 3D RF modules using thin-film passives
  - Thin film introduction
  - Via requirements & estimated performance
  - IMEC via approach
  - Preliminary results
- Conclusions

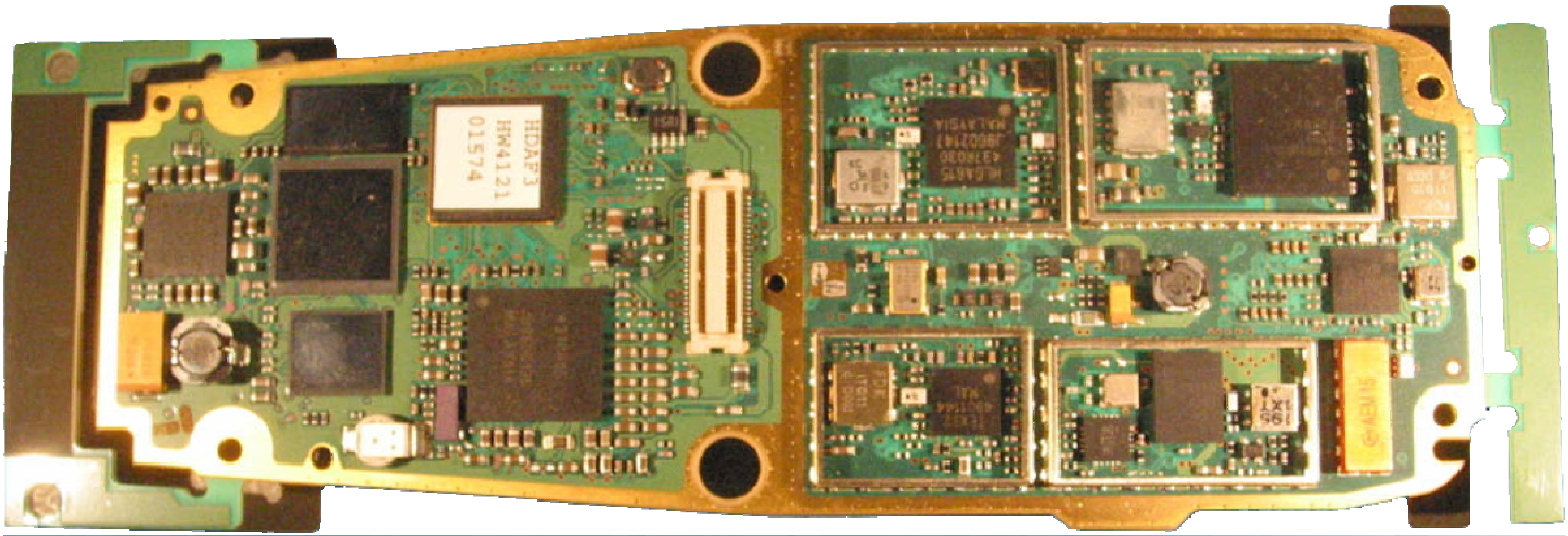
Wireless communications

So many applications …



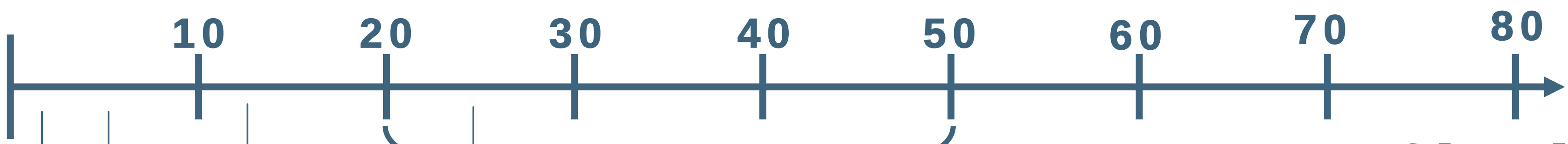
The wireless convergence: more and more wireless standards are required in one terminal

- Smart phone: plenty of discrete devices and multiple radios in these applications (smart phones)
  - Take up large part of limited space in phone
  - Large cost for discrete components and complex board
  - dedicated solutions for each standard take up space, even if they are not used



Wireless communications

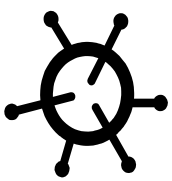
So many applications ...



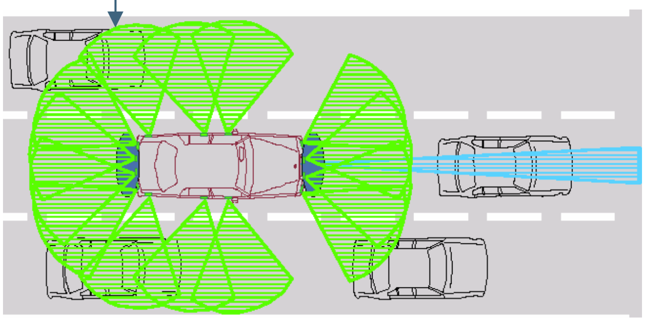
Short Range Radar

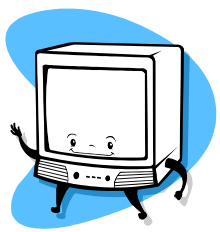
Broadcasting

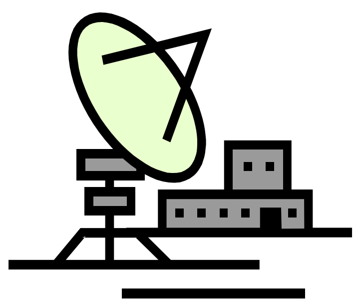
WLAN



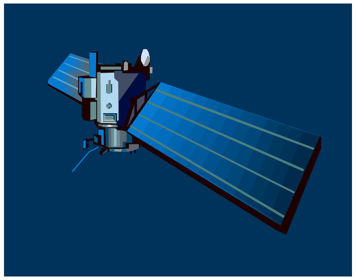
- Radiolocation
- Earth observ. sat.
- Fixed and mobile radio services
- ...







Long Range Radar (ACC)



- Mobile handsets
- Global positioning systems
- Earth observation

Introduction: RF-Packaging Drivers
Miniaturisation of RF Electronic Systems

Enabling Technologies:

– **IC-integration: SOC**

– **High density interconnection and packaging technologies:**

SIP: "System-in-a-package"

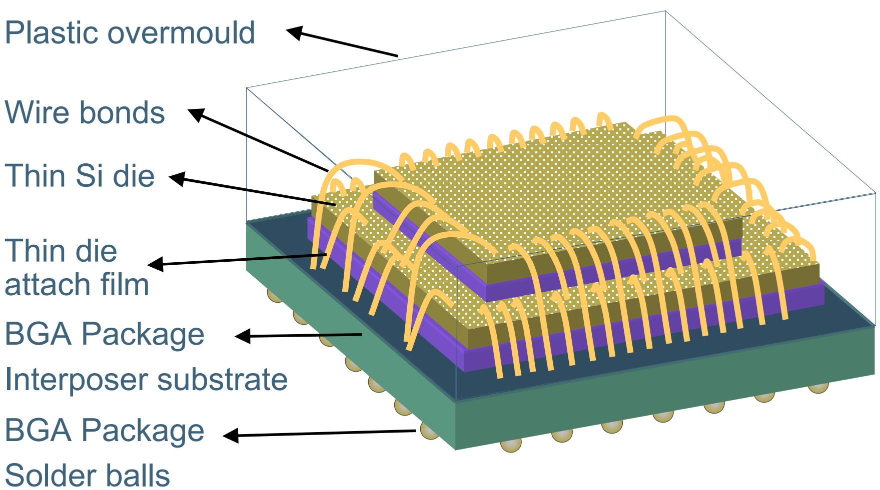
- 3D integration

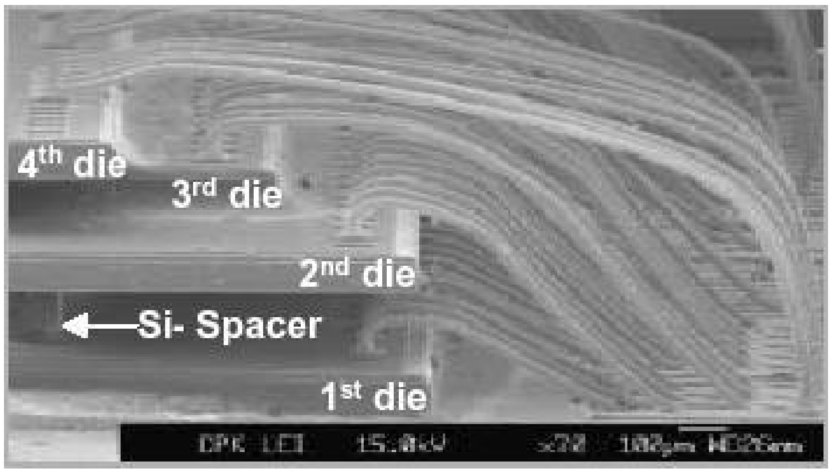
Introduction : Why 3D?

- Drivers for 3D interconnects & packaging :
  - **Size reduction:**
    - **Minimal area / volume of an electronic system**
  - **Solving the "interconnect bottleneck" :**
    - **Long interconnects are too slow**
    - **Long interconnects consume too much power**
  - **Hetero-integration:**
    - **"Seamless" mixing of different microelectronic technologies at the wafer level**

3D packaging technology today

- Stacked-die packages
  - Assembly by wire bonding of stacked die in a single package
- High volume, mainly: portable phone application
  - various types of memory on cell-phone processor chips
- Technology
  - standard wire-bond packaging technology





Source: ChipPac

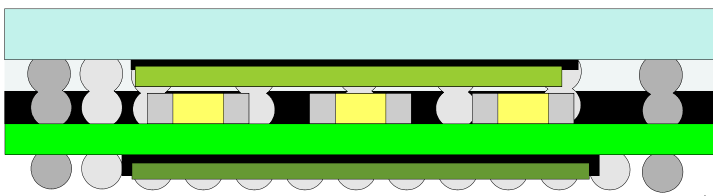
Different 3D-interconnect “flavors”

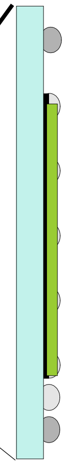
- **3D-SIP: “System-in-Package” Traditional packaging & interconnection technologies**
  - Wire-bonded die stack
  - Stacking of packages: preferably SIP packages
- **3D-WLP: “Wafer-level-packaging” Technology for flip chip bumping, redistribution and CSP**
  - 3D interconnects realized at wafer level
  - 3D interconnects processed *post IC passivation*
- **3D-IC and 3D-SIC: IC-foundry technology**
  - 3D interconnects at local wiring hierarchy *(3D-IC)* or at intermediate or global wiring hierarch *(3D-SIC)*
  - 3D interconnects processed *post Front End and prior to Back End*

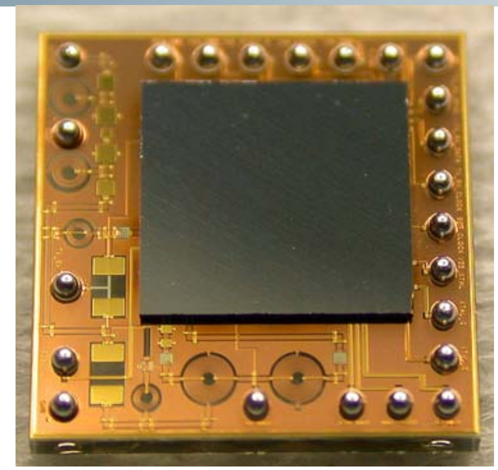
RF-IPD on AF45: 7x7 sqmm Bluetooth Module
Example 3D-SiP stack

RF module "flip-chip" mounted on a digital module

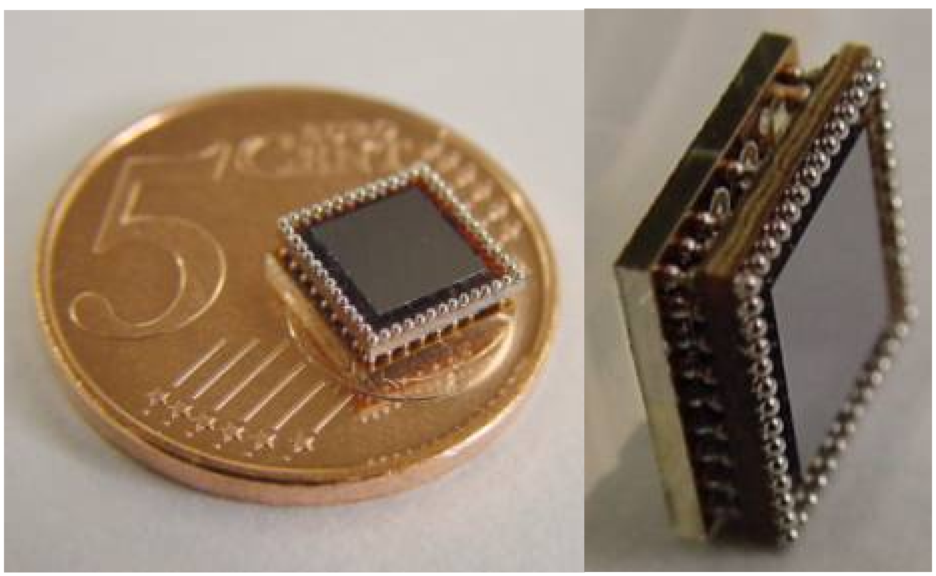
Size : 7x7x2.4mm

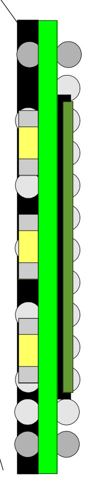


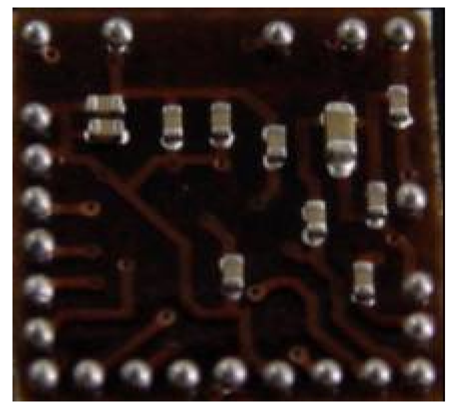




RF chip "flip-chip" mounted on rf-integrated passives substrate

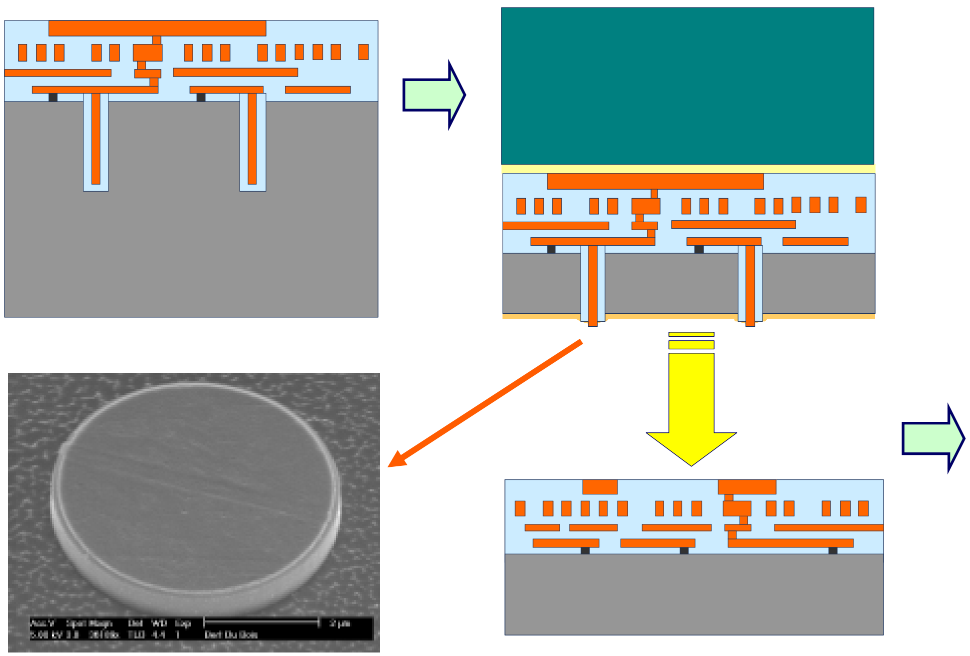


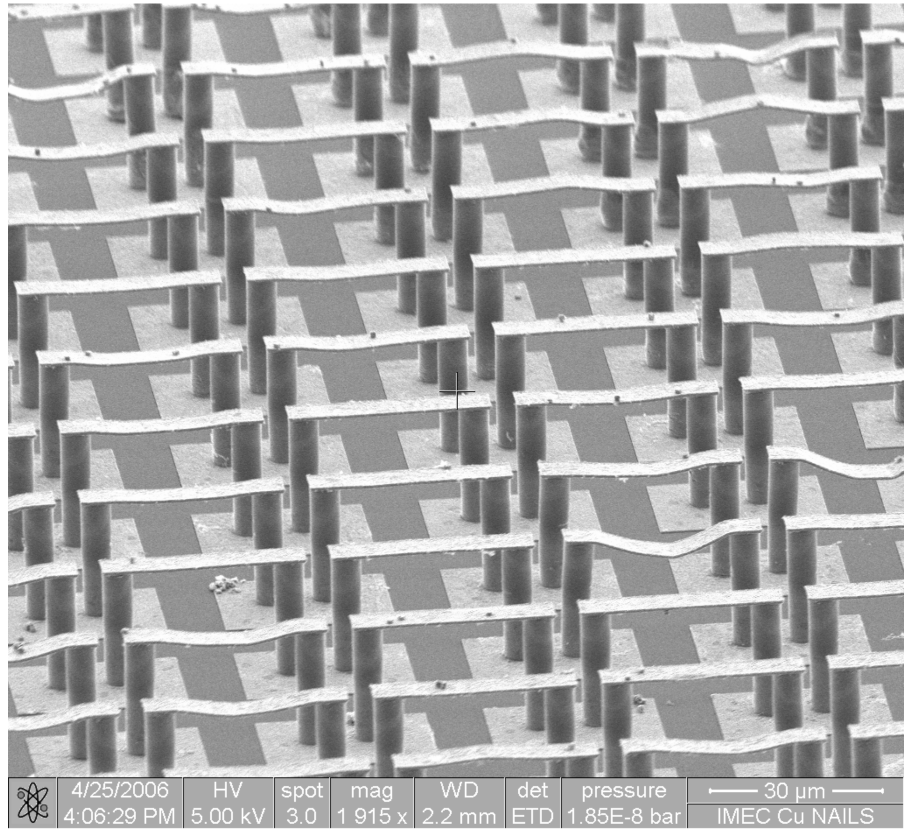




High density laminate with SMD passives on top side and Digital Base band chip on Bottom side

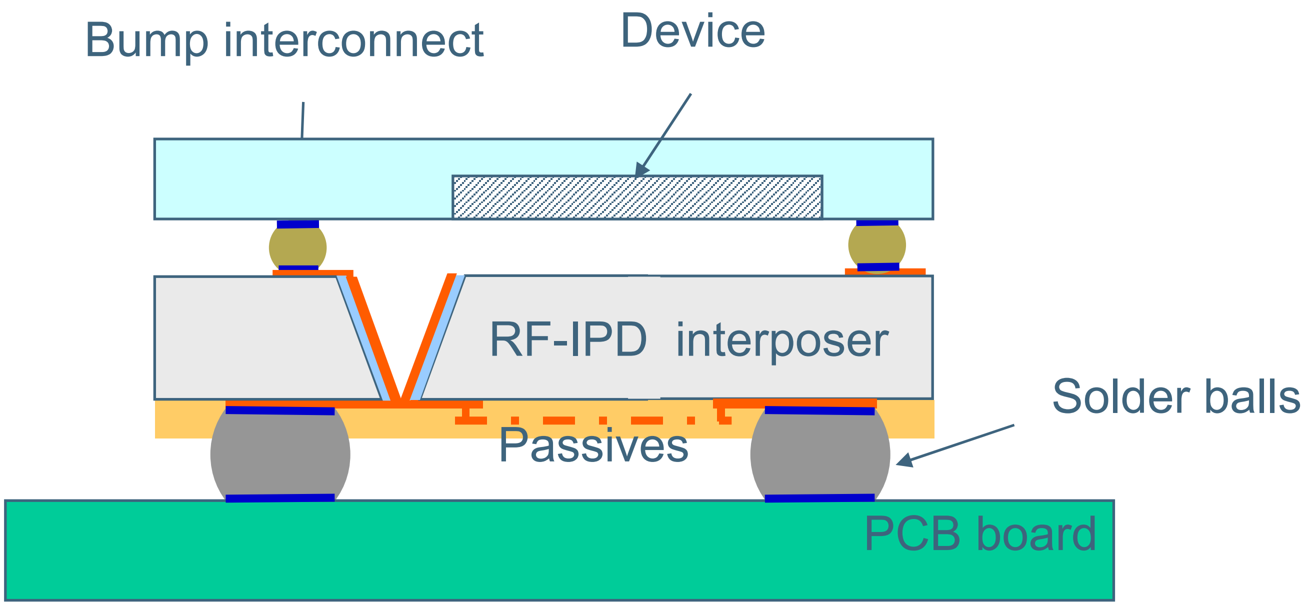
3D-SiC "Cu nail" technology





B. Swinnen et al.,
IEDM 2006

3D-WLP / TSV for RF applications



- Substrate thickness 100 um
- Non-critical interconnect density & pitch
- Via and bump “RF functional”

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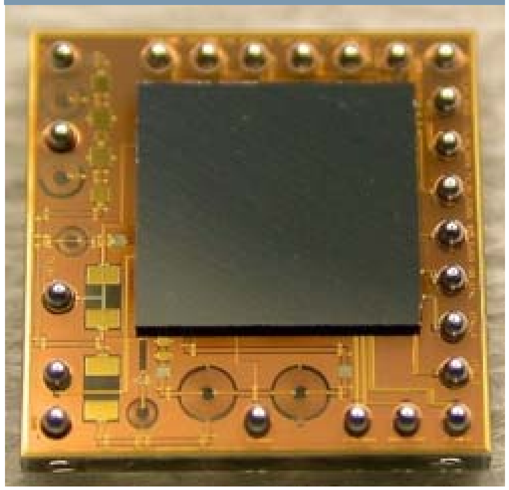
SiP Interposer Technology

- Several Technologies Possible:
  - Ceramic / Laminate / **Thin-film** / … -based MCM
- Thin film MCM-D offers
  - Wafer-level Processing
  - Photo-lithography defined features
    - Excellent control over lateral dimensions
    - High repeatability, high degree of miniaturization
  - Thin film deposited resistor & dielectric layers
    - High density, high precision, repeatable, small tolerances
  - MMIC design style possible
- Substrate choice
  - AF45 Glass
    - low cost, good RF properties
    - Primarily 2D technology (vias using sandblasting)
  - HR-Si
    - thermal advantages
    - micro-machining capabilities (cavities, through-hole vias)
    - 3D stacking

Glass SiP
Beyne, ISSCC2004

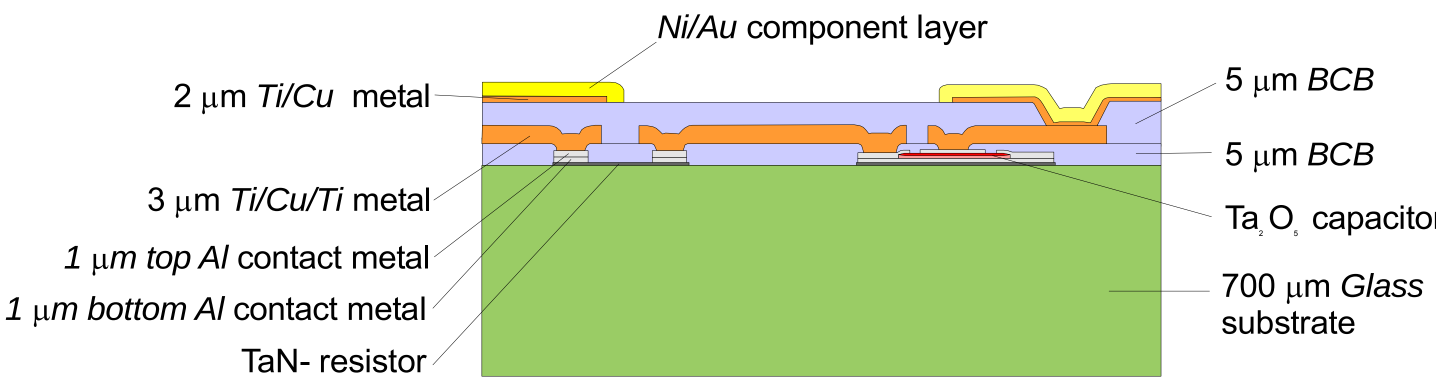


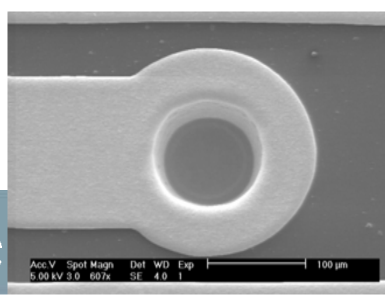
RF-IPD Technology
Multilayer Thin Film with Integrated Passives

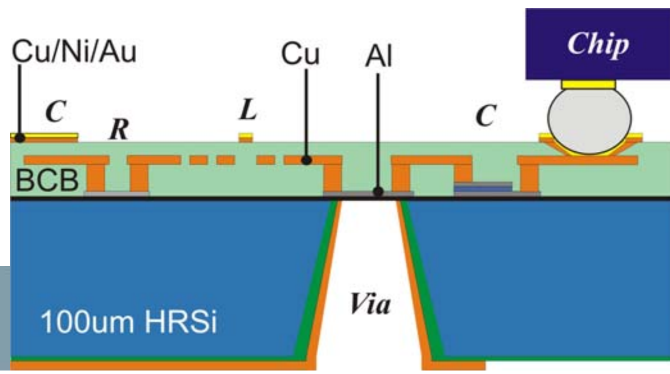
Main Features

- Substrate: glass or HR-Si
- 3 metal planes : Al / Cu / Cu-Ni-Au
- Coplanar waveguide (CPW) lines
  - Electroplated Cu : 3-5 μm thick
  - Smallest feature size : width/spacing: down to 5 μm / 7.5 μm

- Resistors : TaN (25 Ω/□)
- Capacitors : Ta_2O_5 (0.72 nF/mm²) & BCB (6.5 pF/ mm²) & interdigital
- Inductors : 0.6 to 80 nH, Q : 30 - 150
- Flip-chip / wirebond interconnections
- Integrated vias on HR-Si



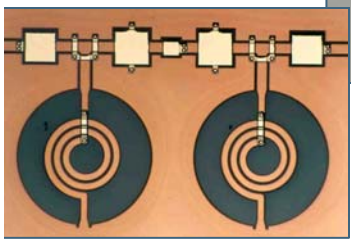




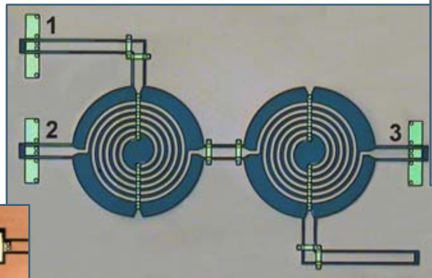
3D-WLP vias

RF-IPD on AF45

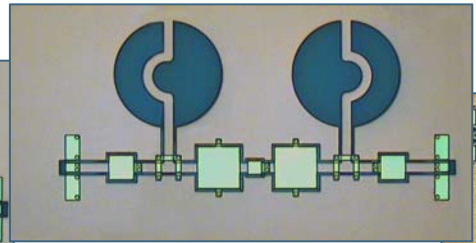
Passive Circuits & Demonstrator Modules



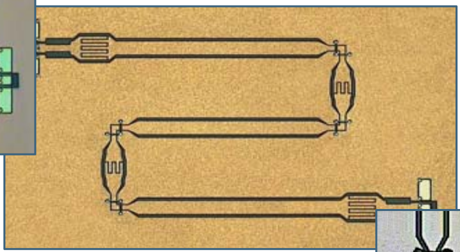
2.45GHz BP Filter



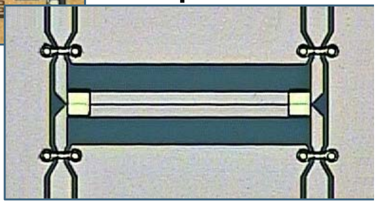
3-5GHz Balun



5.2GHz BP Filter



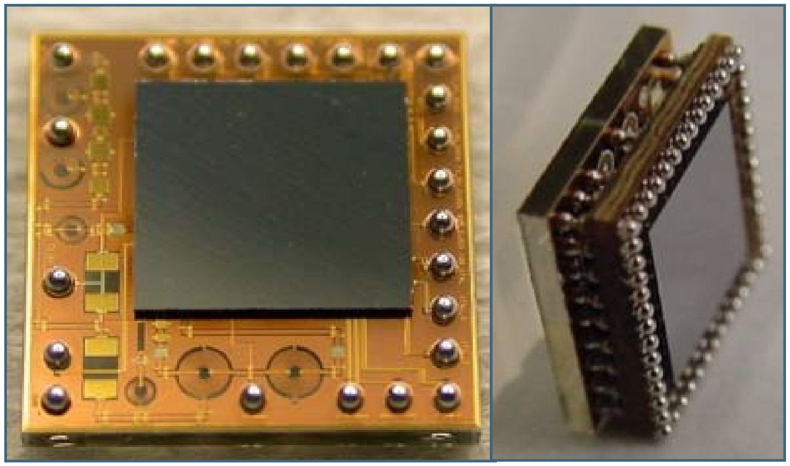
30GHz BP Filter



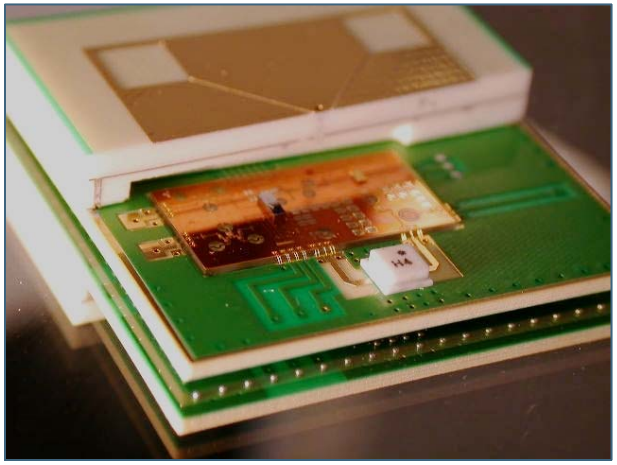
31-60GHz Coupler

Passives

Modules



2.4GHz RF Radio

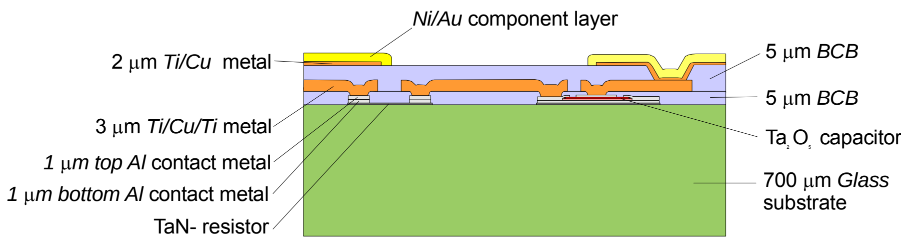


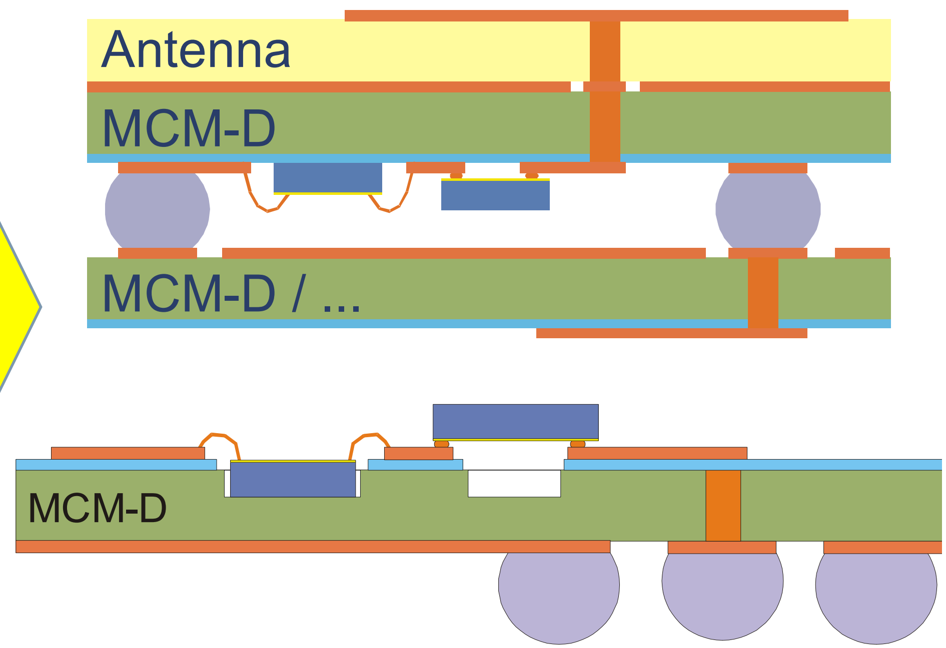
5.2GHz WLAN Front-End

MCM-D on HR-Si
Why investigate HR-Si: Possibilities

- Possibilities
  - 2D & 3D Modules
  - Integrated cavity resonators
  - Integrated waveguides/filters

Enabled by bulk micromachining & RF-vias

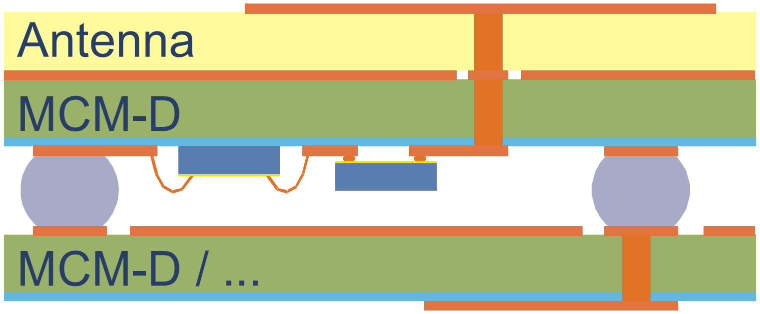




IMEC HR-Si IPD Platform Activities

Core activity:

HiRes Si technology with vias

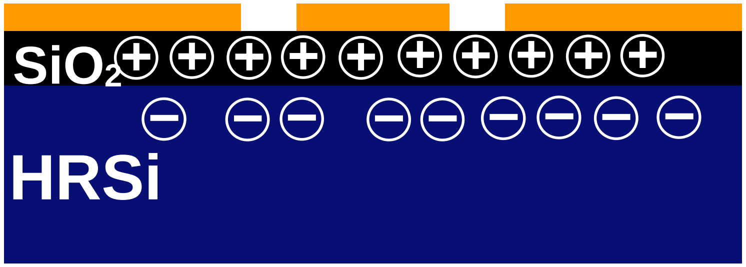


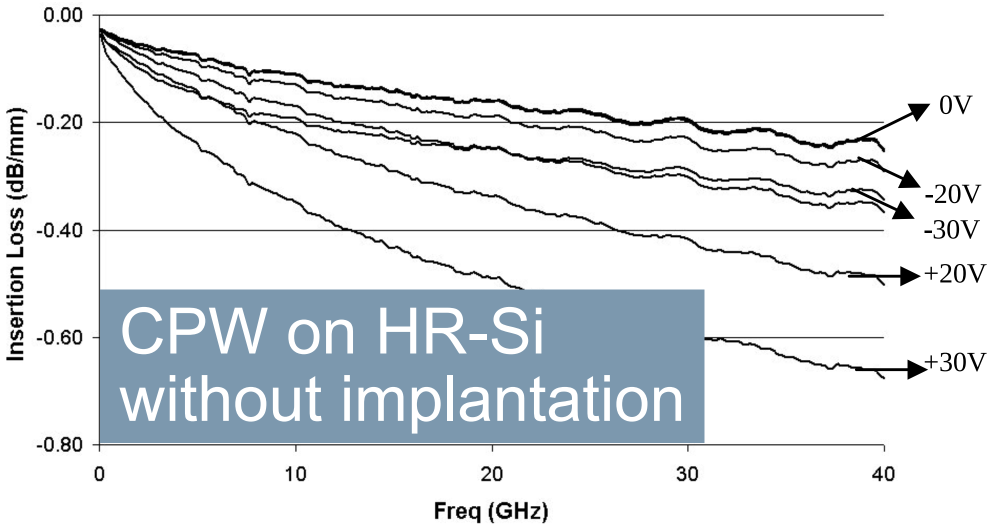
Activities

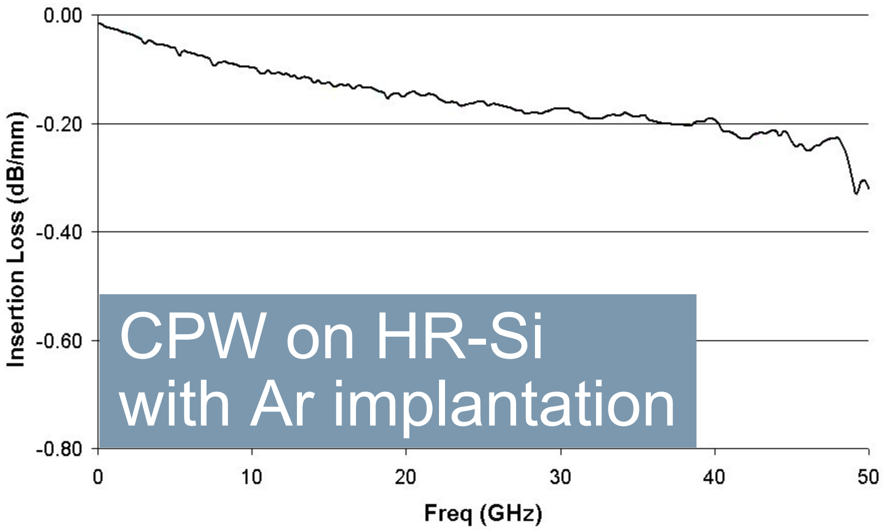
- HR-Si technology development and optimization
    - vias, HR-Si
    - use of cavities vs. UTCS for RF devices
- RF component library development and RF-via design (AF45, HiRes)
- Technology reliability and thermal properties
- RF vs temperature / substrate resistivity influence on passive performance
- Interconnections at die-module and at module-module level
- Exploration of new devices:
    - antennas, mm-wave functions (couplers, waveguide structures ...)
- Circuit/module demonstrators:
  2.4GHz – 5GHz – 17GHz – 30GHz – 60GHz – 77 GHz - 94GHz

RF-IPD on HR-Si
Integrated Passives

- Surface passivation oxide-HRSi interface
  - fixed charges in oxide cause DC dependancy & performance spread
  - Ar implantation
    - increased performance
    - lower spread
    - lower DC-bias dependancy





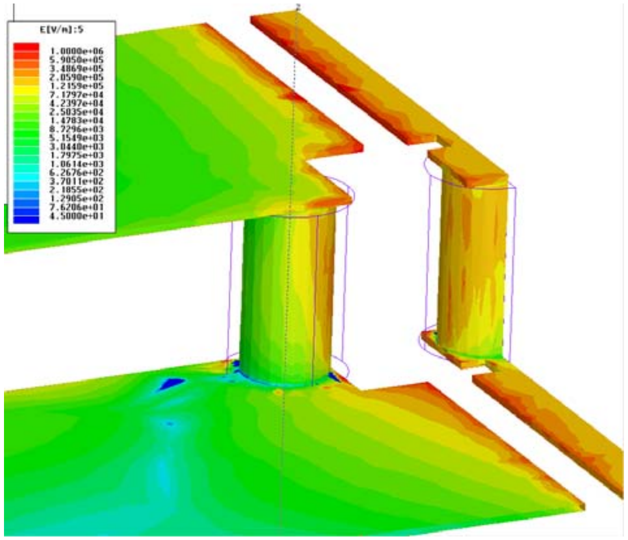


Best Student Paper
EuMIC 2006

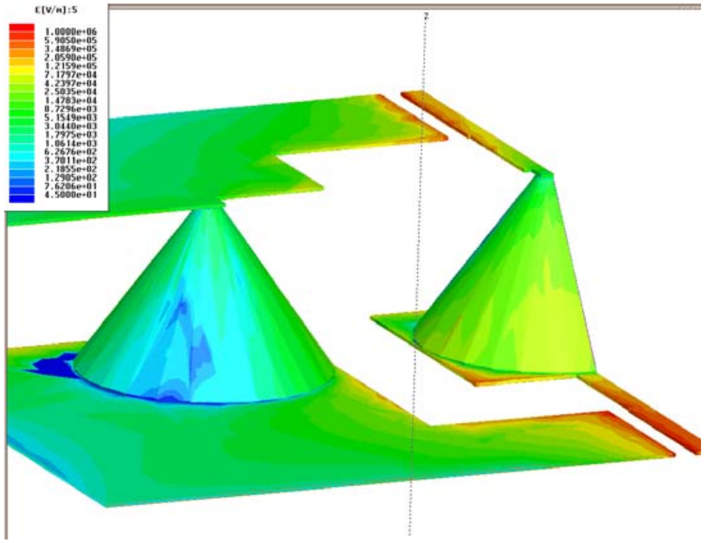
RF-IPD on HR-Si
Via Requirements

- RF feedthrough optimization
  - Wafer thickness
  - Via diameter
  - Pitch
  - Compensation section (inductive)

DRIE etching



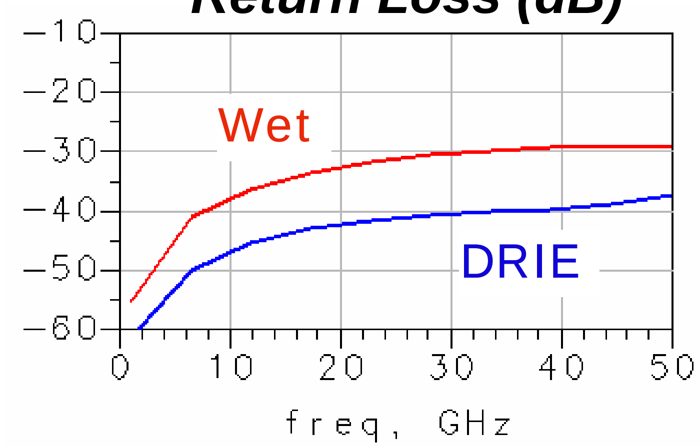
Wet etching



RF-IPD on HR-Si
DRIE vs Wet Etched Vias

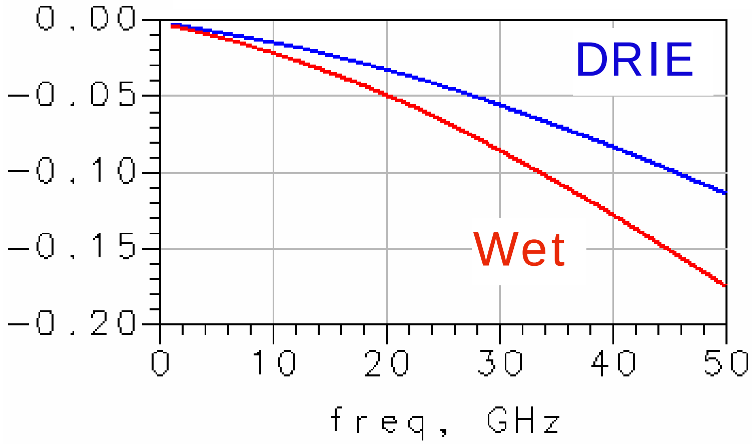
- Chosen wafer thickness 100um
  - Better performance
  - Smaller size
  - Wafer thinner than 100um too fragile
- DRIE etched vias
  - Better performance than wet
  - Smaller size (better for low freq. applications as well)

Return Loss (dB)



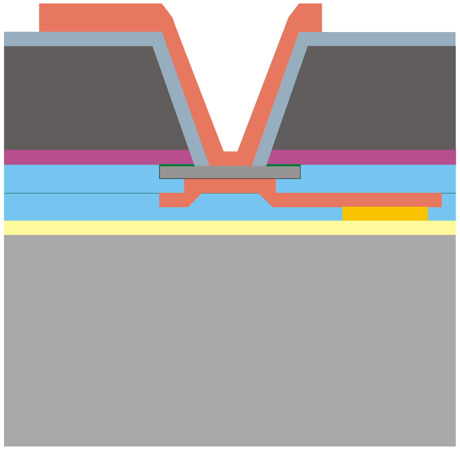
Wth=100um

Insertion Loss (dB)

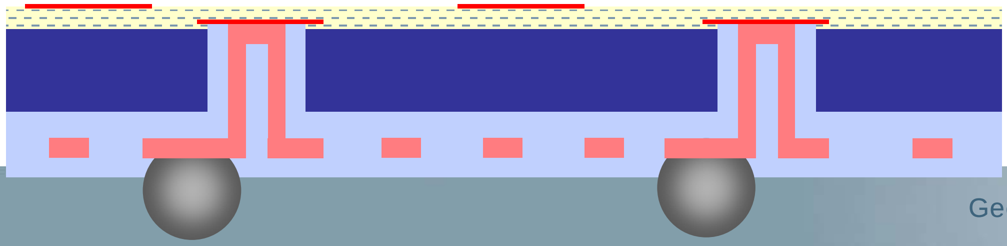


RF-IPD on HR-Si
Through-Si-Via interconnects

- IMEC approach :
  - Via from back of the wafer
  - Thinning first approach
  - Use of a thick polymer isolation layer
  - Partial fill via hole by electroplated copper
  - Polymer fill remaining via hole

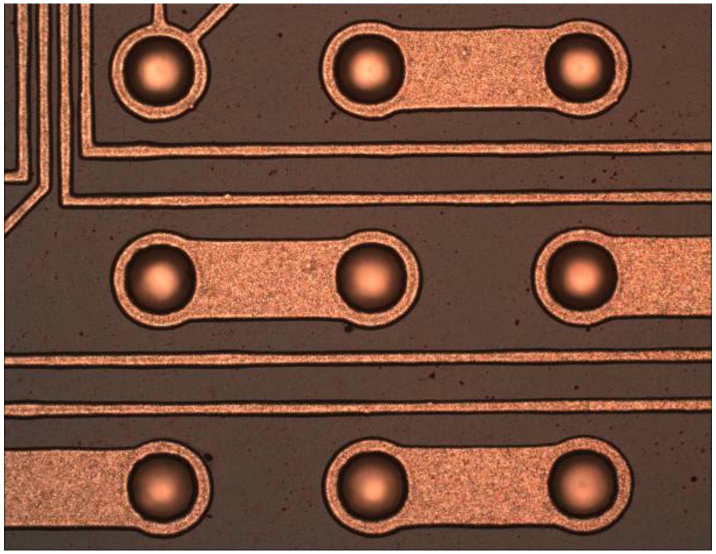


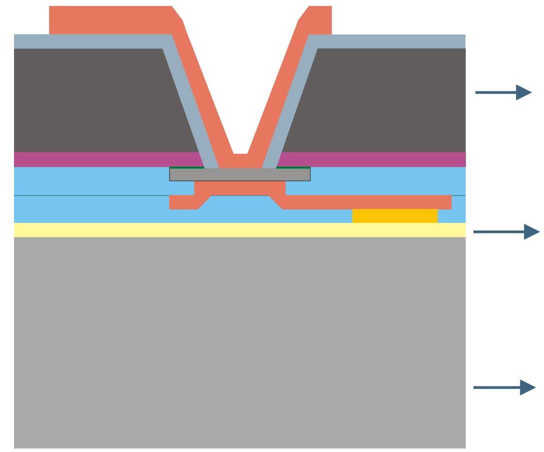
- Advantages:
  - No holes in wafer topside
  - Reduced capacitance through the use of thicker low-k isolation layers.
  - Reduced thermo-mechanical stress : “compliant” through-hole structure
  - Compatible with wafer-level packaging technologies



RF-IPD on HR-Si

Application 3D-WLP TSV for HR-IPD integration

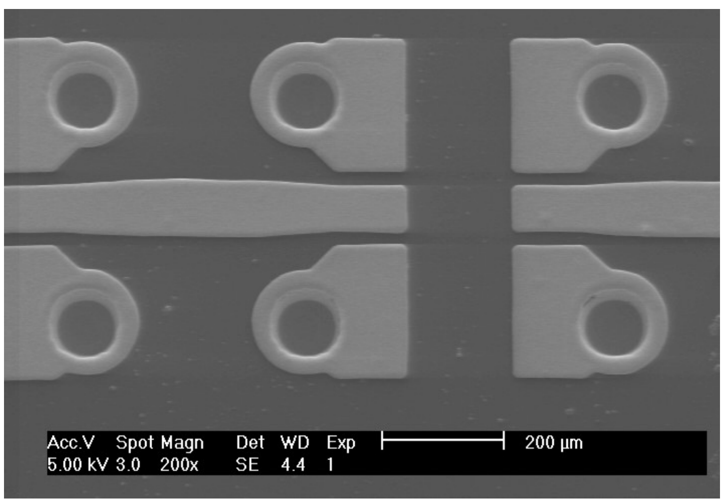


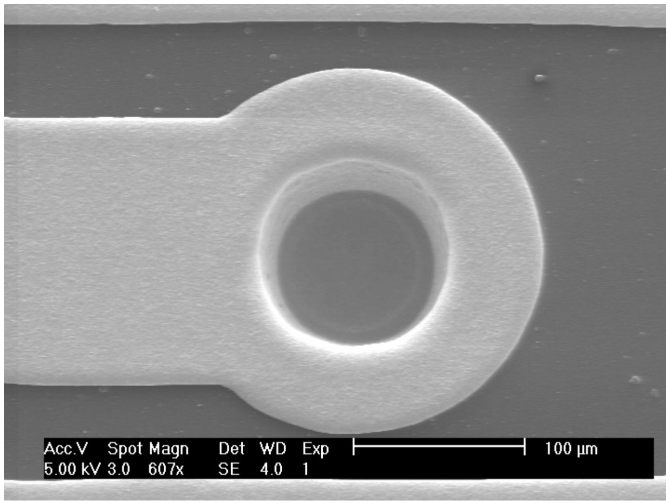


HR-SI
IPD wafer
(100 µm)

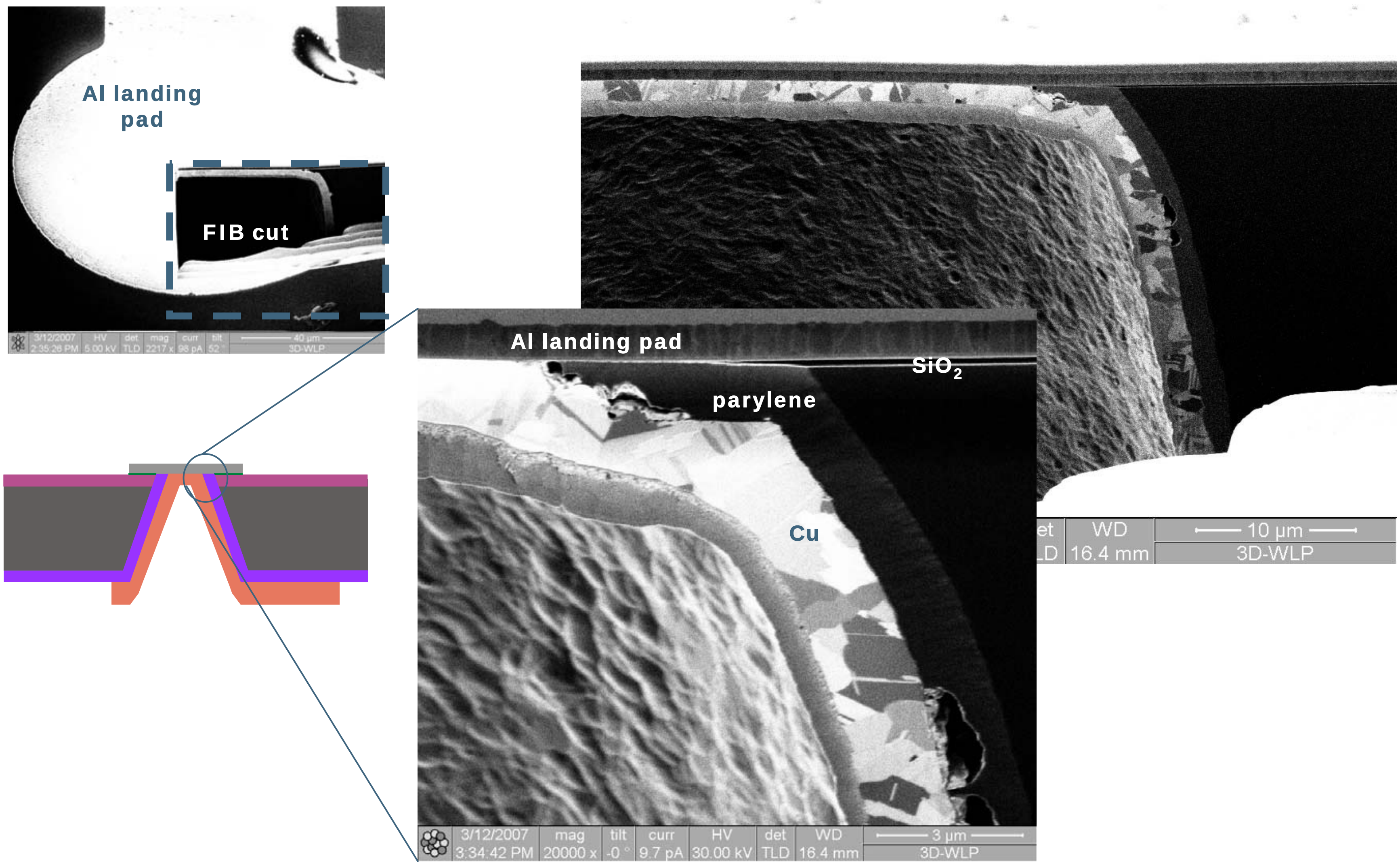
temporary
glue

Carrier
wafer

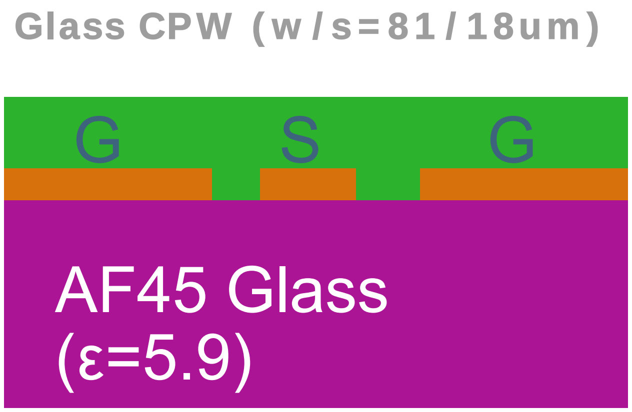


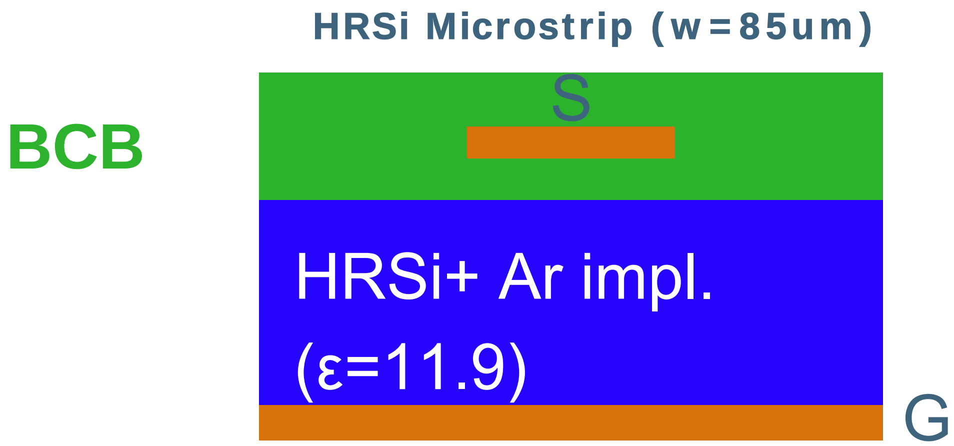


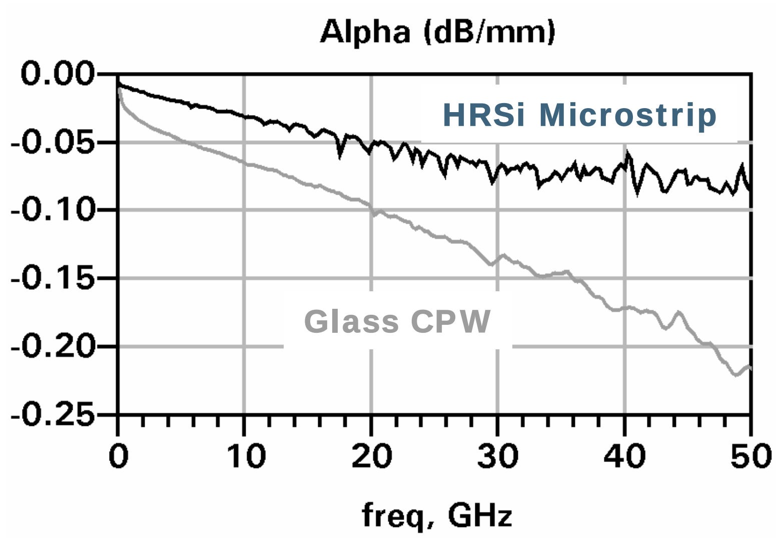
RF-IPD on HR-Si
FIB on completed via (bottom)

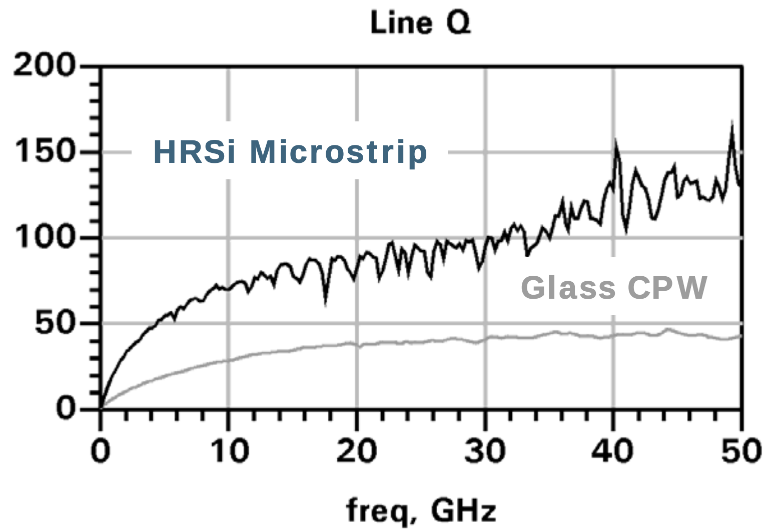


RF-IPD on HR-Si
Comparison MS on HRSi to CPW on Glass



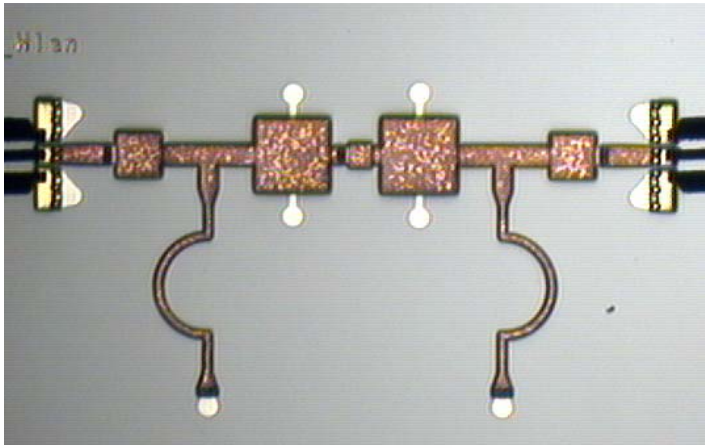


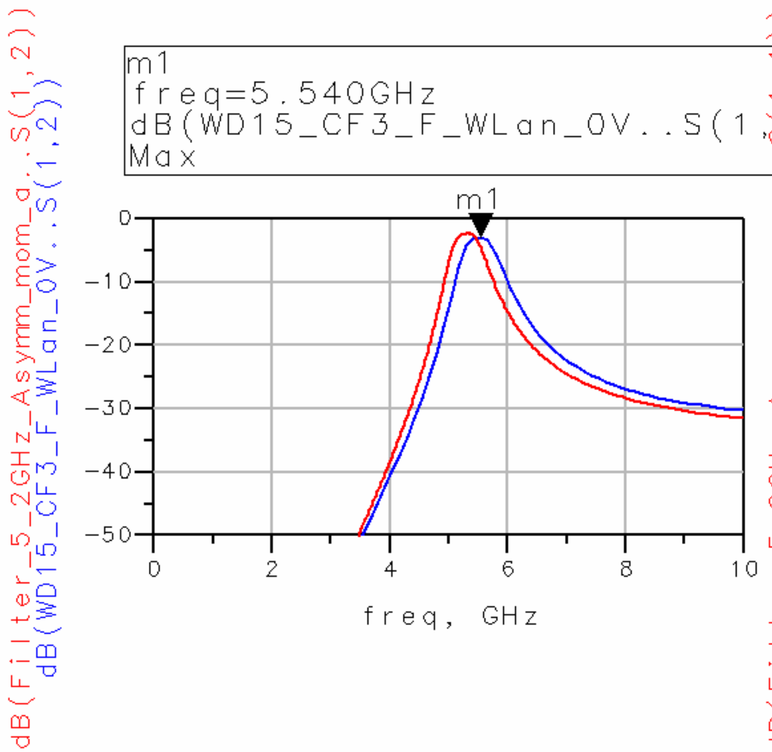


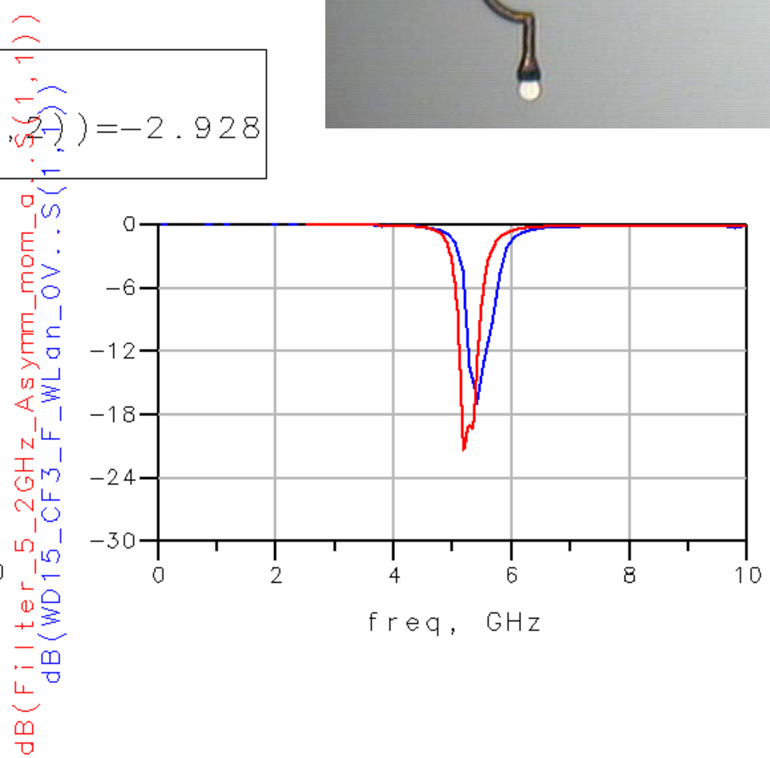


RF-IPD on HR-Si
MS WLAN Filter

- Lumped element filter

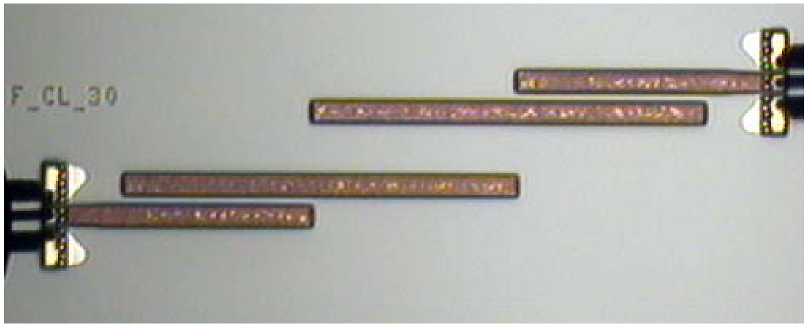




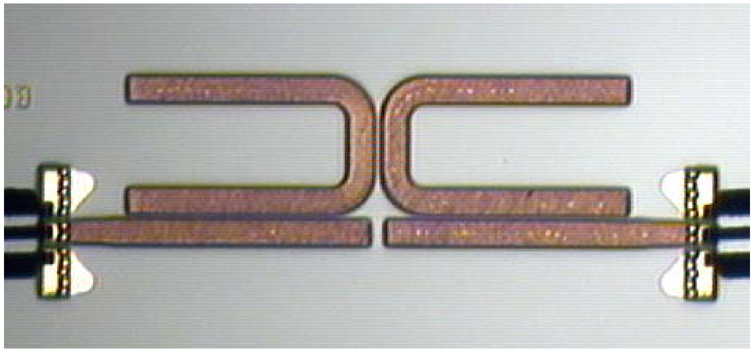


RF-IPD on HR-Si
Coupled line filters at 30GHz

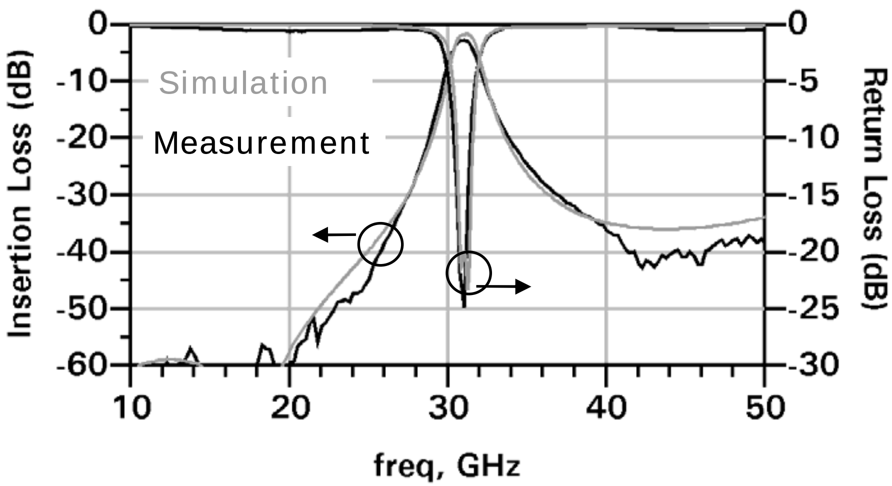
Standard



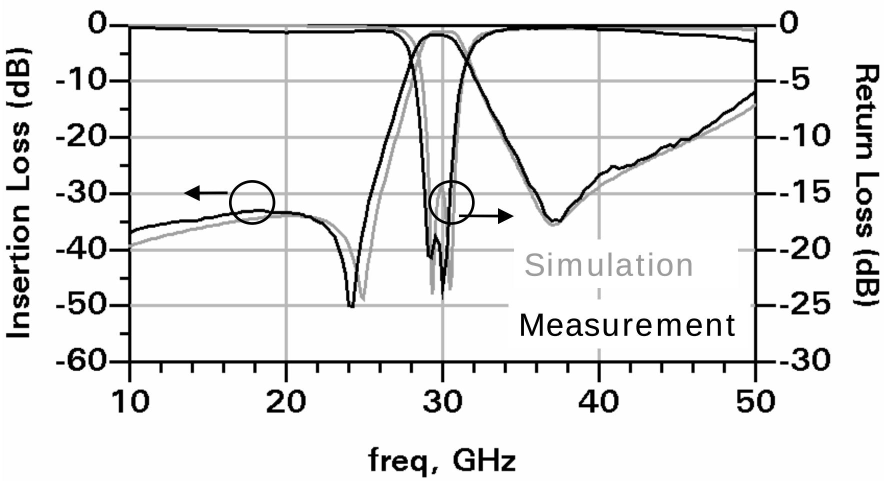
With transmission zeros



5.1% Bandwidth
2.1dB IL

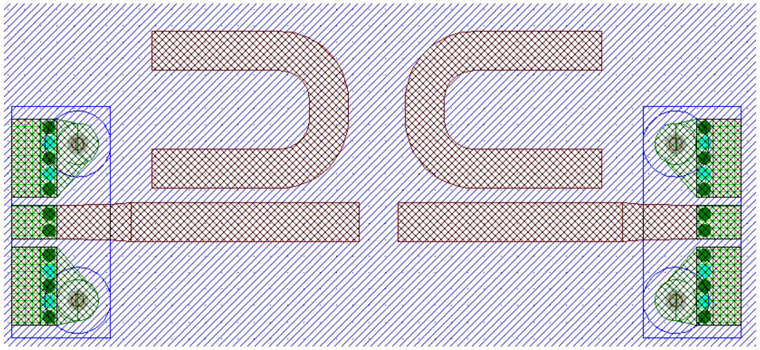


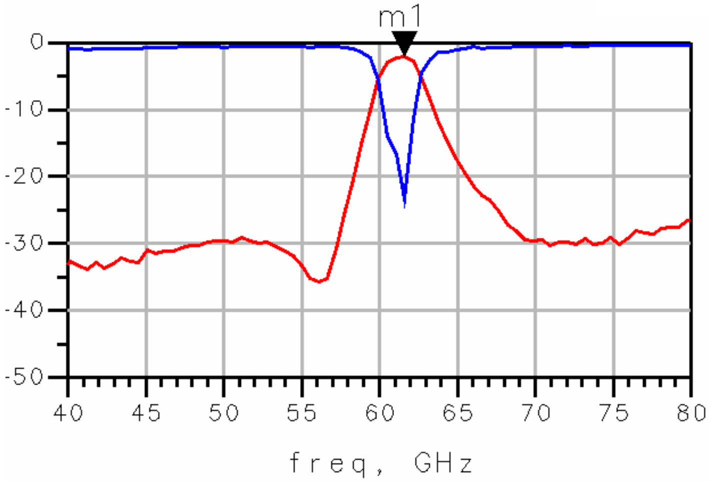
10% Bandwidth
1.7 dB IL



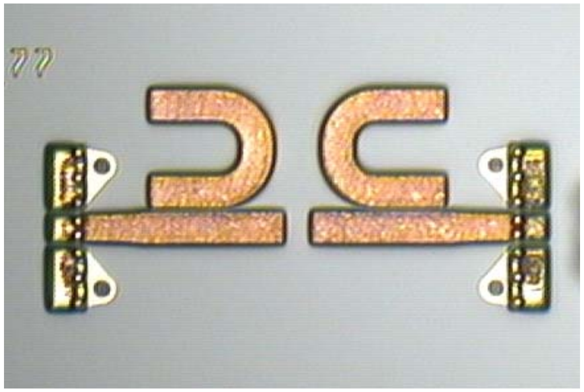
RF-IPD on HR-Si
Coupled line filters at 60GHz and 77GHz

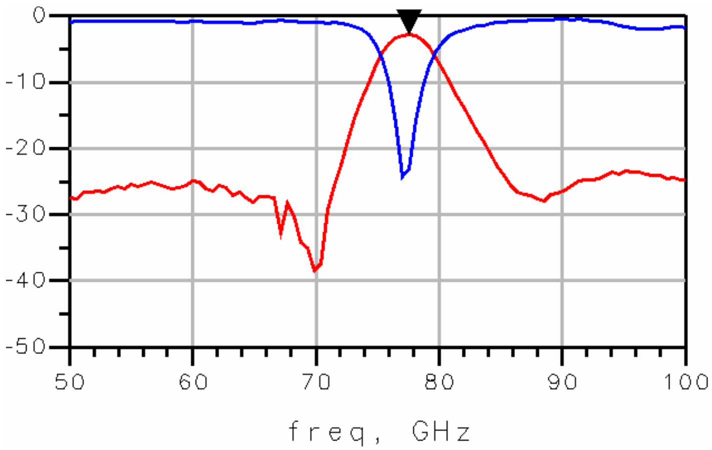
- 60GHz
  - IL: -2dB





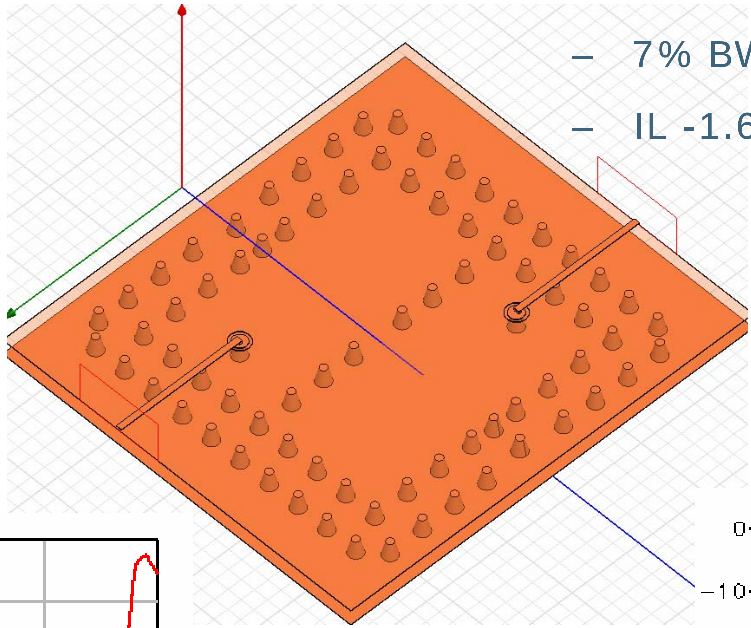
- 77GHz
  - IL: -2.8dB

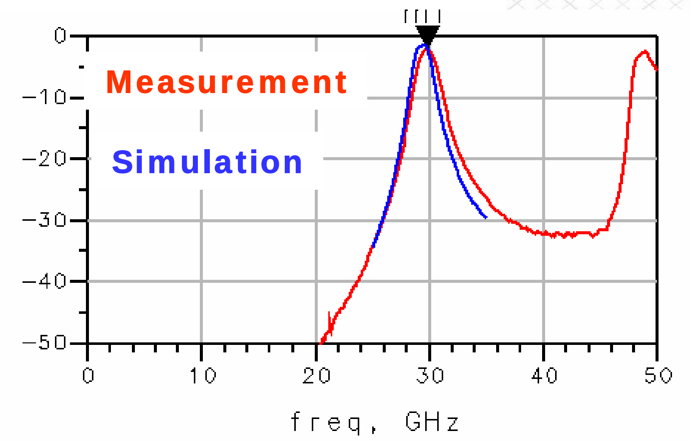


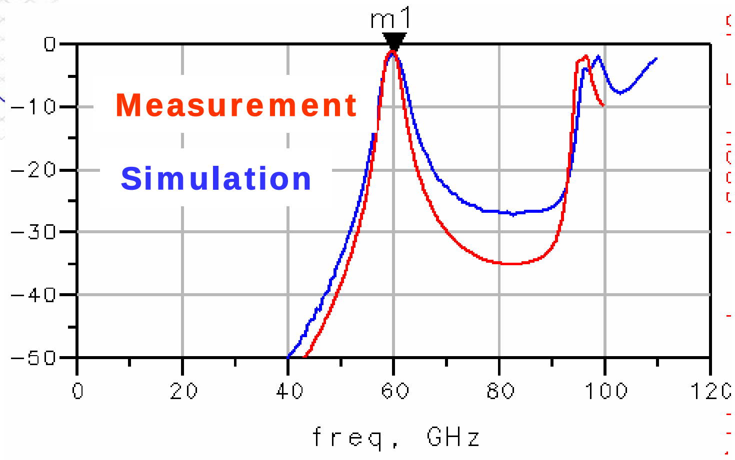


RF-IPD on HR-Si
Cavity Filters 30GHz & 60GHz

- 30GHz
  - Good fit with simulations
  - 5.4% BW
  - IL -2dB
- 60GHz
  - Good fit with simulations
  - 7% BW
  - IL -1.6dB



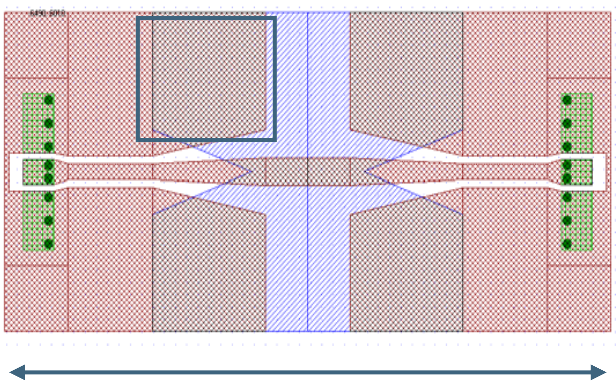




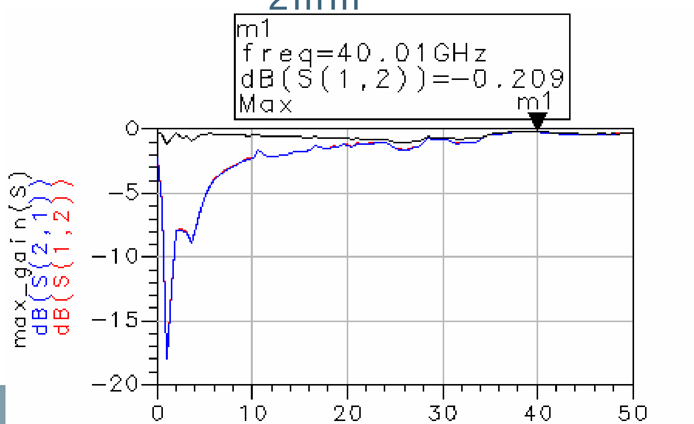
RF-IPD on HR-Si
Vialess transitions

- CPW to CPW
  - 0.1 dB loss / transition
  - RL < -20dB: 20-50GHz

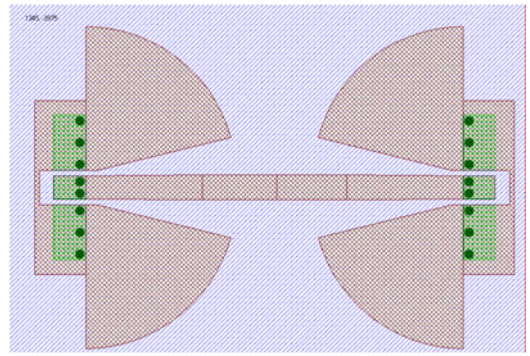
400x400um

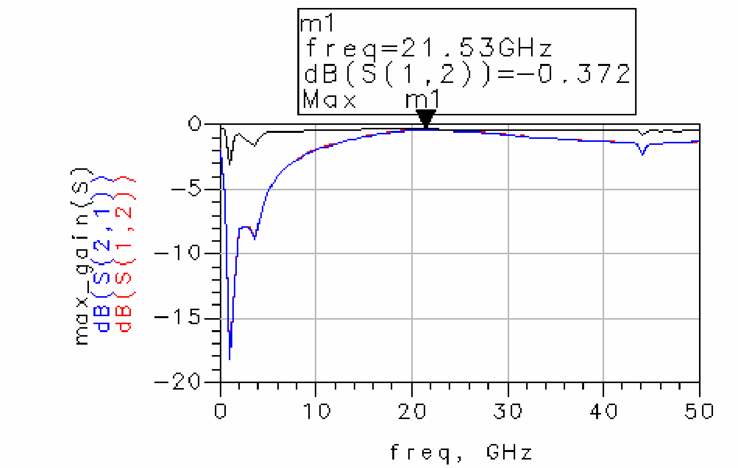


2mm



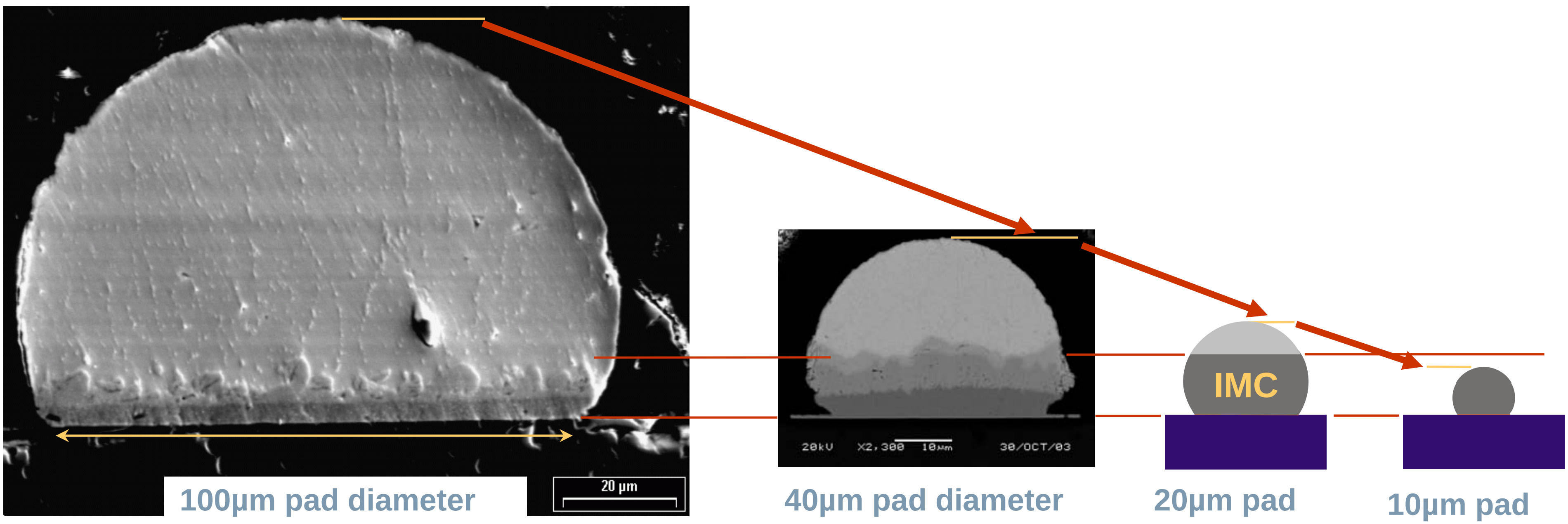
- CPW to microstrip
  - <0.2 dB loss / transition @ 20GHz
  - RL < -20dB: 18-24GHz





Micro-bump joining

- **Flip-chip interconnect scaling**
- With solder joint scaling, the intermetallics formed by UBM solder interaction are of increasing importance
- For the smallest flip chip pitches : only intermetallic compounds after solder bump reflow



100µm pad diameter
150-200µm bump pitch

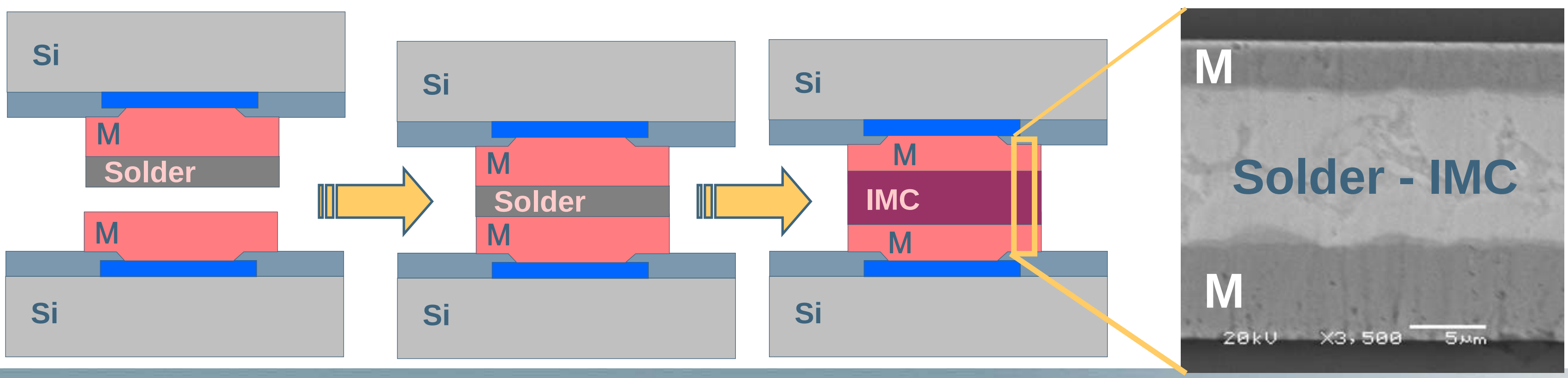
40µm pad diameter
60µm bump pitch

20µm pad
40µm pitch

10µm pad
20µm pitch

Micro-bump joining

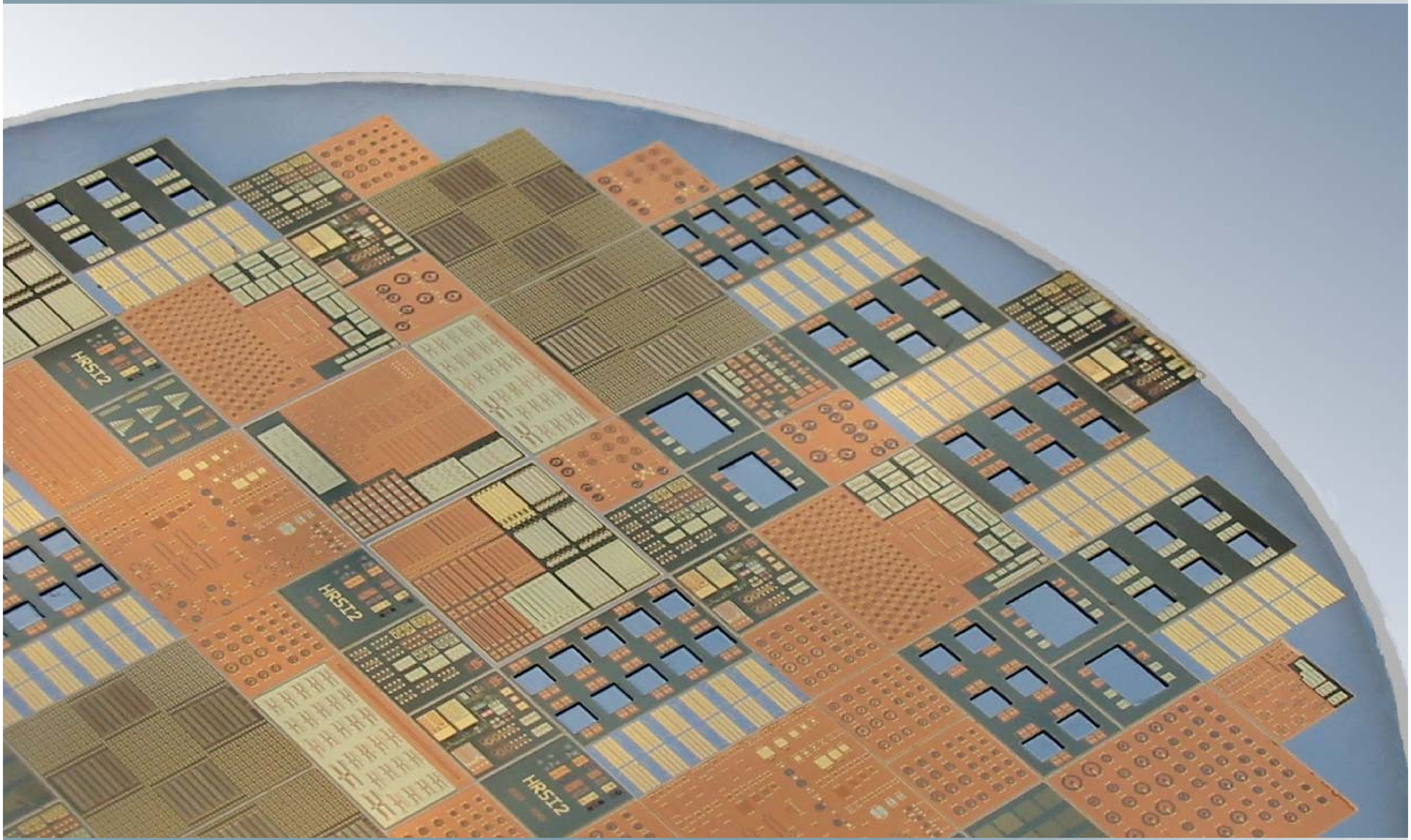
- **Micro-bump**
- Similar to flip chip interconnect,
- *uses a low temperature melting metal or alloy and realizes an inter-metallic connection*.
- However:
  - **Small dimension : no solder 'ball', typically < 10µm thick**
  - **Connection by thermo/compression-reflow method**
  - **Entire solder volume is transformed into an intermetallic compound.**
  - **Thin connection, allows for small thickness variation across the die and bonding substrates (< solder thickness/2)**



Conclusions

- 3D is an enabling technology for the realization of miniature RF components
  - Minimal footprint
  - Increased functionality in reduced volume
  - High performance interconnection of heterogenous technologies
  - Various RF application areas
    - 3D modules, e.g. using TF technology
    - MEMS packaging
    - Antenna integration
  - Small vias required
    - Minimize area
    - Higher operating frequency
- Acknowledge ESA 3DMoP Project

Questions: Geert.Carchon@imec.be



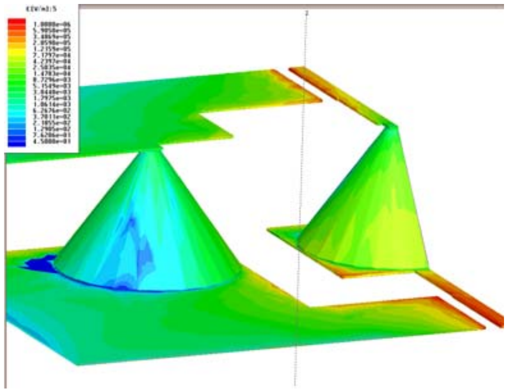
aspire invent achieve

imec

Target specifications for 3D ‘flavors’

	3D-SIP	3D-WLP		3D-SIC
Technology	Package interposer	WLP, Post-passivation		Si-foundry, Post FEOL
3D interconnect	Package I/O	UTCS Embedded die	TSV (Through-Si Vias)	Si-through “Cu nail” vias
Intercon. Density	‘package-to-package’	‘around’ die	‘through’ die	‘through’ die
Peripheral	2 - 3 /mm	10 - 50 /mm	10 - 25 /mm	25 -100 /mm
Area-array	4 - 11/mm^2	100 - 2.5k/mm^2	16 - 100/mm^2	400-10k/mm^2
3D Si Via pitch	-	-	40 – 100 µm	< 10 µm
3D interconnect pitch	300 – 500 µm	20 – 100 µm	-	-
3D Si Via diameter	-	-	25 - 100 µm	1 - 5 µm
Die thickness	> 50 µm	10 - 20 µm	50 - 100 µm	10 - 20 µm

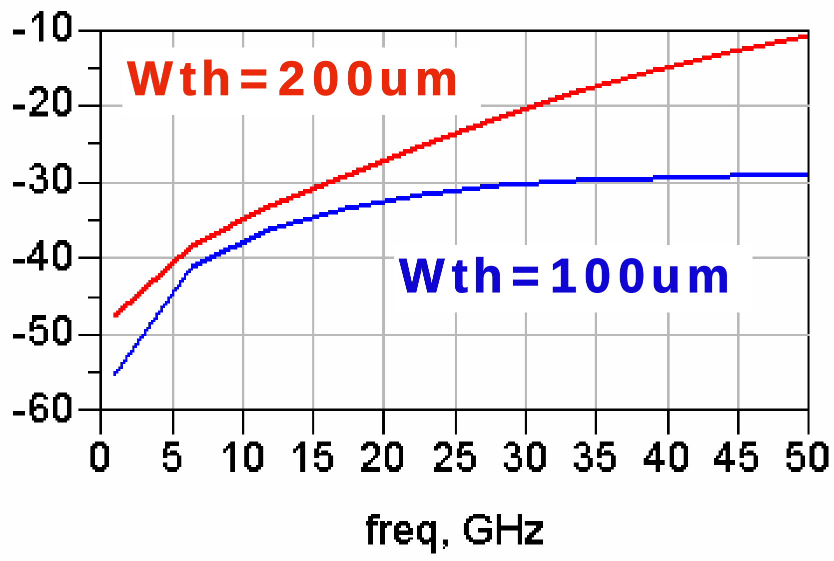
RF-IPD on HR-Si
Wet Etched Vias RF feedthrough



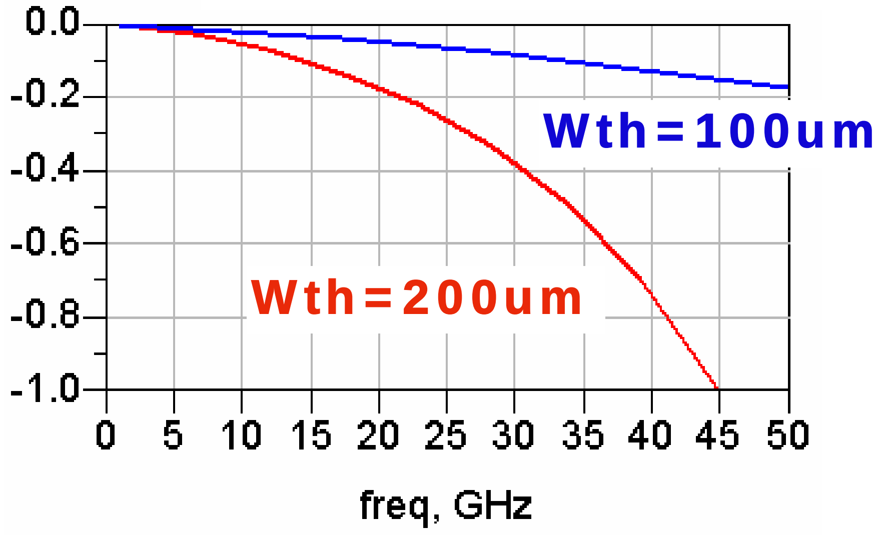
Wth	Top D	Bottom D
100um	30um	175um
200um	30um	320um

- Thinner wafer
  - Better return loss
  - Lower insertion loss
  - Considerably smaller (constant etching slope)

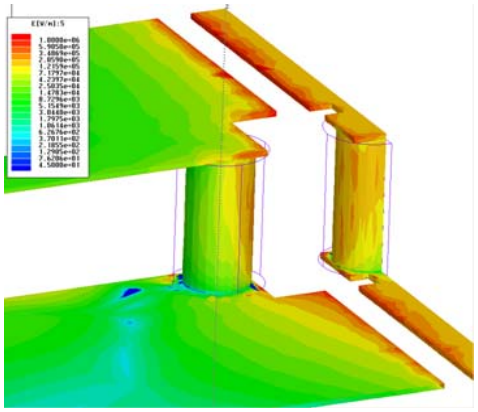
Return Loss (dB)



Insertion Loss (dB)

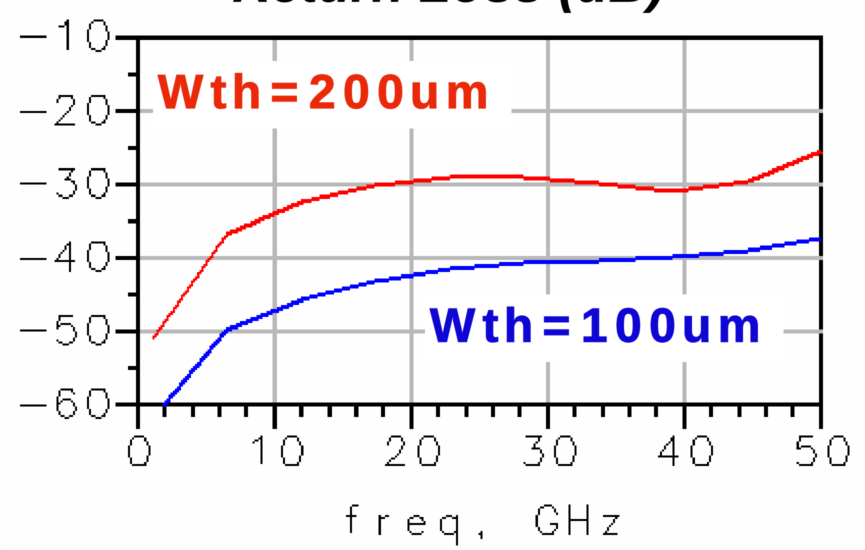


RF-IPD on HR-Si
DRIE Etched Vias RF feedthrough

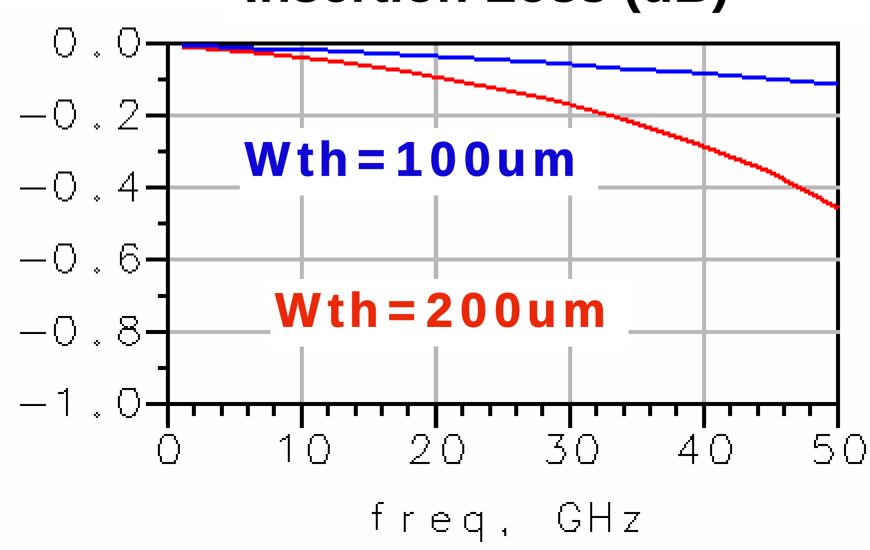


- D=100um
- Thinner wafer
  - Better return loss
  - Lower insertion loss
  - Smaller (lower pitch and shorter matching section)

Return Loss (dB)

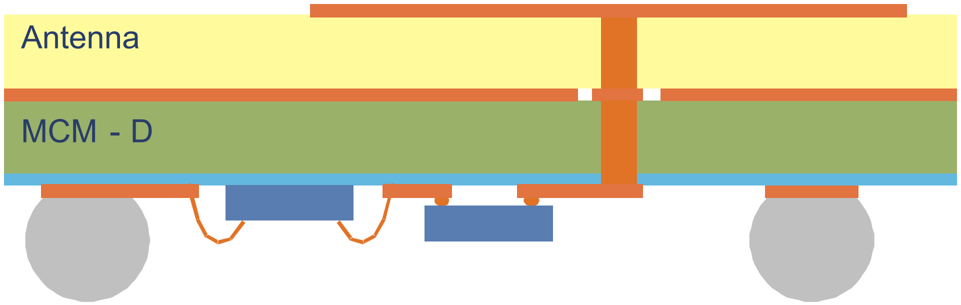


Insertion Loss (dB)

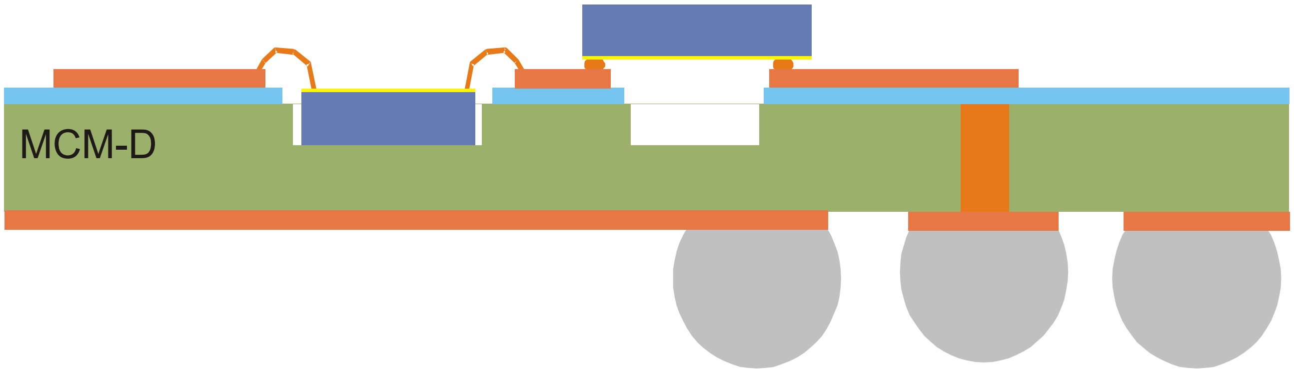


RF applications

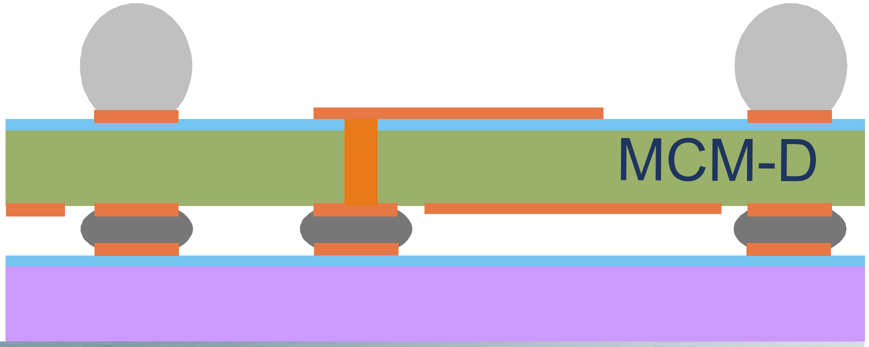
- Tile antenna array



- Hot via



- Heterogenous IPD stacking
  - e.g. including MEMS packaging



3DMoP Project Objectives
3D Microwave Module Packaging

- Investigation of packaging issues and solutions for 3D stacked microwave modules
  target frequency = 1…30GHz

  – Optimization of the high-resistivity Si substrate and MCM-D technology for high-quality RF components

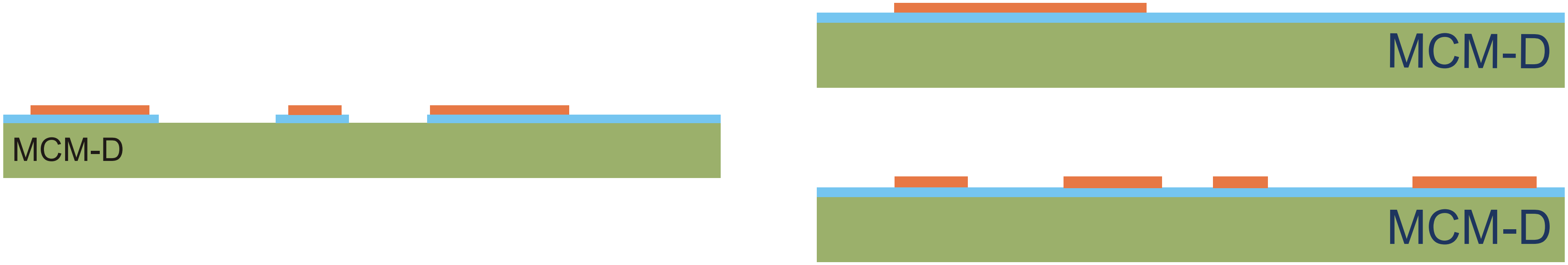
  – Design and integration of through-substrate vias
    - For the realization of RF feedthroughs
    - To connect ground layers on different layers, preventing parasitic modes and its associated coupling

  – Interconnections at the die-module and at module-module level

  – Exploration of the improvements and limitations of the concept with respect to thermal performance and thermo-mechanical reliability

Project Objectives

- Optimization of the high-resistivity Si substrate and MCM-D technology for high-quality RF components



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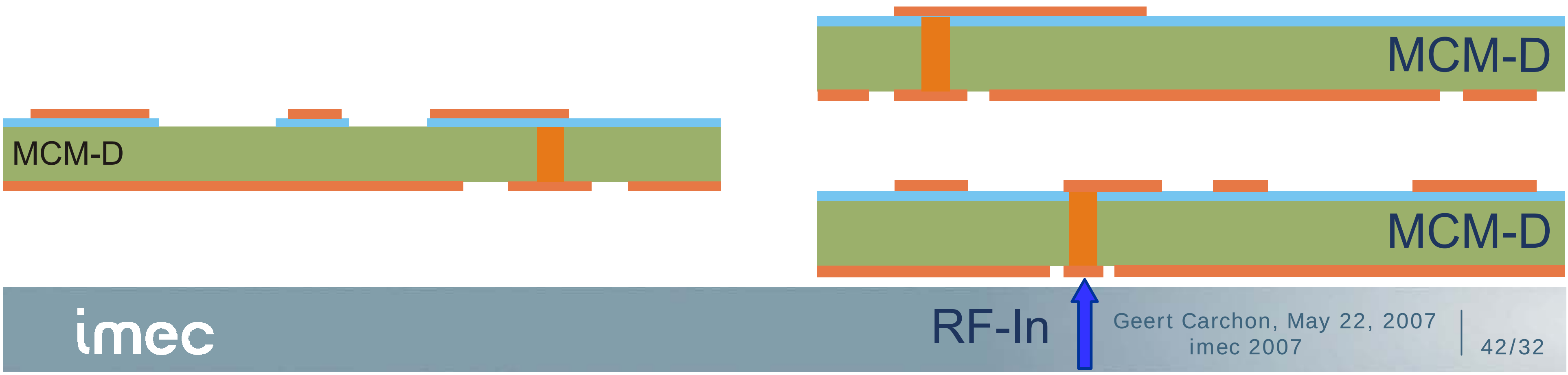

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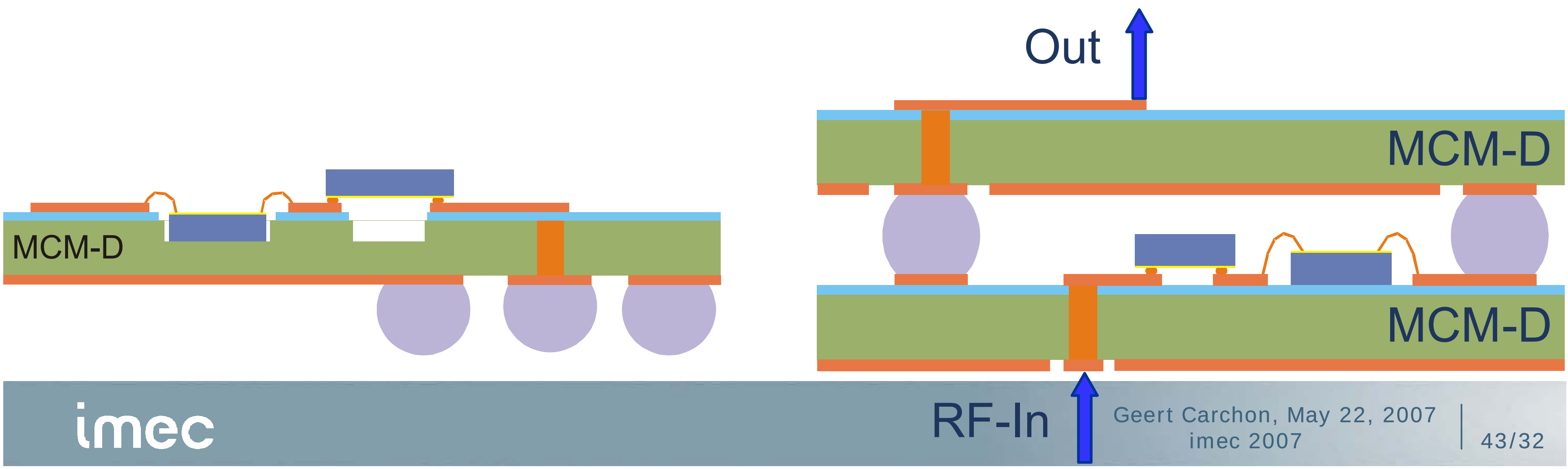

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