Experimental Validation of Fault Injection Analyses with the FLIPPER Tool

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Motivations

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• FLIPPER is FI tool to study SEUs in SRAM-FPGAs

- ESA/ESTEC contract 18559
- SEUs in SRAM-FPGAs affect not only flip-flops and user memory, but also the device configuration memory and thus the logical function of the circuit as well
- The fault model in FLIPPER is the bit-flip of configuration memory cells

CAN WE RELIABLY USE FLIPPER FOR PREDICTION PURPOSES???

Accelerator validation is needed!!!!



- FLIPPER injects bit-flip faults within the FPGA configuration memory by means of partial re-configuration
- The system consists of a hardware platform and a software application running on a PC
- DUT device is an XQR2V6000 device hosted on a piggy-back board, stacked on the control board
- Test vectors and reference values for the functional test of implemented designs are imported by the software application from an external HDL simulator

FLIPPER Boards

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Sample design

• ESA benchmark design consisting of modules

- FFT: Fourier Transform of a data matrix
- MULT16_LUT: 2-stage 16x16 bit multiplier instantiated twice
- MULT16_MULT18: 10-stage 16x16 bit multiplier instantiated twice (embedded)
- FFmatrix: two identical copies of a shift register chain (480 bits each)
- ROMff: two copies of a shift register (256 bit each); the former is loaded and holds the stored values, the latter reads the values stored by the former

V1 and V2 design variants

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- V1 is derived from the unprotected design by straightly applying the TMRtool.
- In V2 a dummy feedback path, controlled by a multiplexer, is inserted for each flipflop (the TMRtool is forced to instantiate a voter for every flip-flop in the design)

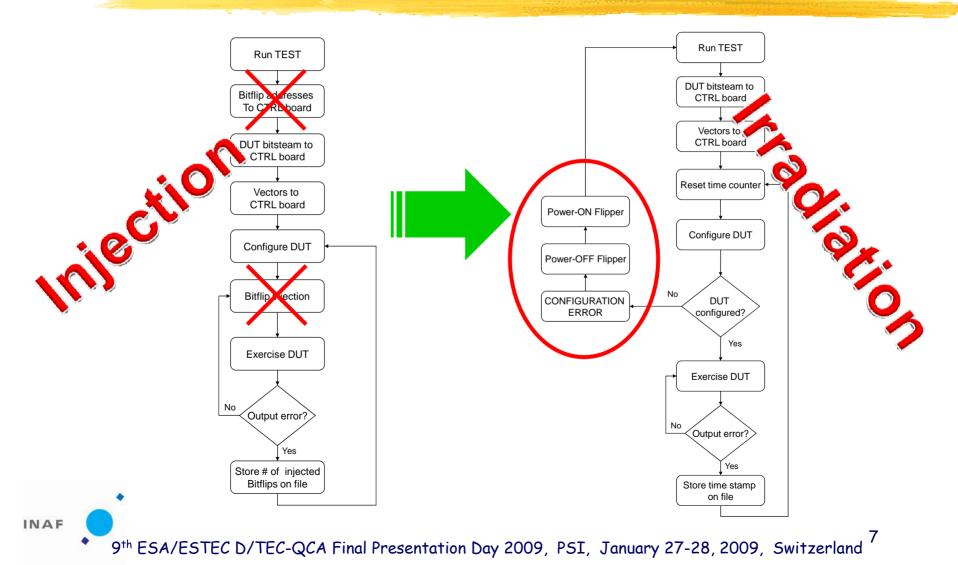
Resource	Plain	V1	V2	
Slice FF	2,926 (4%)	8,778 (12%)	8,778 (12%)	
LUT	3,806 (5%)	13,437 (19%)	29,217 (43%)	
IOB	87 (10%)	264 (32%)	267 (32%)	
MULT 18x18	32 (22%)	96 (66%)	96 (66%)	
GCLK	1 (6%)	3 (18%)	3 (18%)	

FI campaign

Accumulation mode

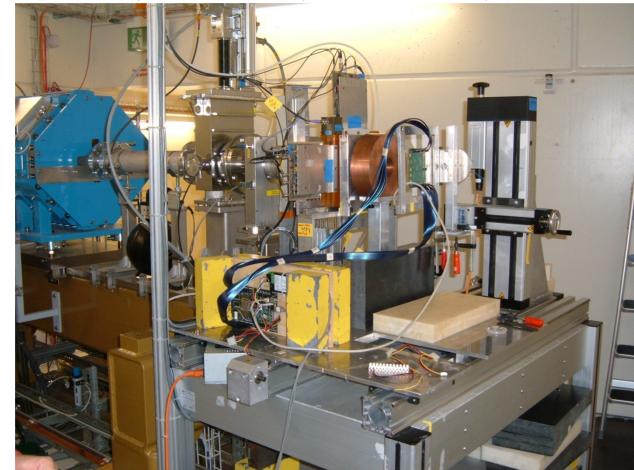
- the altered bit is NOT restored before the successive injection is performed
- mimics the irradiation exp (without scrubbing)
- Configuration memory bits are flipped according to a random list of memory locations
- About 1000 runs for each variant; predefined maximum number of inj. = 100,000

Procedures





PSI, Switzerland, November 23, 2008



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Irradiation experiment



- 180 MeV proton beam (nominal)
- average flux : ~ 6.5·10⁷ cm⁻² s⁻¹
 - 1 CBU at most during test vector application
 - CBU_{rate} : ~ 80 s⁻¹
- stimuli: ~ 28,000 vectors@10 MHz
- total exposure time: ~ 12 hours
- Fluence: ~ 2.19.10¹² p/cm⁻²
- TID: < 140 krad
- \sim 600 samples for V2, \sim 400 samples for V1

Symbol	Description	Min	Мах	Units
TID	Total Ionizing Dose Method 1019.5, Dose Rate ~50.0 rad(Si)/sec	200	-	krad(Si)
SEL	Single Event Latch-up Immunity Heavy Ion Linear Energy Transfer (LET)	160	-	(MeV-cm ² /mg)
SEFI	Single Event Functional Interrupt GEO 36,000km Typical Day		1.5E-6	Upsets/Device/Day

XQR2V6000 : device specification

Device static proton cross section (per bit)

3.10⁻¹⁴ cm² @198 MeV

of configuration cells

19.742.976

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Radiation Specifications⁽¹⁾

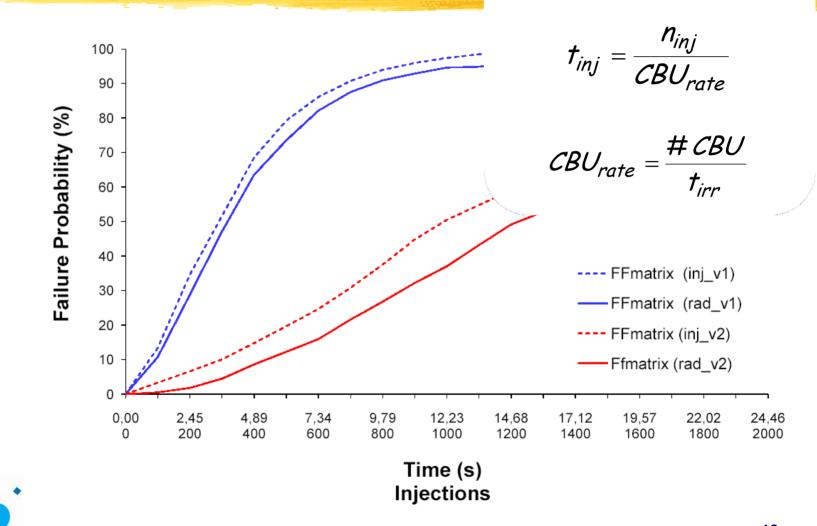
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Table 3: Minimum Radiation Tolerances

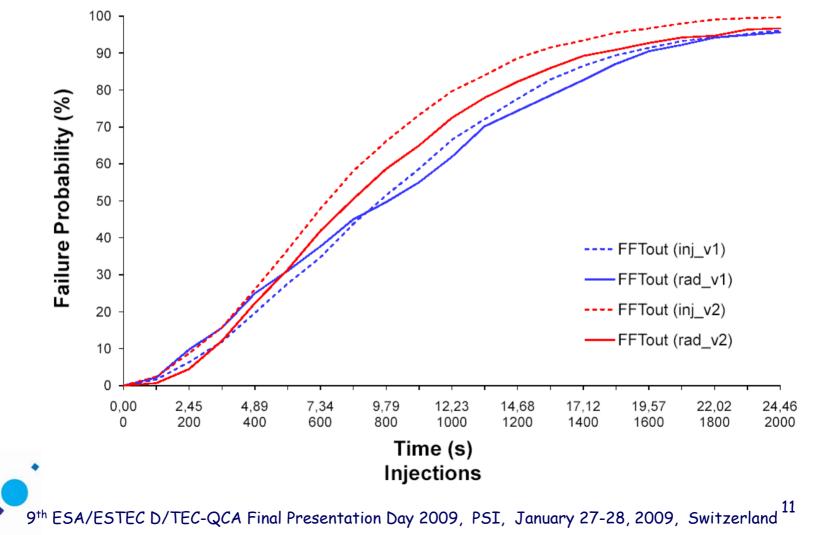
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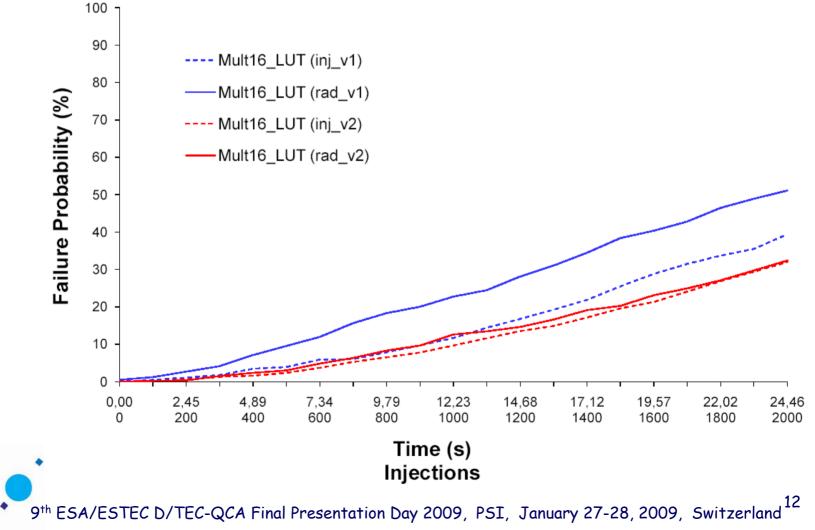
Time-injections correlation





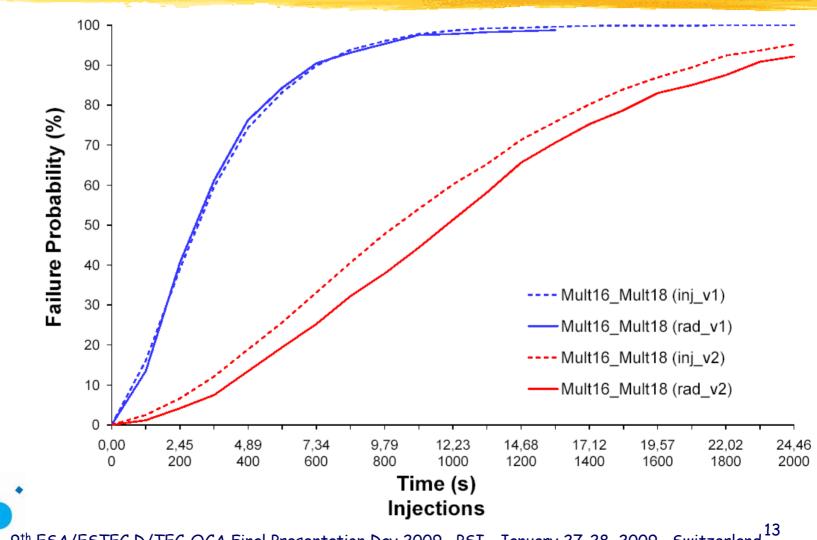


Mult16_LUT

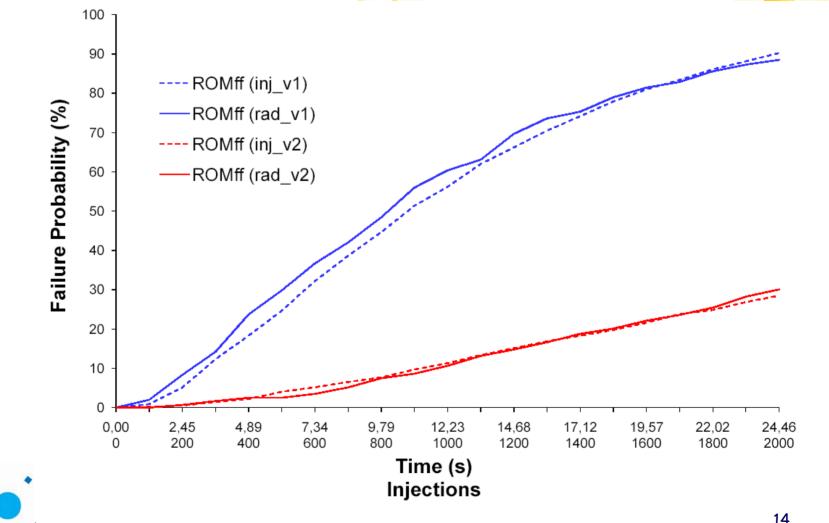


Mult16_Mult18

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- Good agreement between injection and irradiation data
- Suitability of the fault model
- FLIPPER can be effectively used to predict proton data
- Tests of further protection techniques (developed by Politecnico di Torino) are being planned

Alderighi, M., Casini, F., D'Angelo, S., Mancini, M., Pastore, S., Sterpone, L., Violante, M. Soft errors in SRAM-based FPGAs: a comparison of two complementary approaches. IEEE Transactions on Nuclear Science, vol. 55, n. 4, pp. 2267-2273 (2008) Alderighi, M., Casini, F., Citterio, M., D'Angelo, S., Mancini, M., Pastore, S., Sechi, G.R., Sorrenti, G., "Using FLIPPER to Predict Proton Irradiation Results for VIRTEX 2 Devices: a Case Study", Accepted for publication, IEEE TNS, 2009

Thank you!

