SEE and TID Radiation Test Results on ST Circuits in 65nm CMOS Technologies

Final Presentation of ESTEC Contract 2006-2007
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D/TEC-QCA
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Headline

- **Description of the circuits tested during the project**
  - ST 65nm BULK CMOS technology at a glance
  - overview of the 5 Device-Under-Test
    - reference circuits for process/library qualifications and radiation studies
    - ~ 46 Mb SRAMs overall
    - ~ 1 M Flip-flops overall

- **Test plan performed during 7 months over 2006-2007**
  - Highlight for main parameters
    - ~600 test runs performed overall

- **Main test results for Single Event Effects (SEE)**
  - verifications for latchup and hard fail immunities
  - counting for multiple cell and bit upsets
  - R&D digression on a 16Mb prototype SRAM in SOI 65nm
  - measurements of heavy ion and proton cross-sections for BULK 65nm SRAMs and FFs
  - impacts of VDD, high temp. and test facility on the SEU cross-sections

- **Main test results for Total Ionizing Dose (TID)**
  - evidences of gamma immunity at 100 krad

- **Conclusion & Perspectives 2009**

65nm Technology Platform

65nm CMOS Core Process

Dual / Triple Gate Oxides
Dual / Triple Threshold Voltages for MOS Transistors
7-9 Full Copper Dual Damascene Interconnect Levels
0.20µm metallization pitch
Low K

ANALOG

RFCMOS

eDRAM
0.14 µm2

HDSRAM
0.525 µm²

General offer
High current 0.62µm² SVT & HVT
Dual port 0.97µm² SVT & HVT

Power reduction
in activity →Lower VDD
In Standby → lowest leakage

Increase speed
→ Highest cell current

Ultra Low Power
SP 0.56µm² SVT & HVT
SP 0.67µm² HVT

High Performance
High current 0.62µm²
Dual Port 0.97µm²

Representative SRAMs tested during this project

65nm: Technology benefit Summary

Technology	90 LP Hvt	90 LP Svt	90 GP Hvt	90 GP Svt	65 LP Hvt	65 LP Svt	65 LP Lvt	65 GP Hvt	65 GP Svt	65 GP Lvt
Relative speed (Realistic design critical path: delay wc, ns)	12.2	8.0	8.8	6.0	12.6	8.0	6.6	6.9	5.1	4.02
Leakage - 25C (mA/MGates)	0.12	3.5	8.3	81	0.07	1.9	35	35	269	1996
Leakage – 125C (mA/MGates)	6.1	77	115	653	2.6	47	338	268	1671	5772
Dynamic Pwr (ND2, nW/MHz)	9.1	9.3	7.4	6.5	5.6	5.7	6.1	3.9	5.1	5.5

+20% speed (+50% with GP-LVT)

2X reduction

2.6X reduction

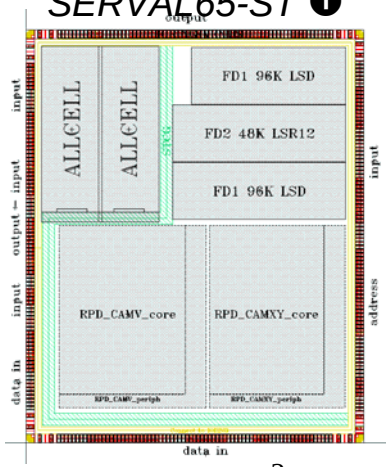
40 to 50% reduction

- **Moving from 90nm to 65nm brings**
  - 50% area reduction for logic and SRAM
  - up to 20% speed performance improvement; extra 25% speed with GP-LVT
  - up to 50% dynamic power reduction
  - up to 2x leakage reduction at same speed @ 25C, > 2.5x @ 125C
- **65nm design platform qualified since May 2007**
- **65nm mass production at ST Crolles 12” (300mm wafers) plant since Mid 2008**
  - second source 12” qualified in Taiwan

Overview of tested testchips in 65nm

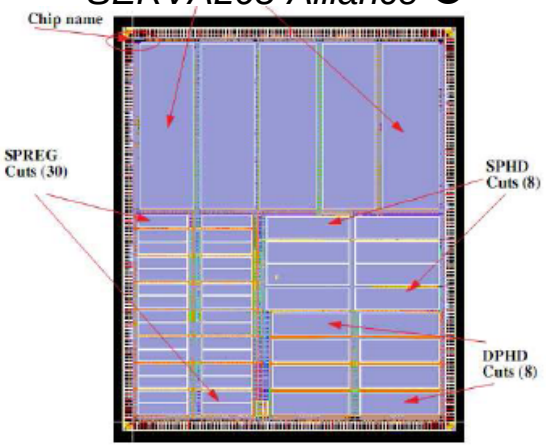
- **4 testchips in ST BULK CMOS 65nm embedding SRAMs and shift registers (FFs)**
  - Testchips for Soft Error Rate characterizations of libraries ❶ + ❷
  - Testchip for validation of rad-hard terrestrial UHD SRAM ❸
  - Reference circuit for libraries validation and qualification and PROcess MOnitoring in the time ❹
    - SRAMs, ROMs, standard cells, via chains (back-end stress), ring oscillators (speed meas.), dividers (delay path meas.), IOs, Fuse : 75 M transistors

SERVAL65-ST ❶



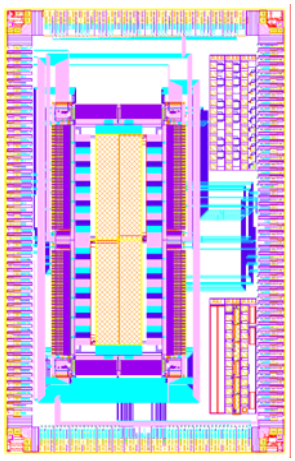
~ 21 mm²

SERVAL65-Alliance ❷



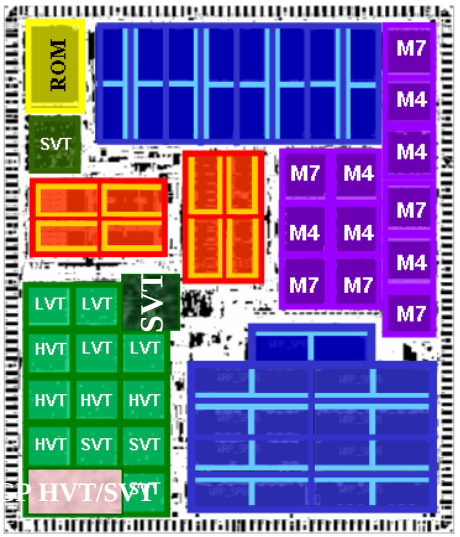
~ 21 mm²

RPD11-14 ❸



~ 21 mm²

PROMO ❹



~ 25 mm² / 75 MT

- **1 SRAM prototype 16Mb in SOI 65nm**
  - not commercially available
  - SOI usage limited at ST so far to specific (RF/mobile) products
- **all testchips pre-characterized by ST with alphas and atmospheric neutrons (terrestrial)**
  - all test set-ups developed by ST and kindly reused for this contract at no cost

Testchip overall contents

- **A total of 46.5 Mbits of SRAMs and ~1 M of Flip-flops tested with space radiations**
- 4 SRAM areas : 0.52µ2, 0.62µ2, 0.67µ2, 0.98µ2
- 2 SRAM architectures : SP (single port) and DP (dual port)
- 2 technologies : BULK and SOI
- 2 Threshold Voltages : Standard and High VT (ultra low power)
- 6 flip-flop types from production libraries
- 1 SRAM covered by 2 eDRAMs (hardened against atmospheric neutrons not space radiations)

Testchip name	Techno option	Macrocell	Device area	Deep-N-Well	Size
SERVAL ST	CMOS065LP	SRAM	0.67µm² (HVT/SVT)	no	2Mb
		SRAM	0.67µm² (HVT/HVT)	no	2Mb
		SRAM	0.62µm² (logic Vt)	no	2Mb
		SRAM	0.62µm² (HVT/HVT)	no	2Mb
		shift-register	FF1 (ref plain FF)	no	96K
PROMO		SPHS	0.525µm²	no	8.5Mb
		DPHD	0.98µm²	no	1Mb
RPD11-14		SRAM	0.525µm²	yes	4Mb
SERVAL65		DPHD	0.98µm²	both	1Mb
		SPHS	0.525µm²	both	2Mb
		SPREG	0.62µm²	both	2Mb
		shift-register	FF1 (ref plain FF, X4, 13T)	both	199K
		shift-register	FF2 (plain, X35)	both	159K
		shift-register	FF3 (plain, X4, 9T)	both	194K
		shift-register	FF4 (clear, x4, 13T)	both	194x2K

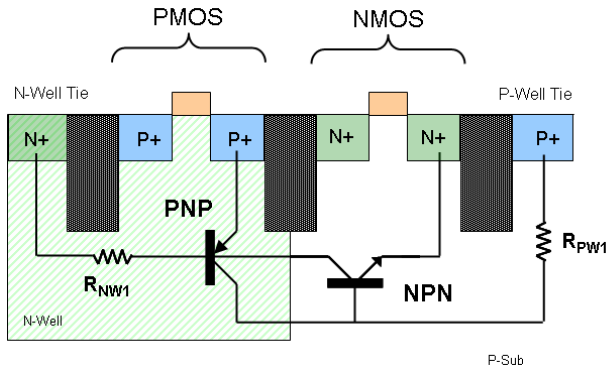
ROBUST

Testchip name	Techno option	Generator	Bitcell area	Deep-N-Well	Size
Rpd11-14	CMOS065 LP	SRAM	0.525µm²	yes	4Mb
SOI6516Mb	SOI65 HP	FSL	0.64µm²	na	16Mb

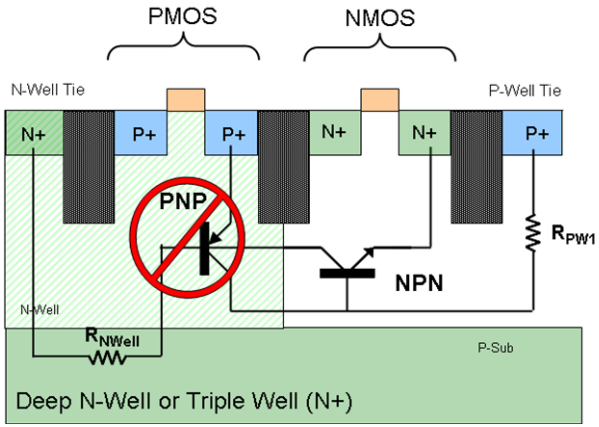
Reminders about ST Deep-NWell (DNW) layer and rad-hard rSRAM™

- **DNW is reversed-biased N+ buried layer qualified as a standard process option**
  - Noise reduction from the substrate
  - P-Well electrical isolation for power reduction in SRAMs

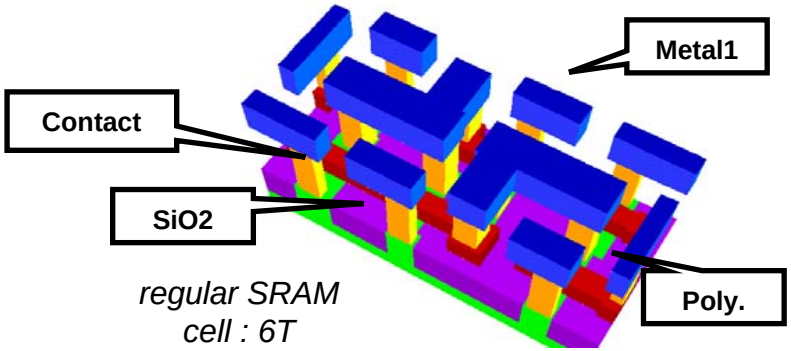
- **DNW efficiency to annihilate SEL proven in ST 90nm at VDD+40% and 125 °C**
  - ST papers at NSREC'07, RADECS'06'07 and ESA QCA days 2007



Deep-NWell added beneath CMOS inverter

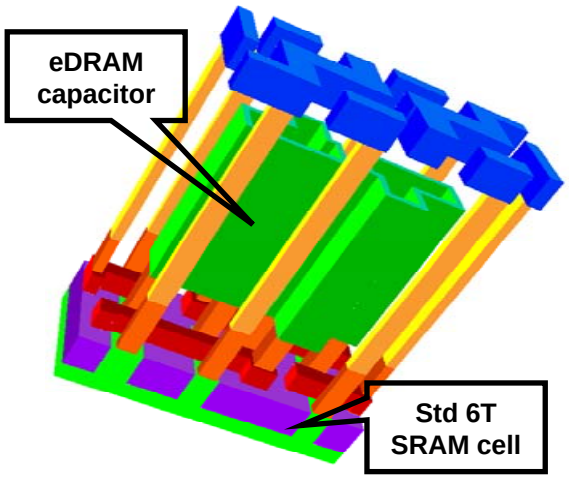


- **ST rSRAM™ is a standard SRAM cell covered by 2 eDRAM caps**
  - no area penalty while maximizing critical charge
  - used in ~70% of all pacemakers and defibrillators from 2010



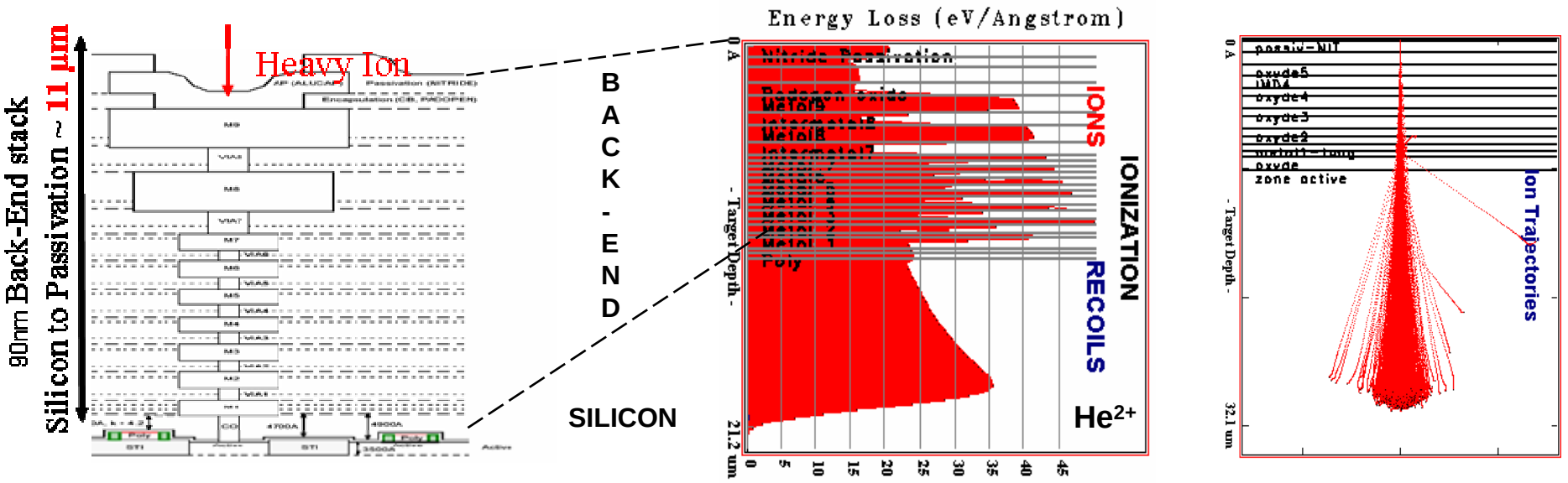
regular SRAM cell : 6T

rSRAM cell : 6T+2C$_{DRAM}$

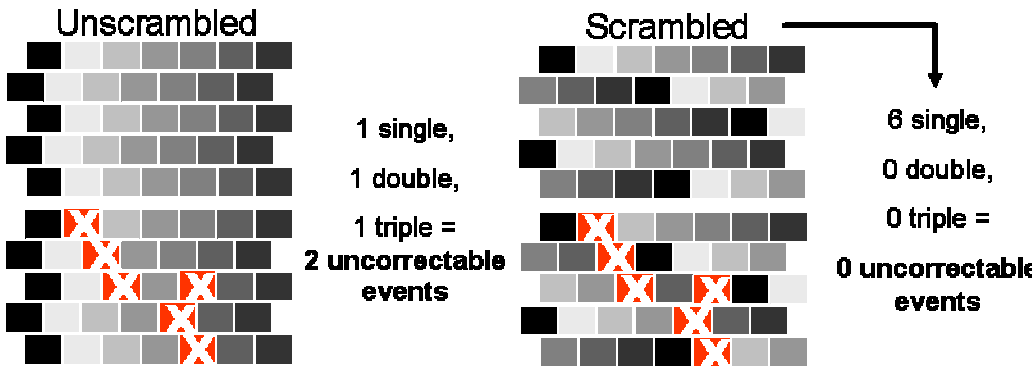


Comments on ion penetration depth and Multiple Upsets

- **Simulations were run to verify that lowest experimental ion-LET can cross through the BEOL**
  - SRIM modeling of 7 thin + 2 thick metal layers + Inter-Metal Dielectrics (SiO2)



- **Multiple Cell Upsets (MCU) are not Multiple Bit Upsets (MBU)**
  - MCU: an event that induces several <u>adjacent bits</u> to fail at one time.
  - MBU: MCU in which two or more bits are involved in the <u>same logic word</u>
  - Scrambling in SRAMs avoids that MCUs become MBUs



Effective test plan

- **4 test campaigns (~1 week each) carried out**
  - at RADEF, UCL, ESTEC and PSI
  - From Dec-2006 to June 2007
- **Extensive Design-of-Experiment:**
  - **Pattern**
    - CKB, SOLID 0 and 1
  - **Power supply**
    - VDD, -20%, + 20%
  - **Temperature**
    - 27 and 125degC
  - **Static and Dynamic algorithms**
    - Dynamic for MCU counting
  - **Current monitoring** on every power domains for TID tests
- **2 samples tested per circuit**
  - 1 spare in case of discrepancy
- **8×2 ion-LET and 4 proton energies**
- **A total of 593 different test runs !**

Device	Pattern	Power supply	Temp.	Algorithm	# of runs
Dec-2006 : UCL Effective Design of Experiment					
SERVAL-AC2	All0 + All1 + CKB	Nom. + Vmax	RT	Dynamic	60 runs
PROMO	All0 + All1 + CKB	Nom. + Vmax	RT	Dynamic	48 runs
SOI 16Mb	CKB	Nom.	RT	Nom.	18 runs
SERVALST	All0 + All1 + CKB	Nom. + Vmax	RT	Dynamic	58 runs
RPD11-14	All0 + All1 + CKB	Nom. + Vmax	RT	Dynamic	58 runs
Feb-2007 : RADEF Effective Design of Experiment					
SERVAL-AC2	CKB	Nom. + Vmin	RT+ 125°C	Dynamic	80 runs
PROMO					Not tested
SOI 16Mb	CKB	Nom.	RT	Static	22 runs
SERVALST	CKB	Nom.	RT + 125°C	Dynamic	52 runs
RPD11-14	CKB	Nom.	RT + 125°C	Dynamic	58 runs
April 2007 : ESTEC Effective Design of Experiment					
SERVAL-AC2	CKB (+ All0/All1)	Nom.	RT	Static	2 runs
PROMO	CKB (+ All0/All1)			Static	2 runs
SOI 16Mb	CKB	Nom.	RT	Static	1 run
SERVALST	CKB (+ All0/All1)	Nom.	RT	Static	2 runs
RPD11-14	CKB (+ All0/All1)	Nom.	RT	Static	2 runs
June 2007 : PIF Effective Design of Experiment					
SERVAL-AC2	CKB	Nom.	RT	Dynamic	42 runs
PROMO					Not tested
SOI 16Mb	CKB	Nom.	RT	Static	28 runs
SERVALST					Not tested
RPD11-14	CKB + ALL0/125°C + ALL1/125°C	Nom. + Vmax /125°C	RT + 125°C	Dynamic	60 runs

Test results for investigations on latchup and hard fail

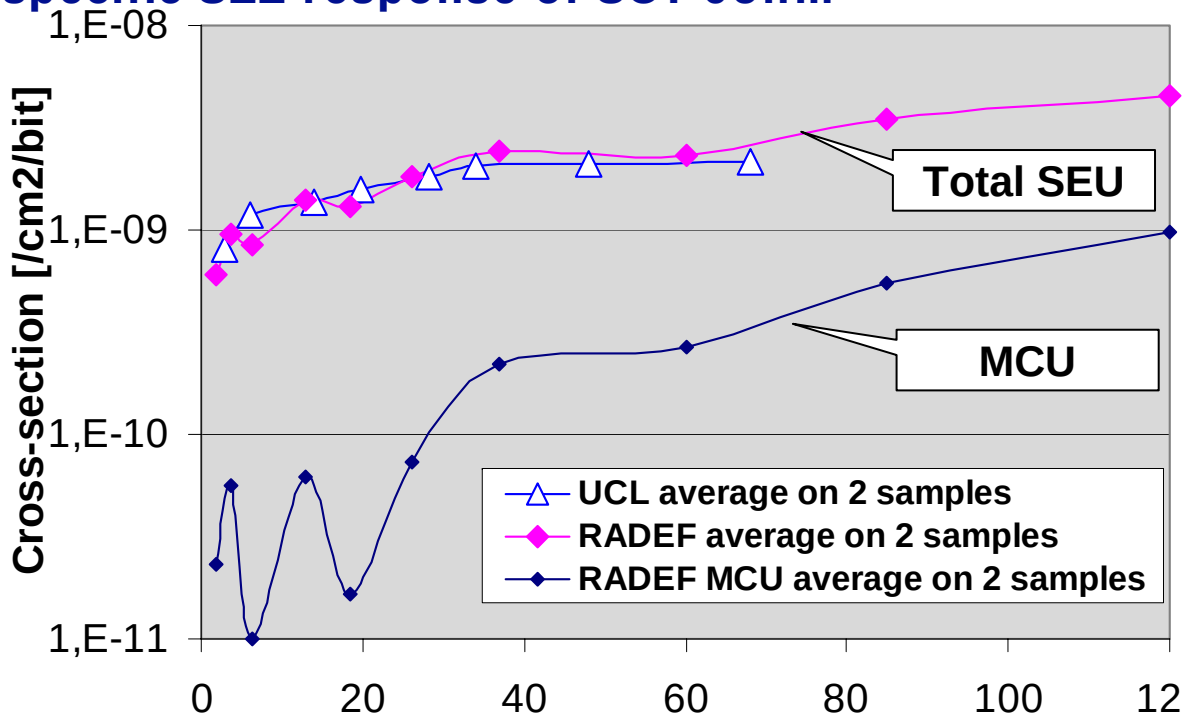
- **Rare latchup events were measured at high LET on Ultra High Density (UHD) SRAMs not covered by Deep N-Well**
  - High Density inverters are intrinsically more prone to latchup

- **No Latchup was ever recorded during irradiations on devices covered by Deep N-Well**
  - verified with heavy ions and protons,
  - up to 120 MeV/mg.cm2 and VDD + 40% and 125 degC

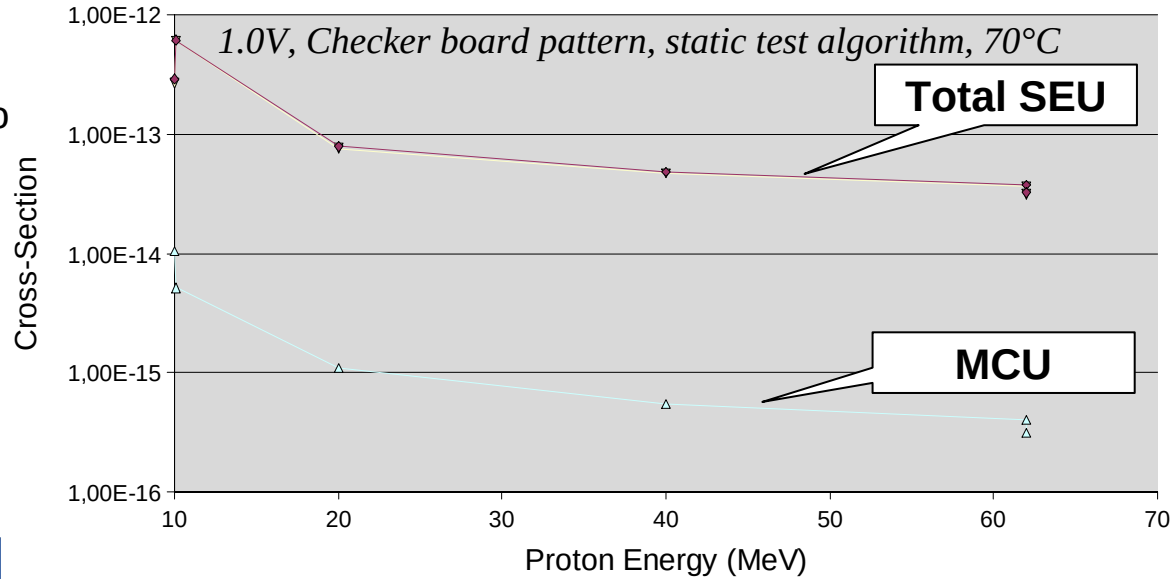
- **No hard fail nor permanent damage were ever recorded during all tests**
  - on circuits in ST CMOS 130nm, 90nm, 65nm
    - immunity also verified in 45nm (with 1-800MeV neutrons)
  - with heavy ions and protons
  - LET up to 120 MeV/mg.cm2
  - proton energy up to 60 MeV
  - VDD up to nominal + 40%
  - temperature up to 125degC

R&D digressions : the specific SEE response of SOI 65nm

- **Test results with heavy ions :**
  - Low SEU cross-section ~ 2.10^{-9} /cm2.bit
  - Very low MCU cross-section < 5.10^{-10} /cm2.bit
  - Very good agreement between UCL and RADEF

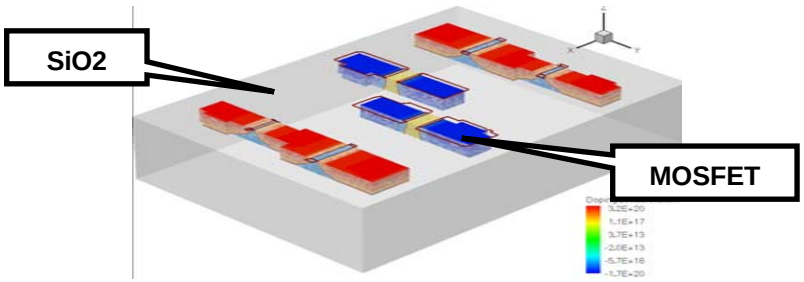


- **Test results with protons :**
  - Low SEU cross-section ~6.10^{-14} cm2.bit
  - Higher sensitivity at low energies due to the SOI technology itself
    - not a test artifact
    - also reported by R.A.Reed, in IEEE TNS Dec. 2002
  - Very low MCU cross-section <10^{-15} /cm2.bit

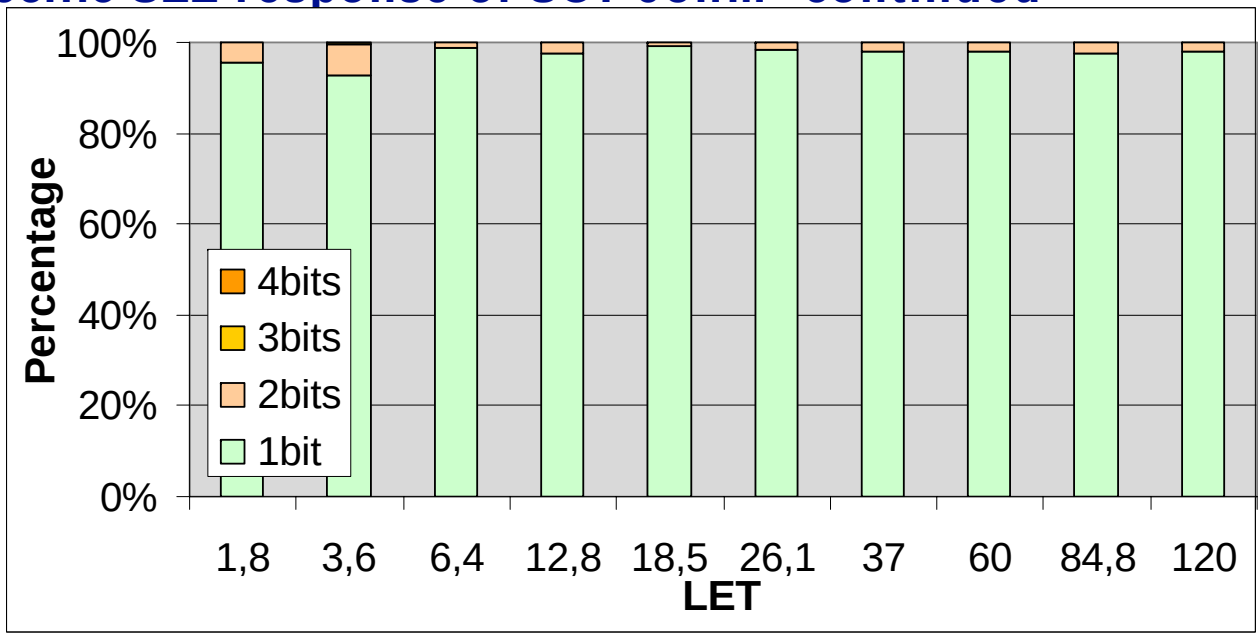


R&D digressions : the specific SEE response of SOI 65nm -continued

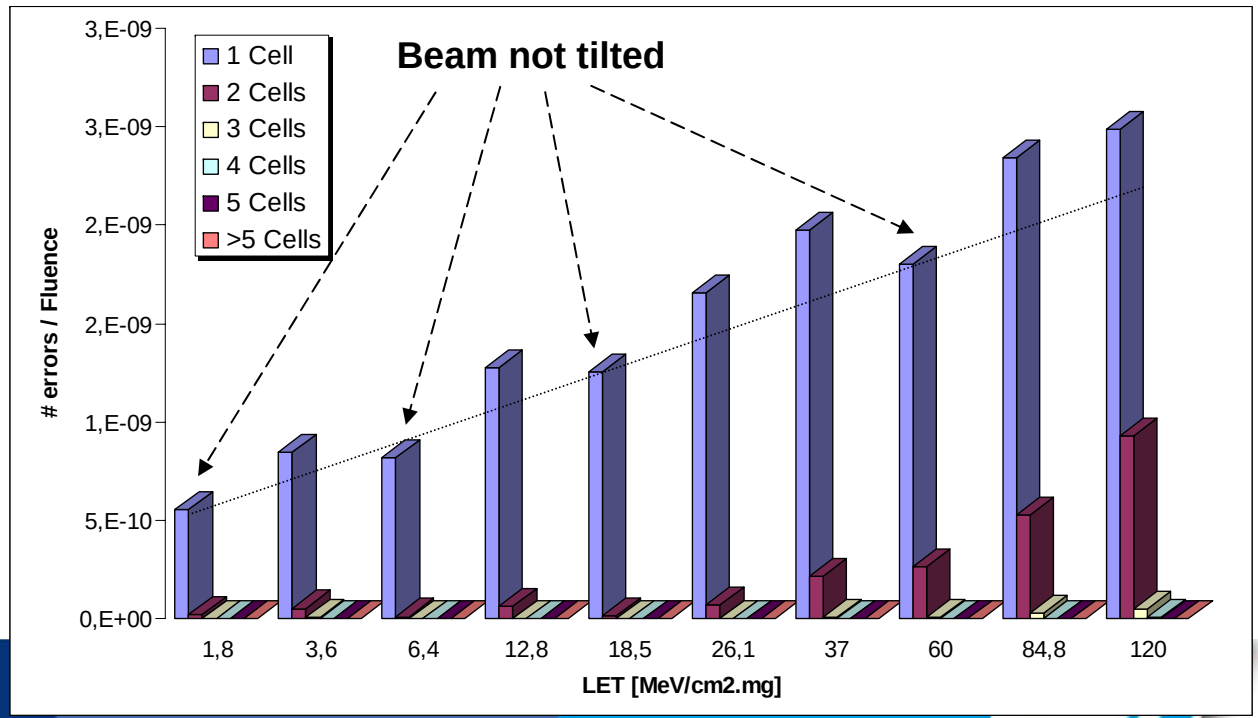
- **Relative percentage of MCU spread for the 16Mb SOI 65nm SRAM as a function of the LET**
  - >95% of errors are SEU
  - SiO2 isolation around MOSFETs



SOI SRAM cell

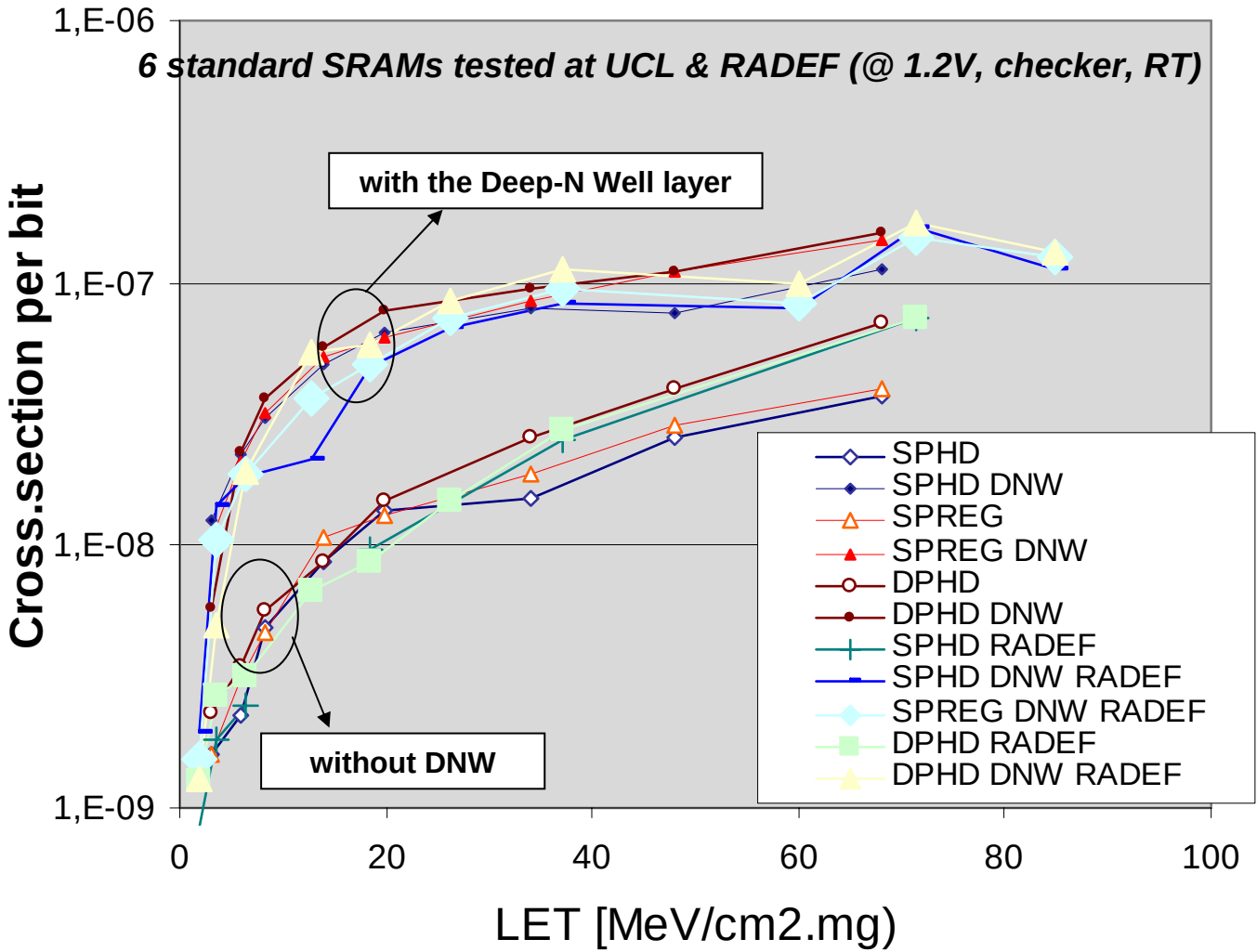


- **Absolute MCU spread for the 16Mb SOI 65nm SRAM as a function of the LET**
  - MCU2 (order 2) mainly
  - MCU3 only at LET 84.8 and 120



Heavy ions test results for commercial 65nm BULK SRAMs

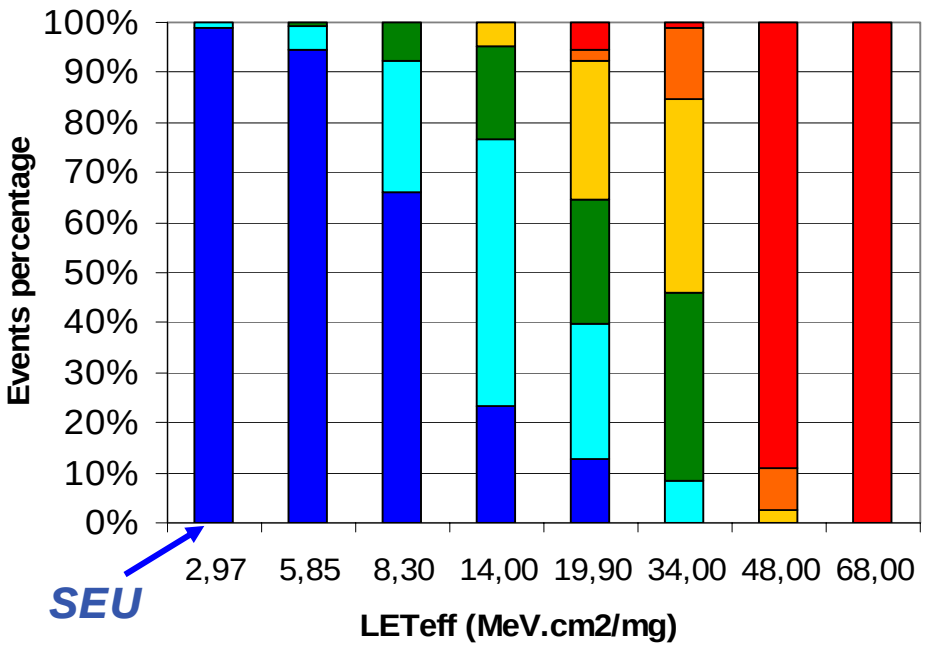
- **Cell area does not significantly impact the error cross-sections**
  - 0.52/0.62/0.64 µ2
- **Cross-sections @LET 60 range from 1^{E}-8 to 2^{E}-7 /cm2.bit**
  - without any mitigation
- **With DNW, zero SEL measured but SEU cross-sections increased**
  - at low LET mainly
- **No more saturation above LET 60 for SEU cross-sections in CMOS 65nm**
  - typical of Ultra Deep Submicron
  - see ST papers at RADECS'06'07



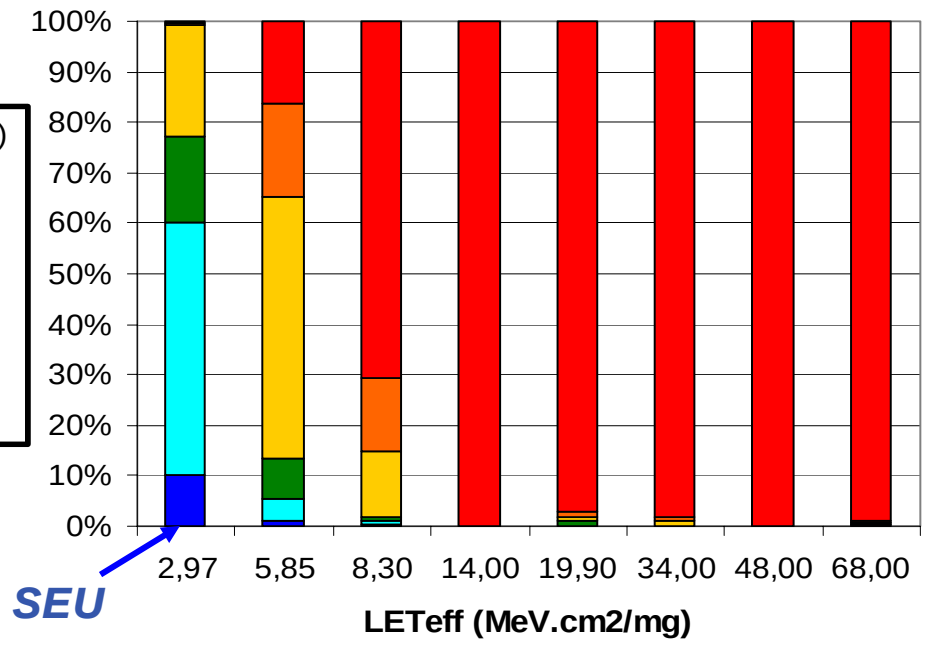
Heavy ions test results for commercial 65nm BULK SRAMs -continued

- **Higher cross-sections with Deep NWell due to a stronger MCU component**
  - MCUs rapidly overcome SEUs (effect maximized with UHD SRAMs)
  - phenomenological cause (parasitic bipolar amplification) in ST papers at NSREC & RADECS 2007

MCU spread in UHD SRAM (Worst Case)

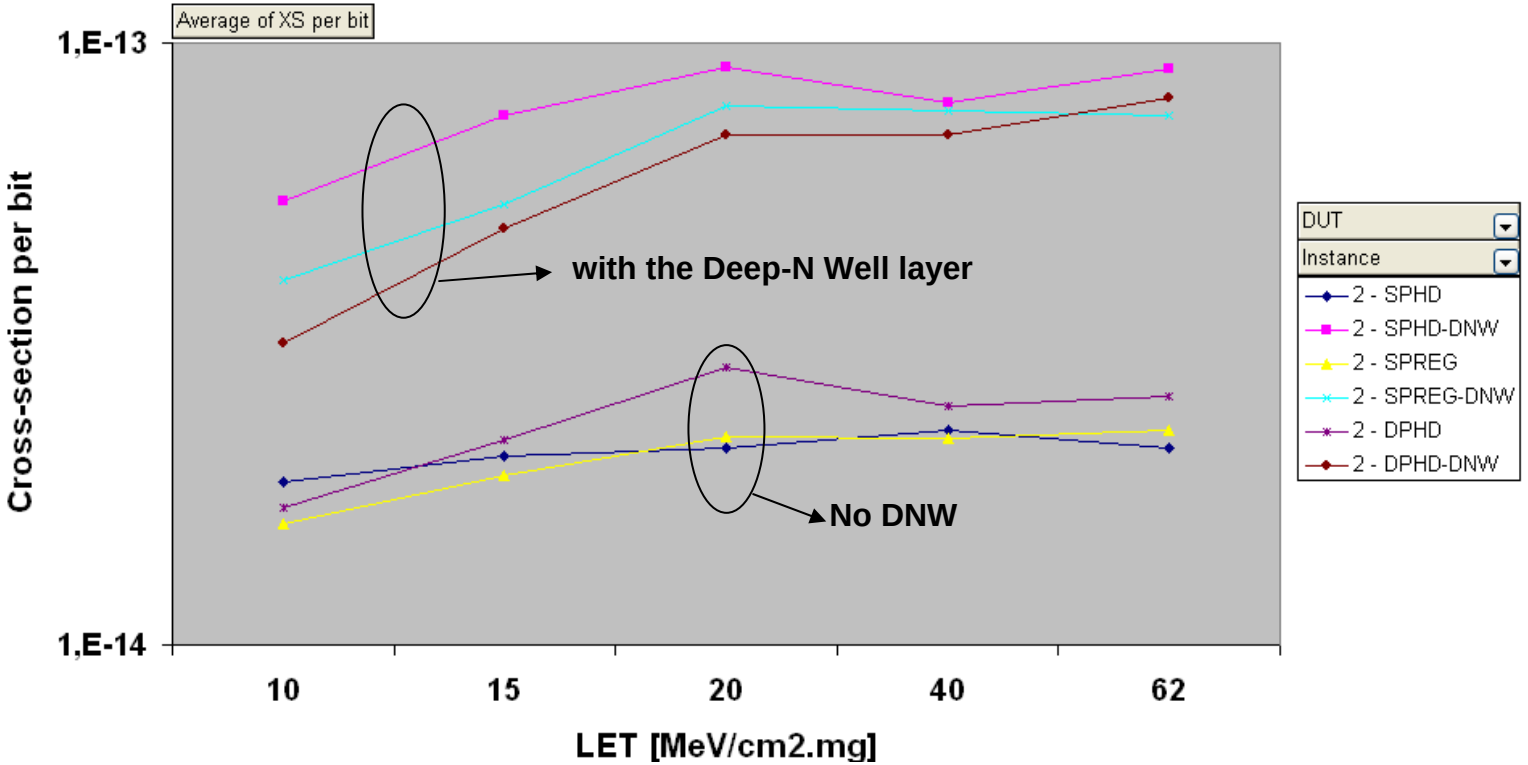


MCU spread in UHD SRAM + DNW



- **No MBU ever recorded with Deep-NWell even for the worst case of UHD SRAMs**
  - With ad-hoc internal multiplexation (scrambling) in ST memory arrays
- **EDAC/ECC can be 100% efficient while ensuring a full latchup immunity**

Proton test results for commercial 65nm BULK SRAMs



- **Proton cross-sections range from 1^{E}-14 and 1^{E}-13 cm2/bit**
  - cell area (0.52/0.62/0.98µ2) does not significantly impact cross-sections

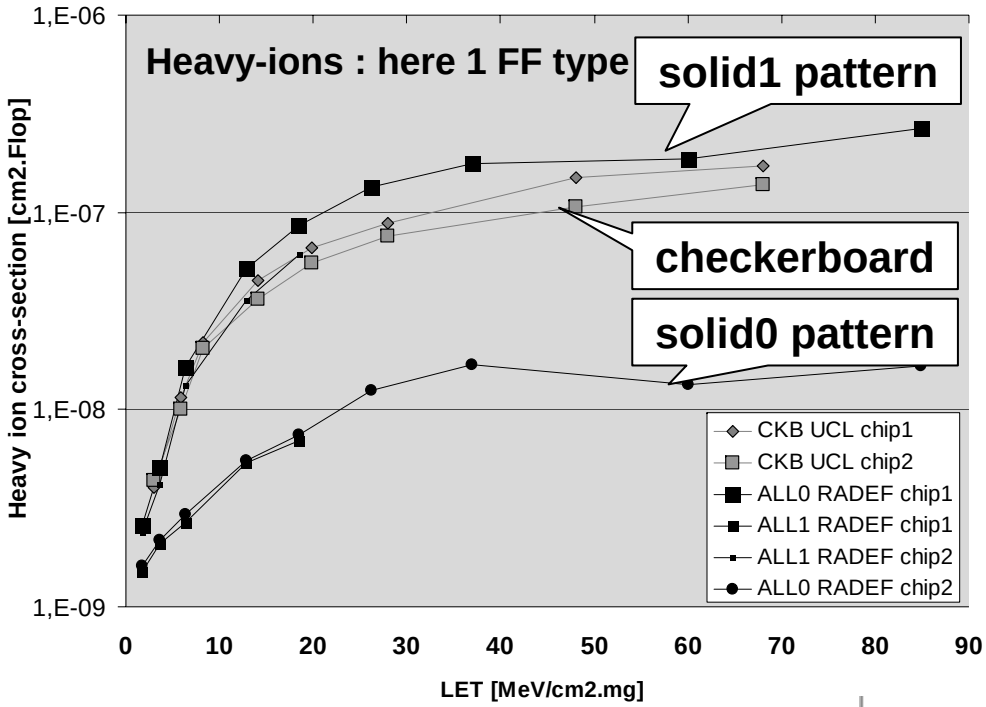
- **Typical Protons SEE rate for a non-hardened 65nm SRAM : 2.56e-8 SEUs/bit/day**
- **Typical Heavy ions SEE rate for a commercial 65nm SRAM : 1.66e-7 SEUs/bit/day**
  - CREME96 with a 2-parameter Bendel and Weibull functions for fitting protons and HI data
  - GEO synchronous orbit, minimum solar activity, 100mils Aluminium shielding, no ageing

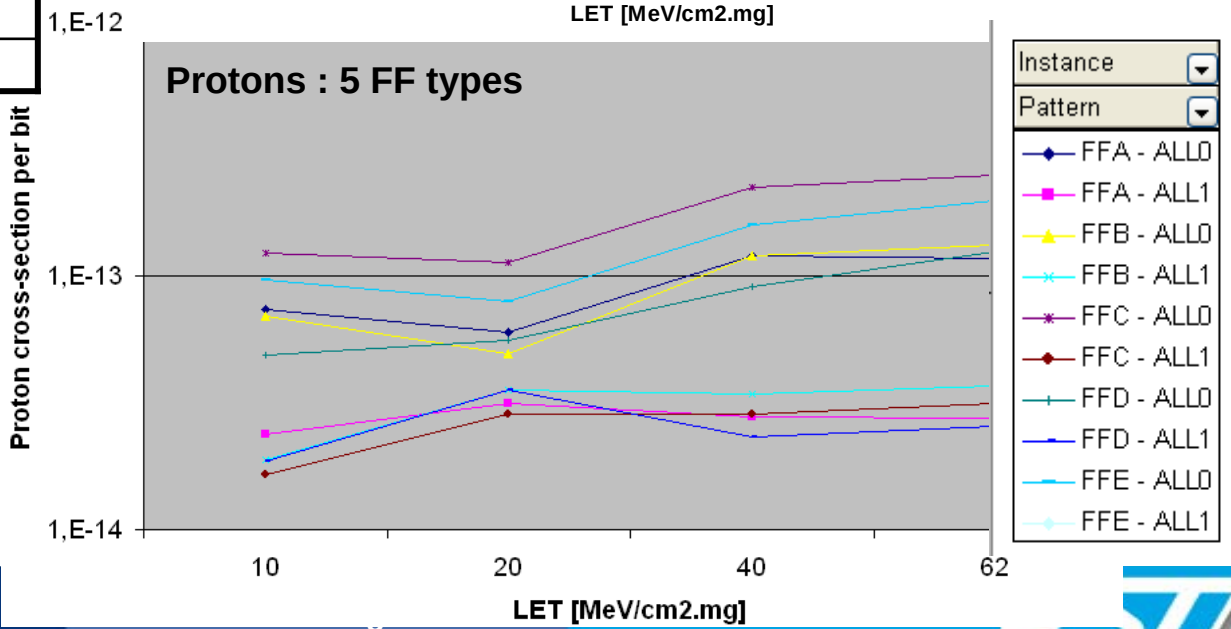
Heavy ions & proton test results for commercial 65nm Flip-flops

- **SEU cross-sections of flip-flops (FF) from production libraries strongly vary**
  - over 1-2 decades
  - with the test patterns
  - VDD and clock
  - FF drive, pitch and design type

	Flip-flops selected for radiation radiations	FIFO size	DNW
FFA	Plain-FF, lowest drive	199 K	yes
FFB	Plain-FF, highest drive	160 K	yes
FFC	Plain-FF, highest drive, HD	194 K	yes
FFD	Clear-FF, lowest drive	133 K	yes
FFE	Plain-FF, lowest drive, HD	194 K	no

- **SEU cross-sections of FF and SRAM are now similar on a per device basis**
  - 1^{E}-8 to 2^{E}-7 with heavy ions
  - 3^{E}-14 to 4^{E}-13 with protons





Impacts of temperature and power supply on SEU cross-sections

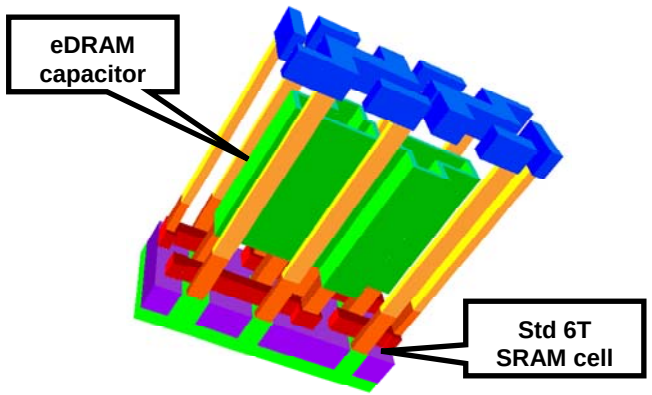
- **The higher the temperature the higher the cross-sections or SEU sensitivity:**

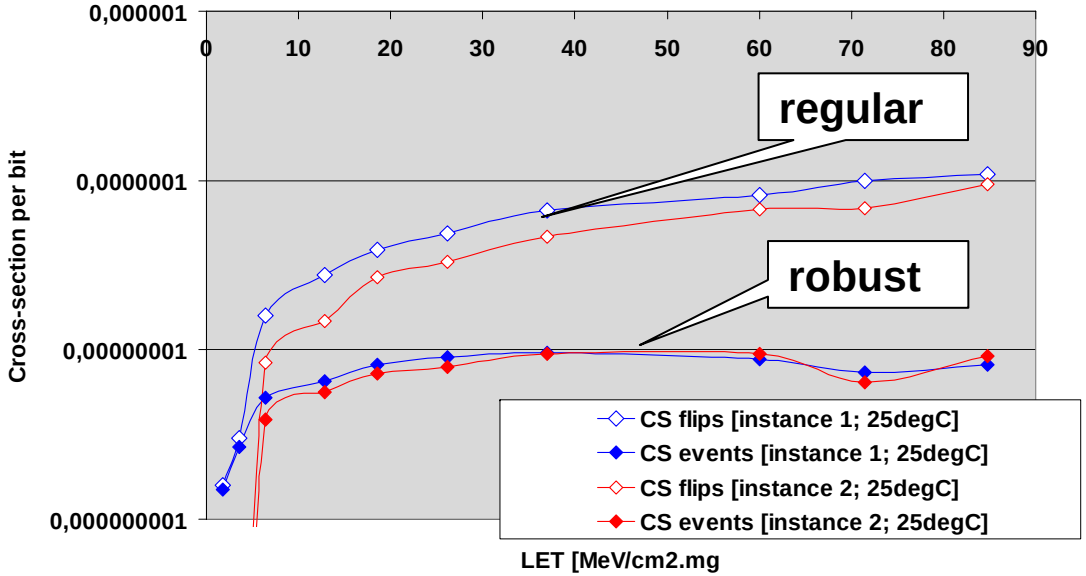
	Highest temperature used for the heavy ion testings	Cross-section increase at “saturation” (LET ~60) between RT and highest temperature
Chip A: SRAM #1 and #2	**+85 °C**	**+37%** and **+42%**
Chip B: SRAM #1 and #2	**+125 °C**	**+30%** and **+42%**
Chip C: SRAM #1 to #6	**+125 °C**	**+52%** on average

- **The higher the LET, the stronger impact of the temperature**
- **The higher the power supply, the slightly lower the asymptotic cross-section**
  - E.g. +13% on the SEU cross-sections when the power supply was reduced by 20%
- **The LET threshold remains unchanged whatever the power supply**
  - at least the variation cannot be experimentally quantified

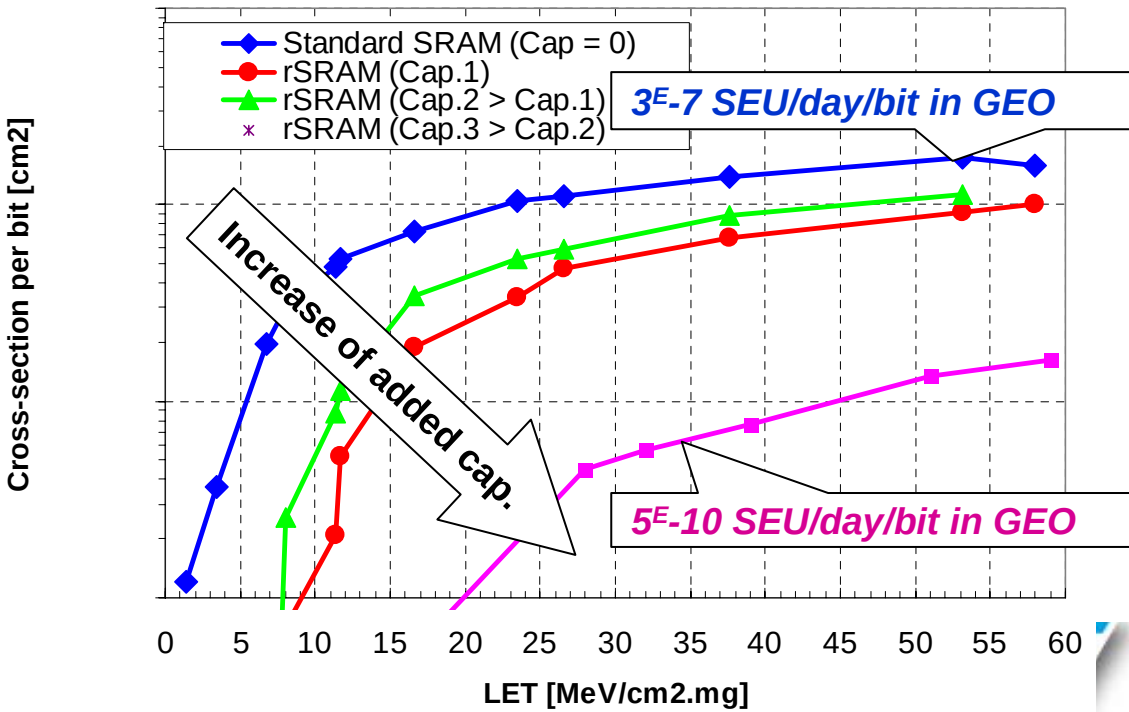
Improvement of SEU cross-sections with the ST neutron-immune UHD rSRAM

- **One decade improvement for the heavy ion cross-sections when using the ST neutron immune UHD SRAM**
  - Embedded SRAM, not standalone
  - Originally designed for consumer products not space

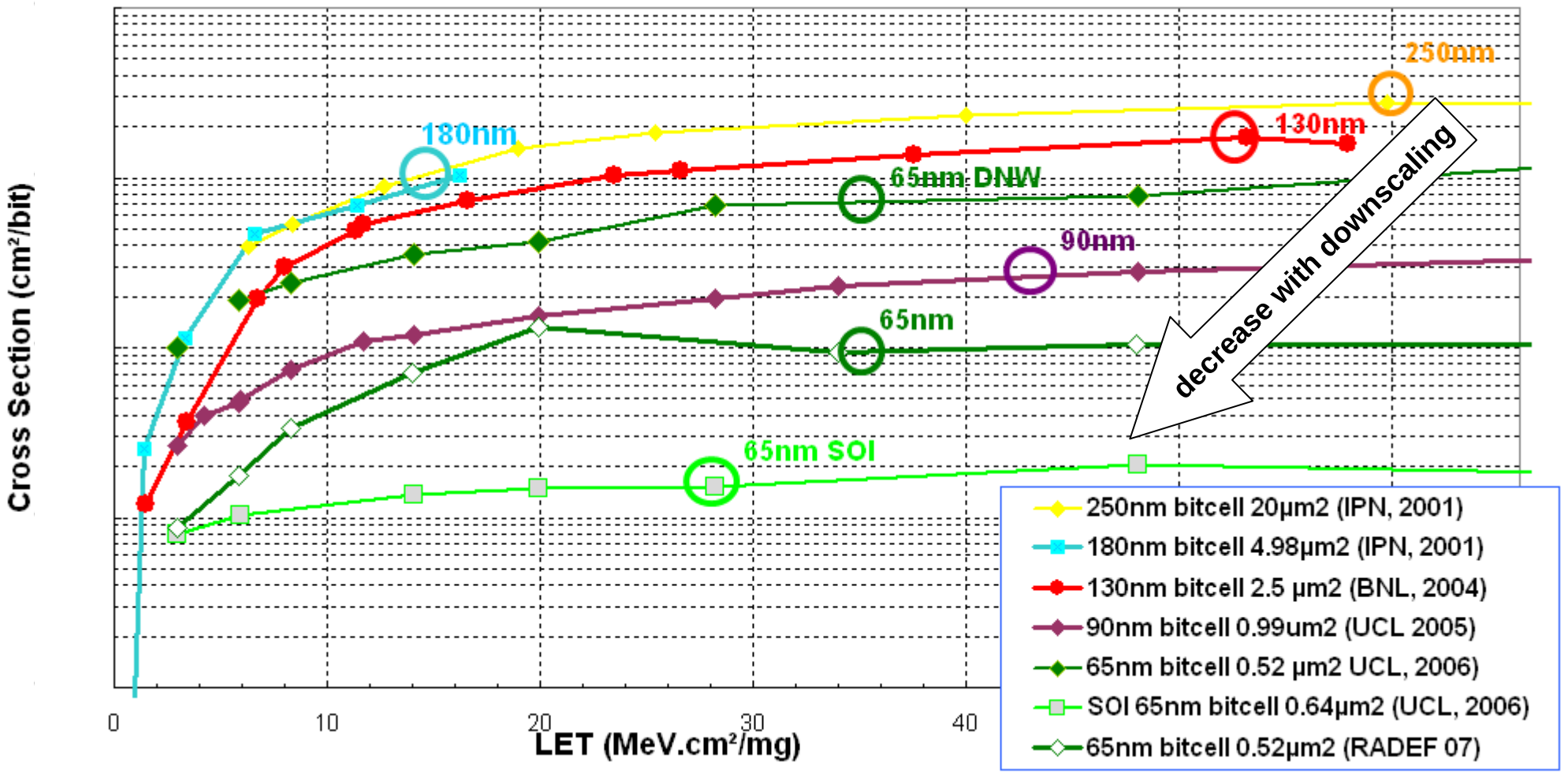




- **Hardening level can be fine tuned with the added eDRAM capacitor value**
  - the higher the added eDRAM capacitor the better the hardening
    - illustrations in 130nm
  - various design trade-offs



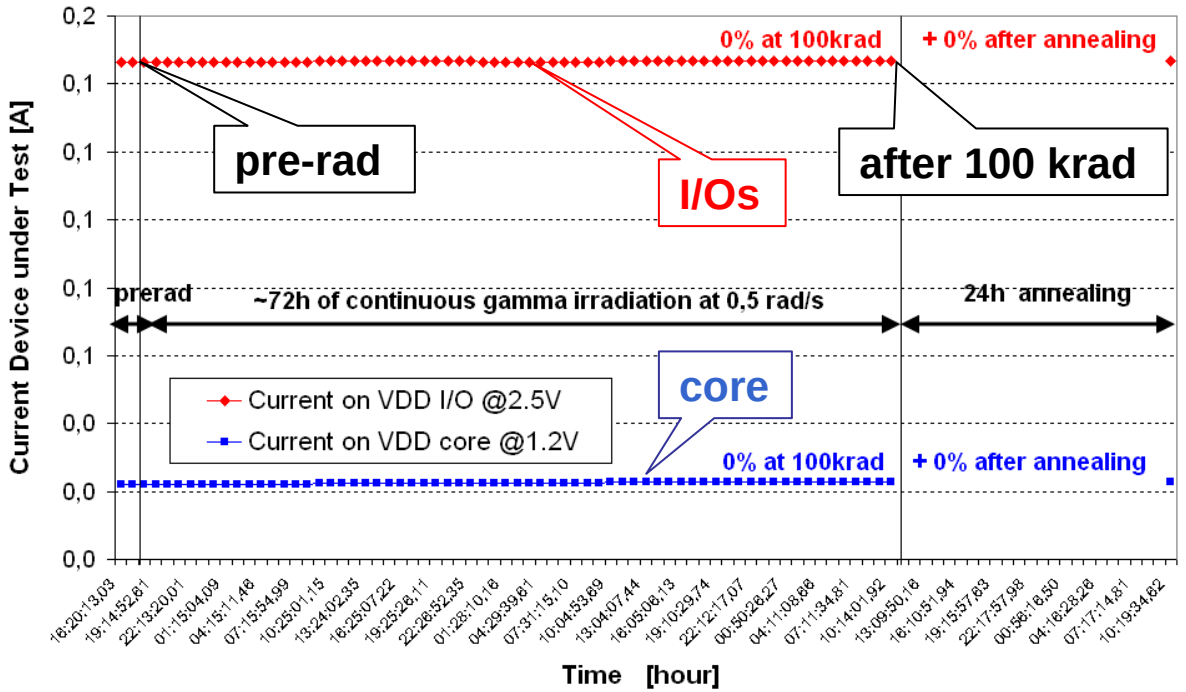
Heavy ions test results for commercial ST SRAMs in CMOS 250 / 180 / 130 / 90 / 65 nm



- **SEU cross-sections intrinsic reduction by 30× from commercial CMOS 250nm down to 65nm**
  - LET threshold unchanged
- **Moving from technology 250nm to 65nm naturally improves by 50× the SEU rate / bit / day**
  - estimations on XS here above with CREME96, GEO, minimum solar activity, 100mils Alu shielding

TID test results in 65nm with the ESA-ESTEC Cobalt 60 source

- **Same TID response measured for four 65nm circuits irradiated up to 100 krad at ESA-ESTEC, Holland**
  - all devices power supplied at nom. VDD
  - all devices with input signals tied to specified values (not floating)
  - topological checkerboard
  - dose rate ~1.875 $krad_{Si}$/h
  - annealing period of 24hours
  - current monitored on all power lines of each board. Sampling every second
    - **210,000 read points**



- **No over consumption at 100 $krad_{Si}$**
  - zero current increase on all power domains

- **100% functionality at 100 kradSi**
  - first order functional parameters unchanged
  - second order functional parameters (Iddq, time, setup/hold timings, …) not accessible for tested circuits

Conclusion

- **5 circuits in 65nm tested with radiations by ESA and ST-Crolles from end 2006 to mid 2007**
  - with heavy ions, protons and gamma rays
  - using ESA certified beam facilities and test methods

- **A total of 340,000 test data collected**
  - ~600 test runs to quantify impacts on SEE of VDD, temp, pattern, clock, facility, algorithm, …

- **High intrinsic radiation hardness measured with heavy ions and protons**
  - no latchup nor hard fail
    - up to 120 MeV/mg.cm-²
  - low SEU cross sections with heavy ions / protons
    - can be further improved using ST rad-hard solutions such as rSRAM™
  - **EDAC/ECC are 100% efficient with appropriate scrambling**

- **Extremely high intrinsic radiation robustness measured with gamma rays**
  - no over-consumption and full chip functionality at 100 krad for every DUTs
  - **no longer need for costly TID mitigation techniques** (such as guard rings, edgeless transistors, local P+ doping implants …)

- **Additional experiments are forecasted over 2009**
  - still in ST 65nm, but extended to 230 MeV protons and 300 krad cumulated over 2 months
  - new ST rad-hard devices : rad-hard Flip-flop libraries in 65nm and medical rSRAM™ in 130nm
  - new ST advanced technologies : 65nm for Non Volatile Memory / 45nm qualified process (32nm)

BACK-UP

65nm Global Core Devices Table

	W=1µm	GP for LP/GP Mix			Low Power			IO HS	IO
		High VT	Std VT	Low VT	High VT	Std VT	Low VT	Analog W=10µm	Analog W=10µm
	Vdd (Volt)	1.0			1.2			1.8	2.5
	Tox (nm)	1.2			1.8			3.1	5.0
	Ldrawn (nm)	60			60			200	280
	Lsilicon (nm)	45 (N) / 48 (P)			57(N) / 60(P)			145	280
NMOS	CET_inv (A)	20.5			26			34	55
NMOS	Ion (µA/µm)	669	830	931	425	610	740	680	580
NMOS	Ioff (nA/µm)	5.1	51	239	0.0066	0.36	5.2	0.02	0.007
NMOS	Vt lin (V)	0.283	0.201	0.152	0.53	0.41	0.34	0.44	0.45
NMOS	Vt Sat (V)	0.189	0.096	0.037	0.43	0.28	0.19	0.33	0.4
NMOS	Jg_on (A/cm²)	<5			<0.016			~0	~0
PMOS	CET_inv (A)	22.5			27.5			37	56
PMOS	Ion (µA/µm)	300	395	458	210	310	386	310	340
PMOS	Ioff (nA/µm)	2.1	36	231	0.0045	0.092	2.4	0.03	0.01
PMOS	Vt lin (V)	0.326	0.241	0.184	0.57	0.47	0.39	0.48	0.39
PMOS	Vt Sat (V)	0.226	0.124	0.047	0.47	0.34	0.24	0.42	0.35
PMOS	Jg_on (A/cm²)	<5			<0.0018			~0	~0
RO	FO1 (ps)	17	10.5	8.5	27	17	13	~15	~35

VT : Threshold Voltage

HS : High Speed

Networking
Multimedia
Printer

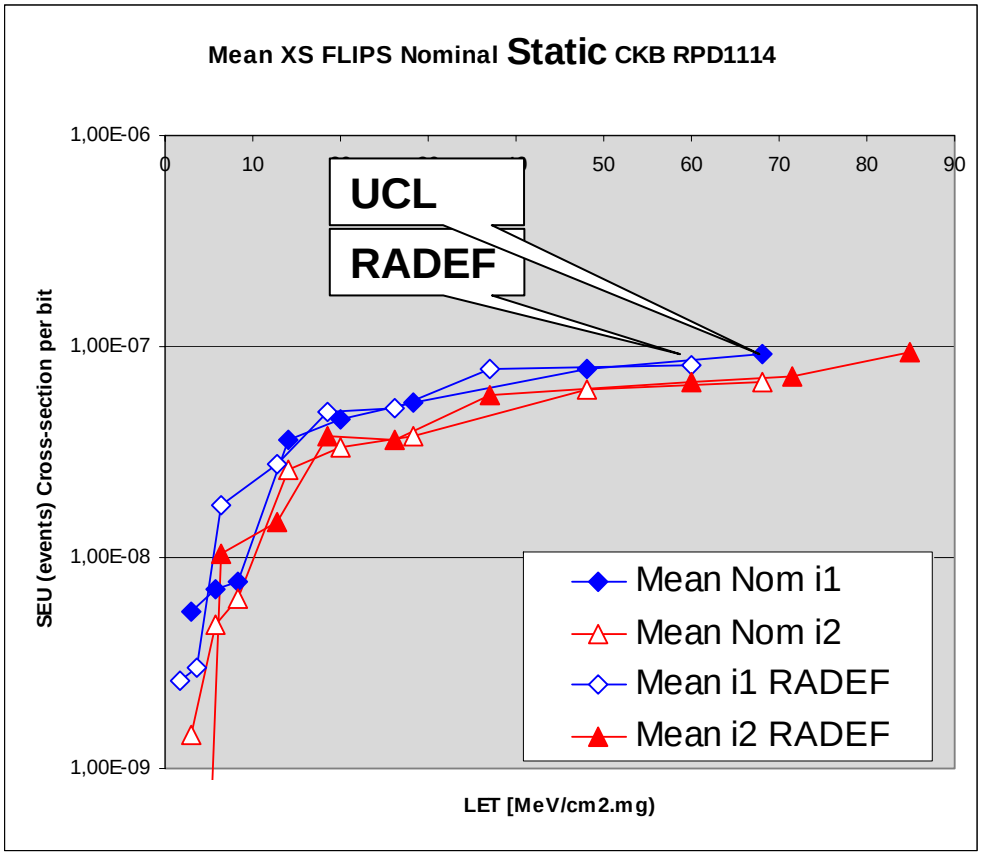
Consumer
Mobile Applications
Printer

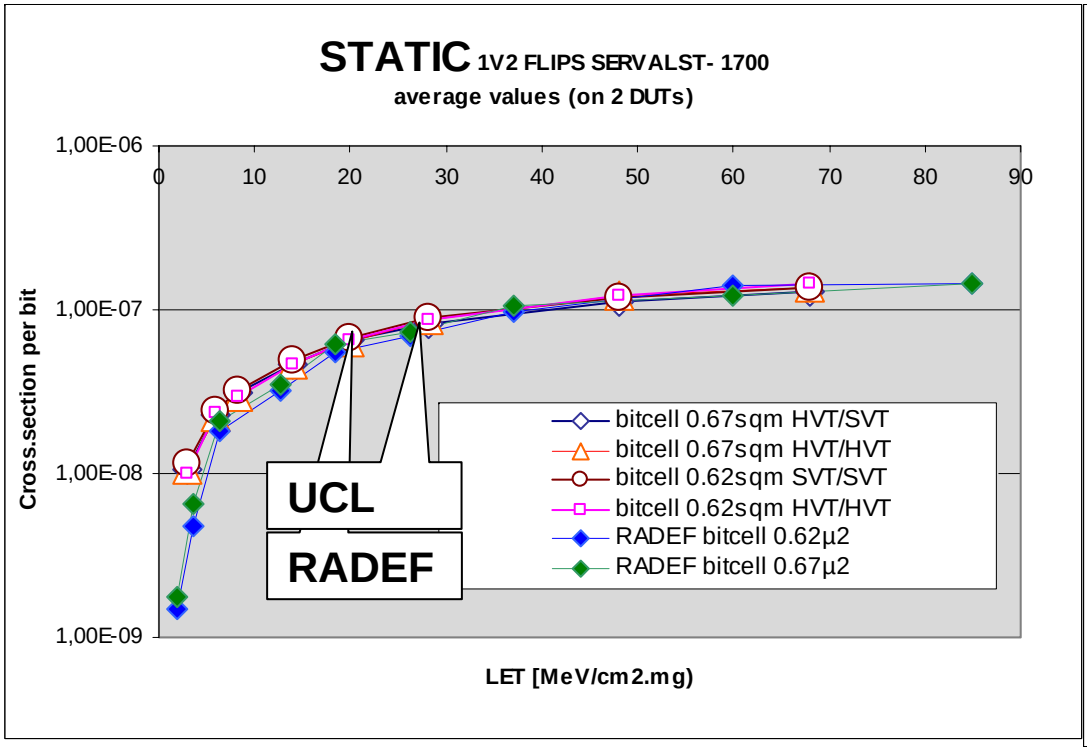
IOs
Analog

Low Power process option characterized during this project

(No) impact of test facility on the measured SEU cross-sections

- **Excellent agreement between RADEF and UCL for every test conditions**
  - whatever the LET
  - within ± 20% at a given LET





(Minor) overall impact of test parameters on SEU cross-sections

Same order of magnitude whatever the test parameters and LET