

# Radiation Characterisation of ST MOSFETs – Overview and Results

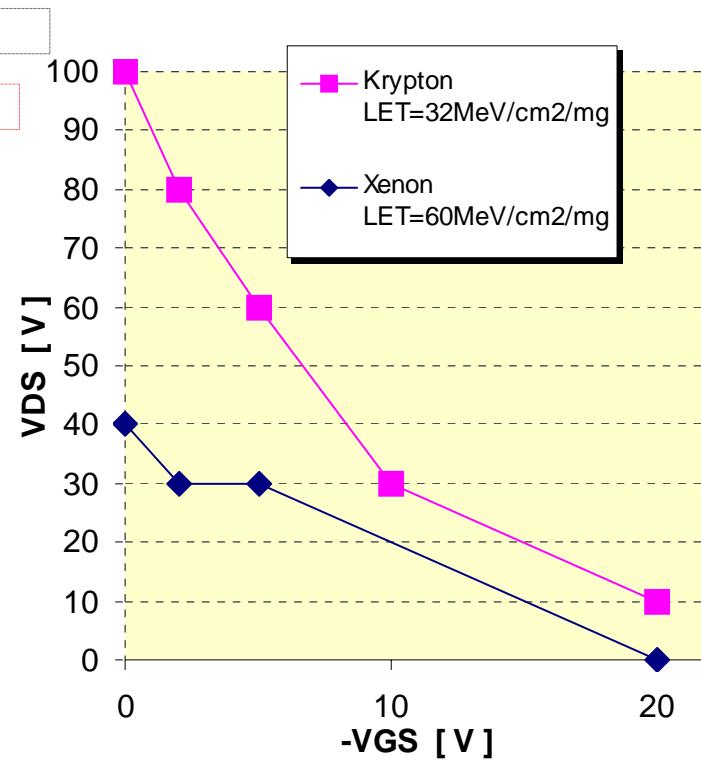
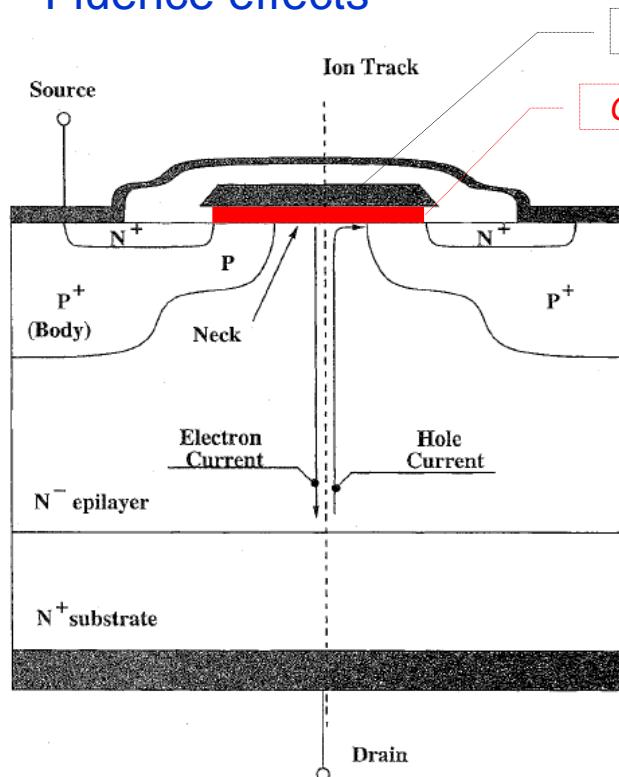
Fredrik Sturesson ESA/ESTEC

Francoise Bezerra, CNES

28<sup>th</sup> of January 2009

# INTRODUCTION

- What is Single Event Gate Rupture in Power MOSFETs
- What can be hidden behind SEGR test data?
  - Latent oxide damage effects
  - Fluence effects

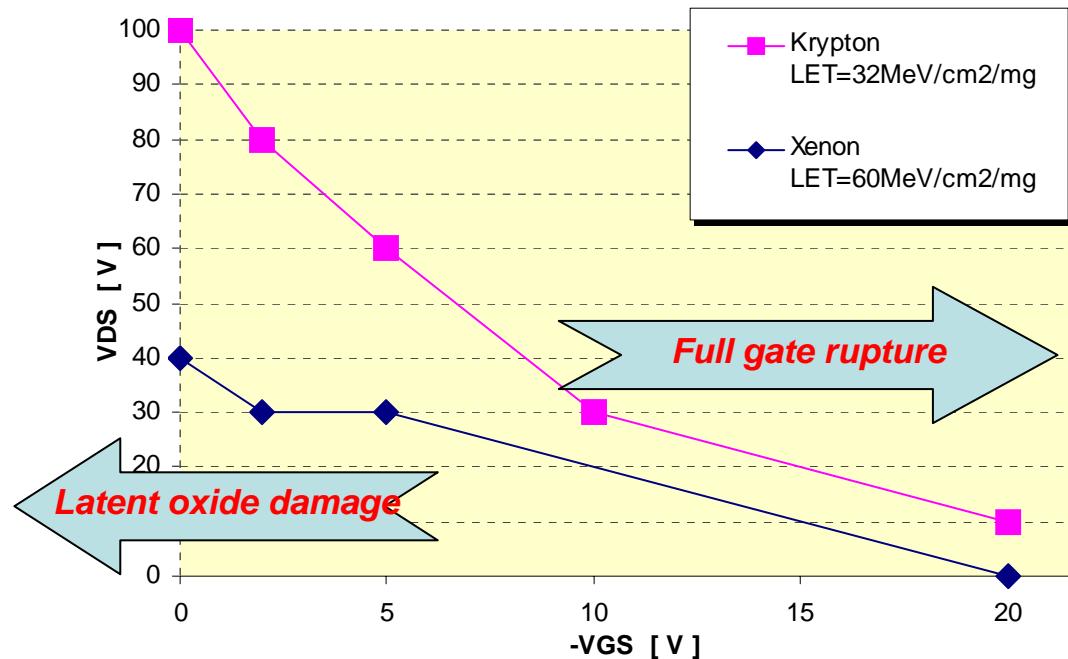


# Safe Operation Area (SOA) Testing

- Test Object
  - Prototype from STM
  - SEB hardened
  - 100V N-channel
- Irradiation
  - RADEF, Jyväskylä, Finland
  - Xenon
    - 1217 MeV
    - Range(Si) = 89um
    - LET(Si) = 60.0 MeV-cm<sup>2</sup>/mg
- Post Irradiation Gate Stress test

# Latent Oxide Damage

- SEGR effects can be divided into two categories
  - Full gate rupture
    - Achieved at high negative Gate voltages
  - Latent oxide damage
    - Achieved at low gate voltages



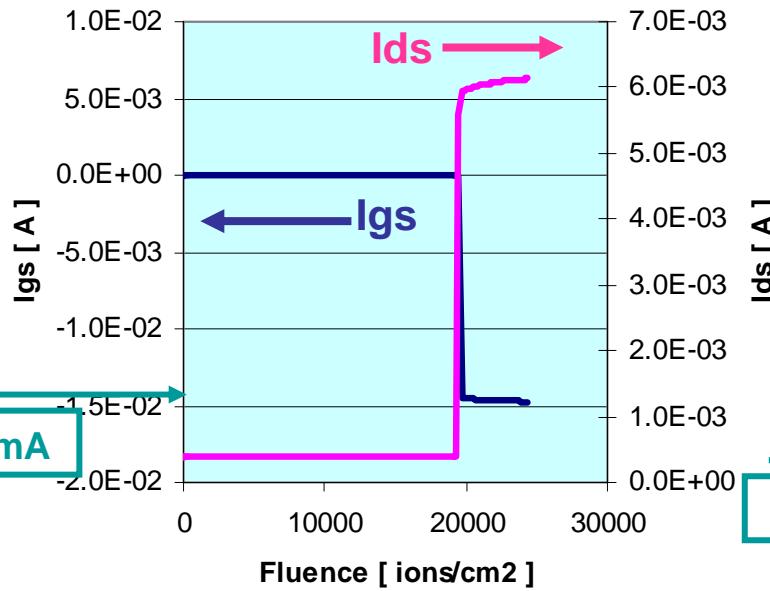
# Latent Oxide Damage

- Example Full gate rupture

- $V_{ds} = 20 \text{ V}$
- $V_{gs} = -20 \text{ V}$

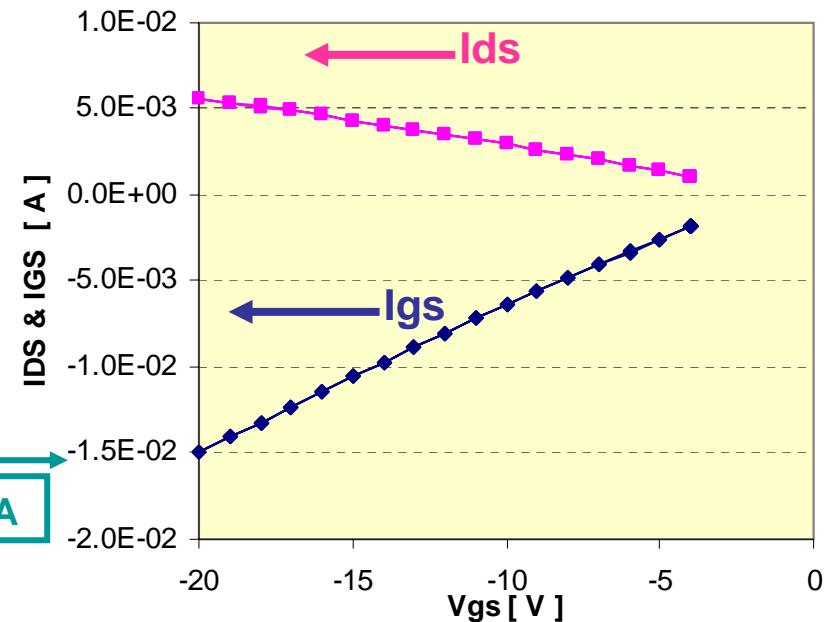
## *During Irradiation*

- Rupture drain & gate



## *After Irradiation*

- Ohmic drain & gate



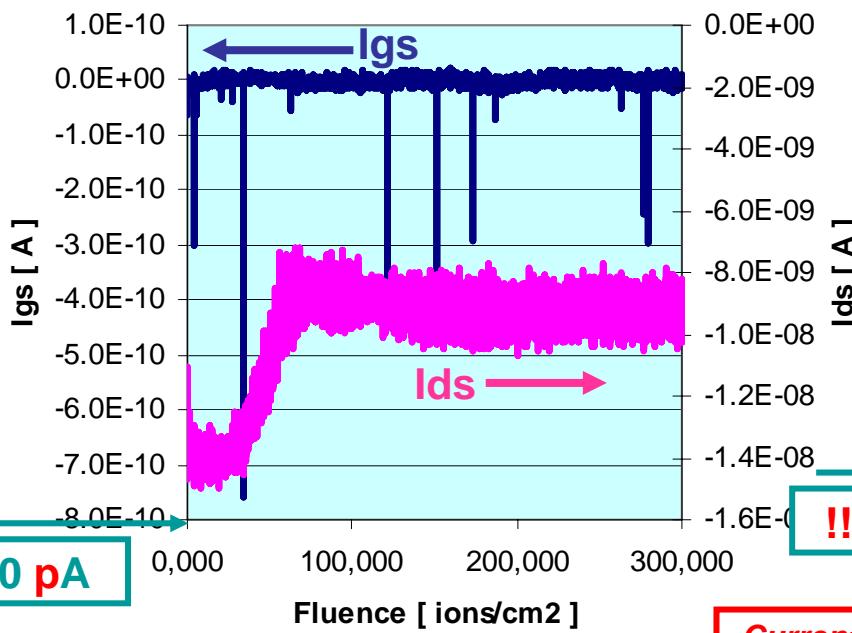
# Latent Oxide Damage

## ➤ Example Latent Oxide Damage

- $V_{ds} = 50 \text{ V}$
- $V_{gs} = 0 \text{ V}$

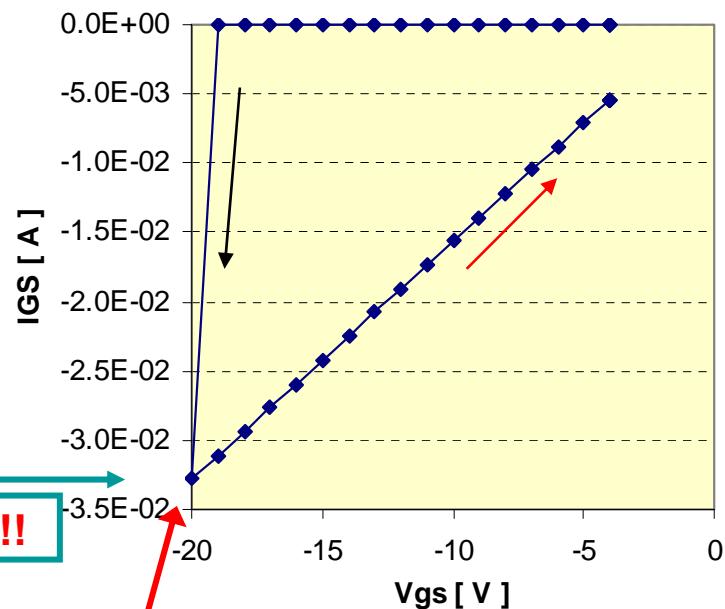
### *During Irradiation*

- *No evidence of rupture*



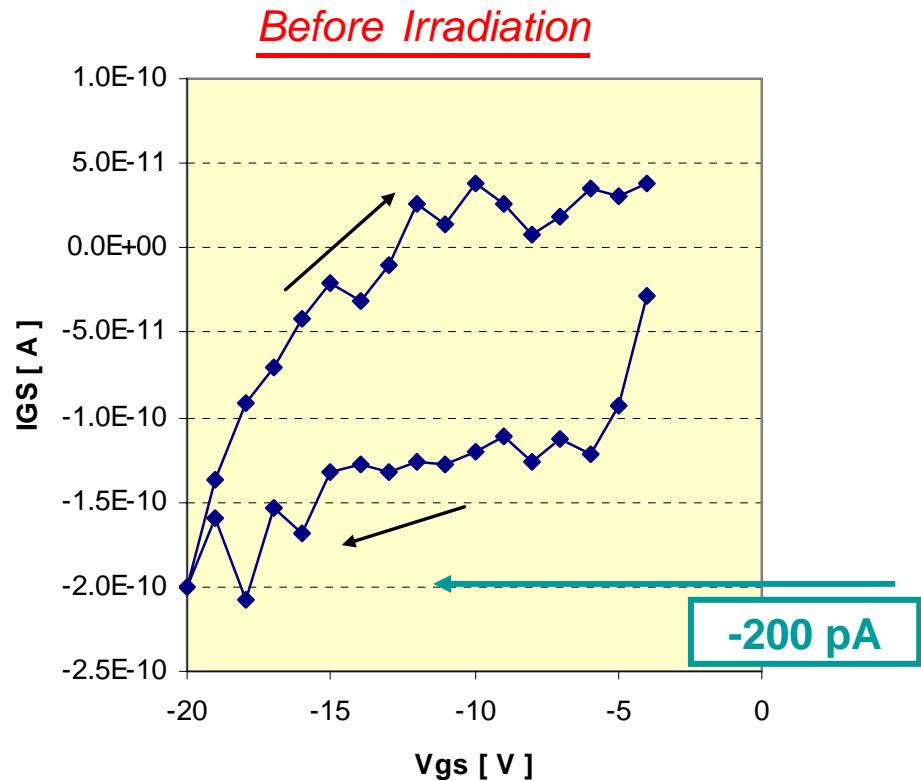
### *After Irradiation*

- *Rupture when applying -20V to gate*



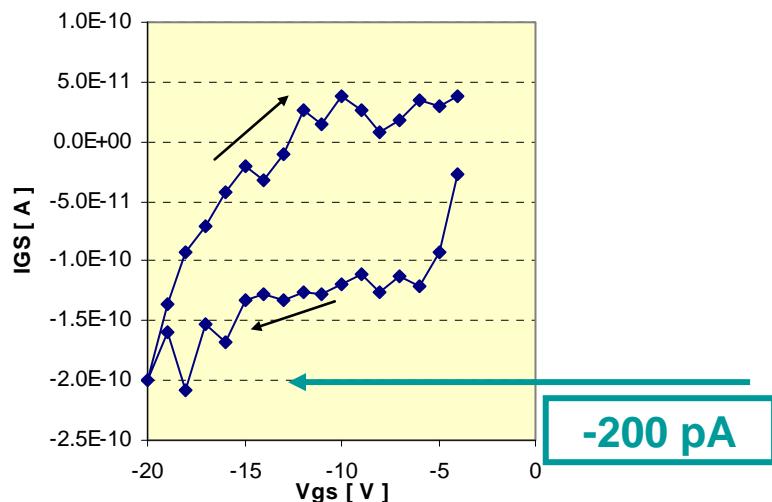
# Post Irradiation Gate Stress Test

- Reveal Latent Oxide damage
  - By applying a high voltage to the gate oxide after irradiation
    - Voltage level
    - Time of stress
- Used Method
  - Ramping up and down  $V_{gs}$  to maximum rated gate voltage :
    - At each voltage step measure
      - $I_{gs}$
      - $I_{ds}$
    - 200 ms at each voltage step

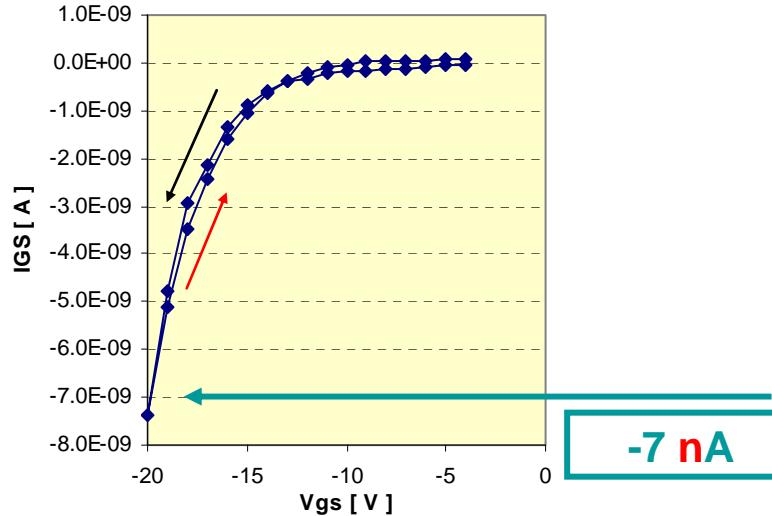


# Post Irradiation Gate Stress Test

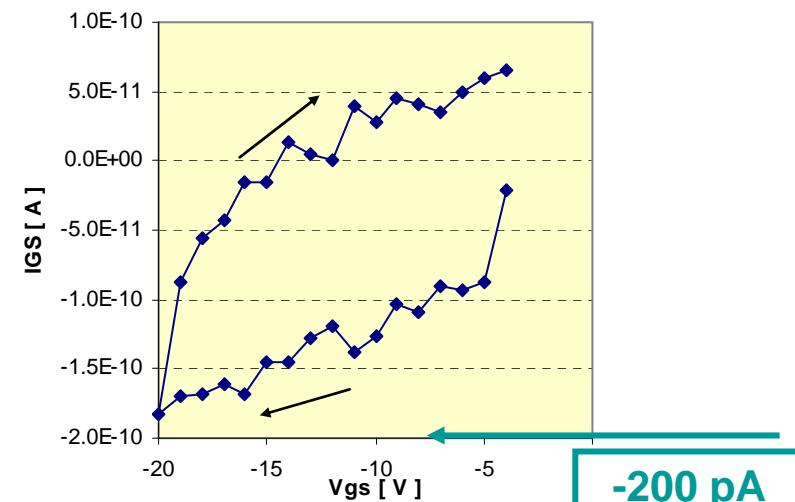
*Pre irradiation*



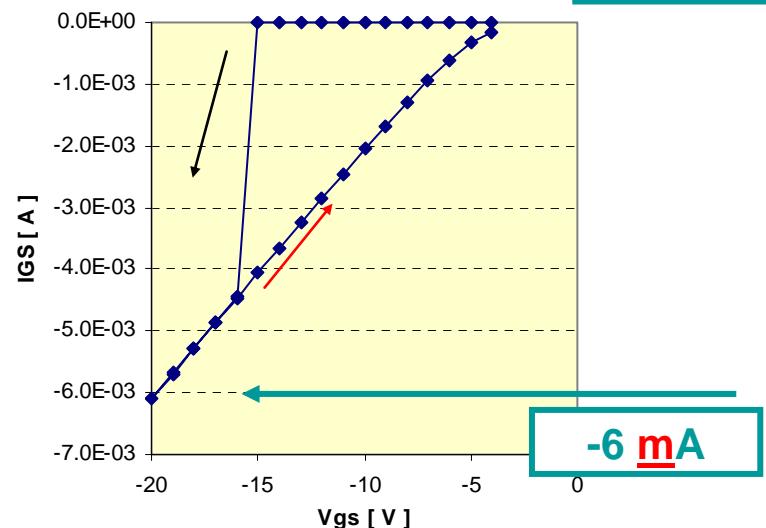
*Leakage Post irradiation*



*No change Post irradiation*

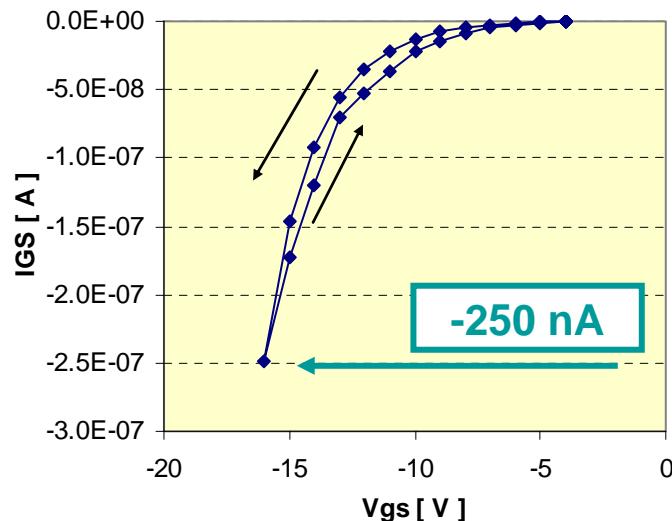


*Rupture Post irradiation*

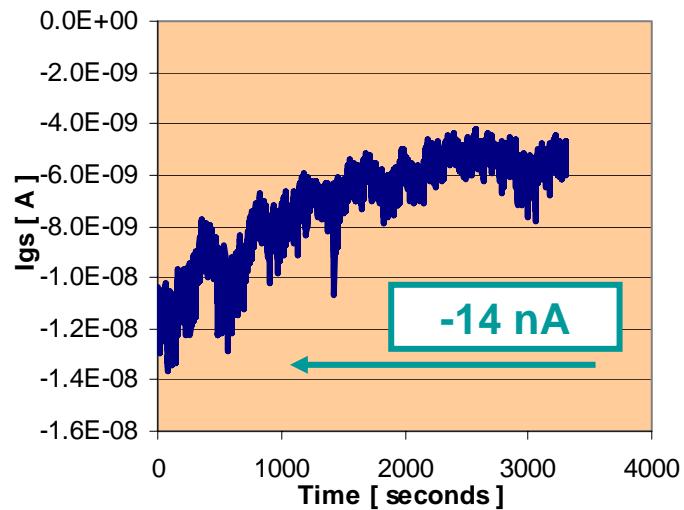


# Post Irradiation Gate Stress Test

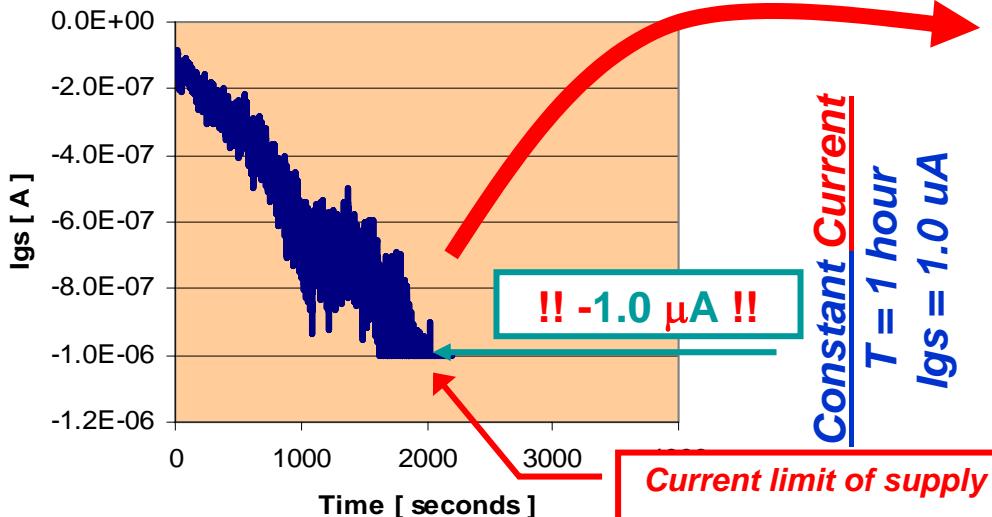
Voltage Ramp  
 $T_{step} = 200\text{ms}$



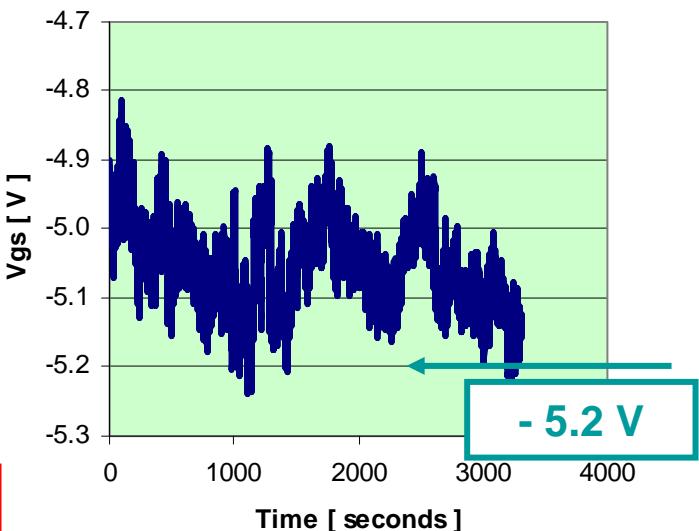
Constant voltage  
 $T = 1 \text{ hour}$   
 $V_{GS} = -12\text{V} (75\% \text{ of Max})$



Constant voltage  
 $T = 1 \text{ hour}$   
 $V_{GS} = 16\text{V} (100\% \text{ of Max})$



Constant Current  
 $T = 1 \text{ hour}$   
 $I_{GS} = 1.0 \mu\text{A}$



# Post Irradiation Gate Stress Test

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    - Range(Si) = 89um
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- Post Irradiation Gate Stress test
  - Voltage ramp to -20V<sub>gs</sub>
  - V<sub>ds</sub> = 0 V
  - T = 200 ms per voltage step
- Pass criteria for SOA
  - No SEGR during irradiation
  - I<sub>gs</sub> below 100nA in Post Irradiation Gate Stress test

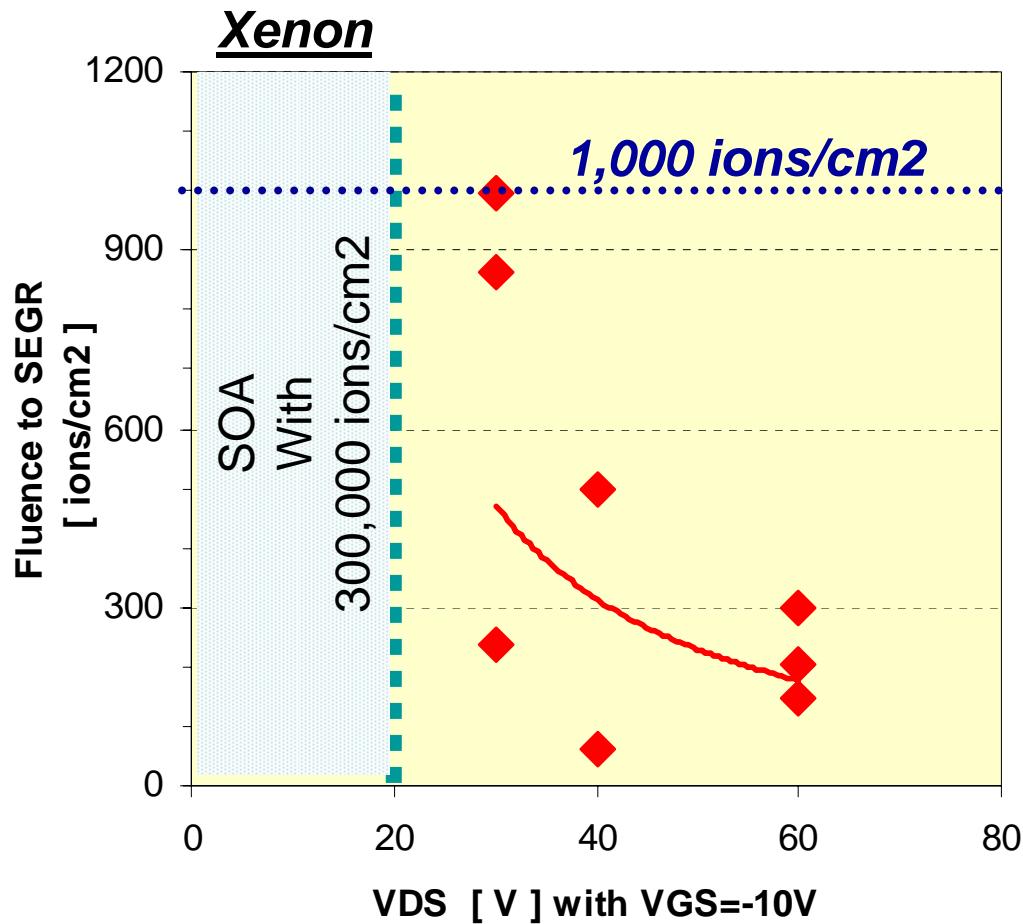
## ➤ CONCLUSION

- Post irradiation gate stress test must be performed in SEGR testing
- Degradation from SEGR can wrongly be interpreted to total ionising dose degradation
- Voltage and time are critical parameters

# Fluence Effects

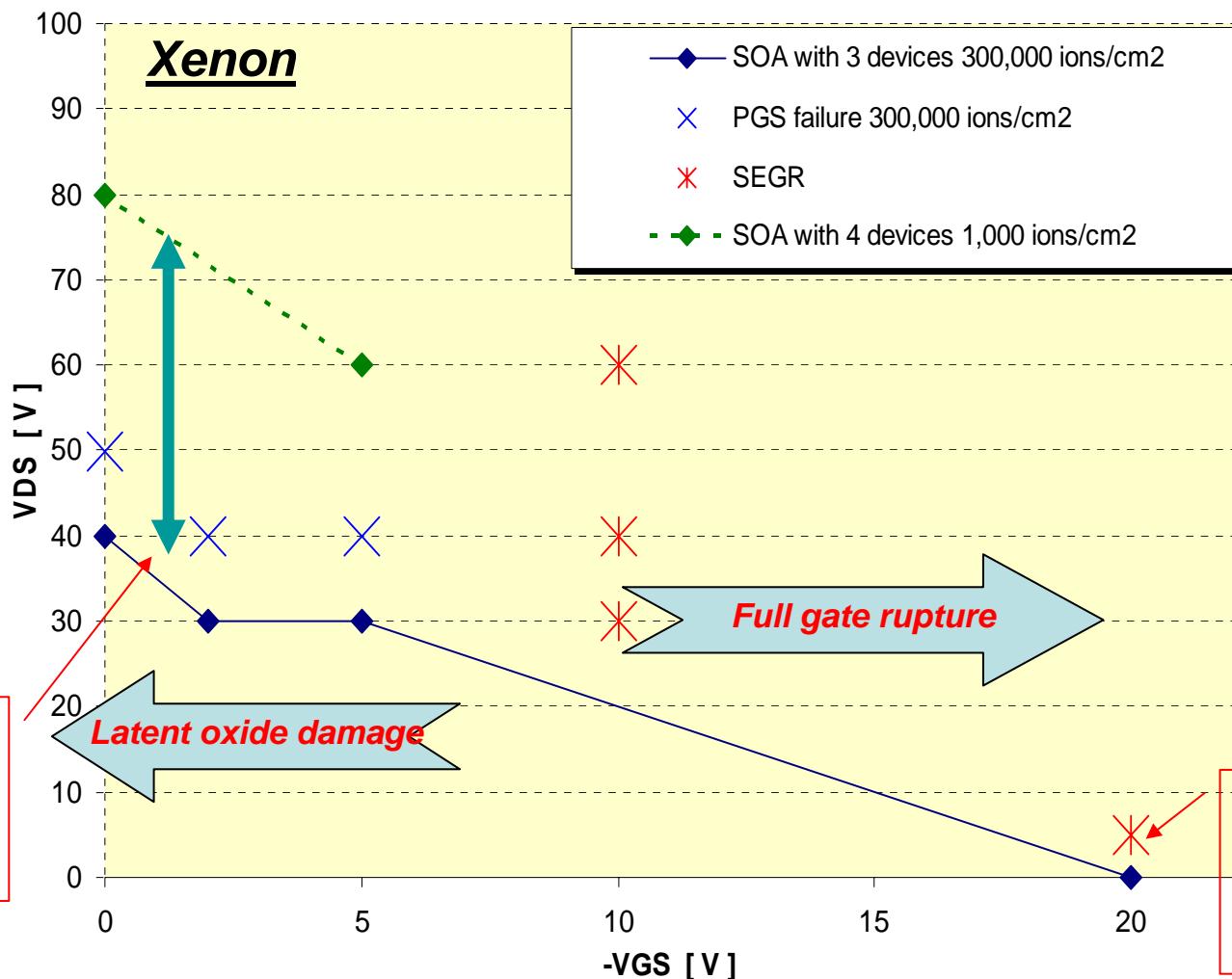
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- Pass criteria for SOA
  - No SEGR during irradiation
  - I<sub>gs</sub> below 100nA in Post Irradiation Gate Stress test
- SEGR Safe Operation Area as function of
  - V<sub>ds</sub> and V<sub>gs</sub>
  - Two Cases:
    - High Fluence
      - 300,000 ions/cm<sup>2</sup>
      - 1000 ions/cm<sup>2</sup>-s
      - 3 devices per bias condition
    - Low Fluence
      - 1,000 ions/cm<sup>2</sup>
      - 10 ions/cm<sup>2</sup>-s
      - 4 devices per bias condition

# Fluence Effects



- SOA with 1,000 ions/cm<sup>2</sup> exclude all possible fluence effects
- Total fluence with 4 devices is 4,000 ions/cm<sup>2</sup>
  - Well above measured cross section for SEGR

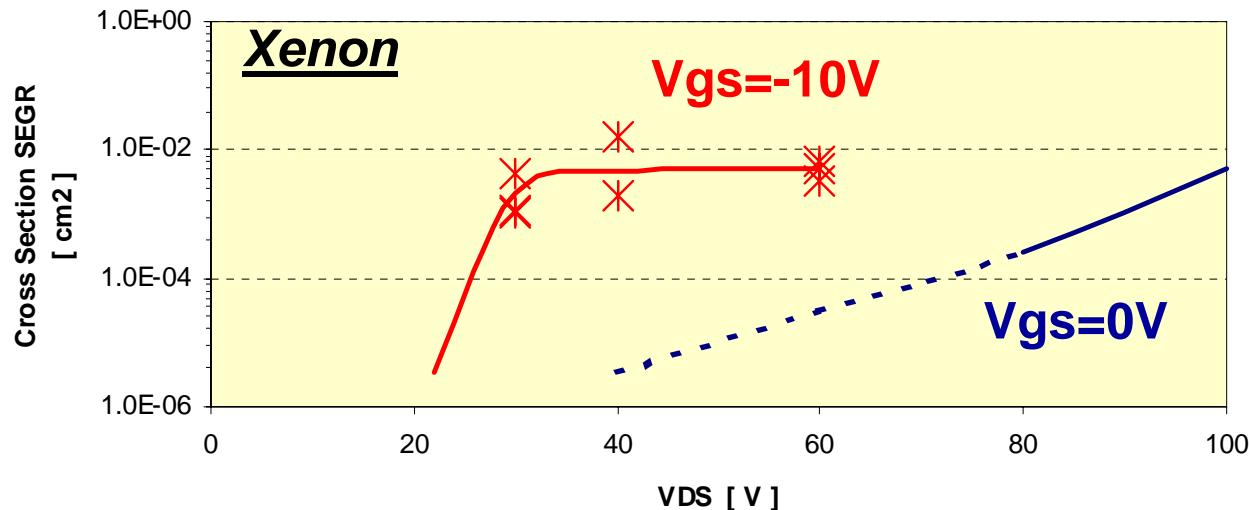
# Fluence Effects



# Discussion Fluence effects

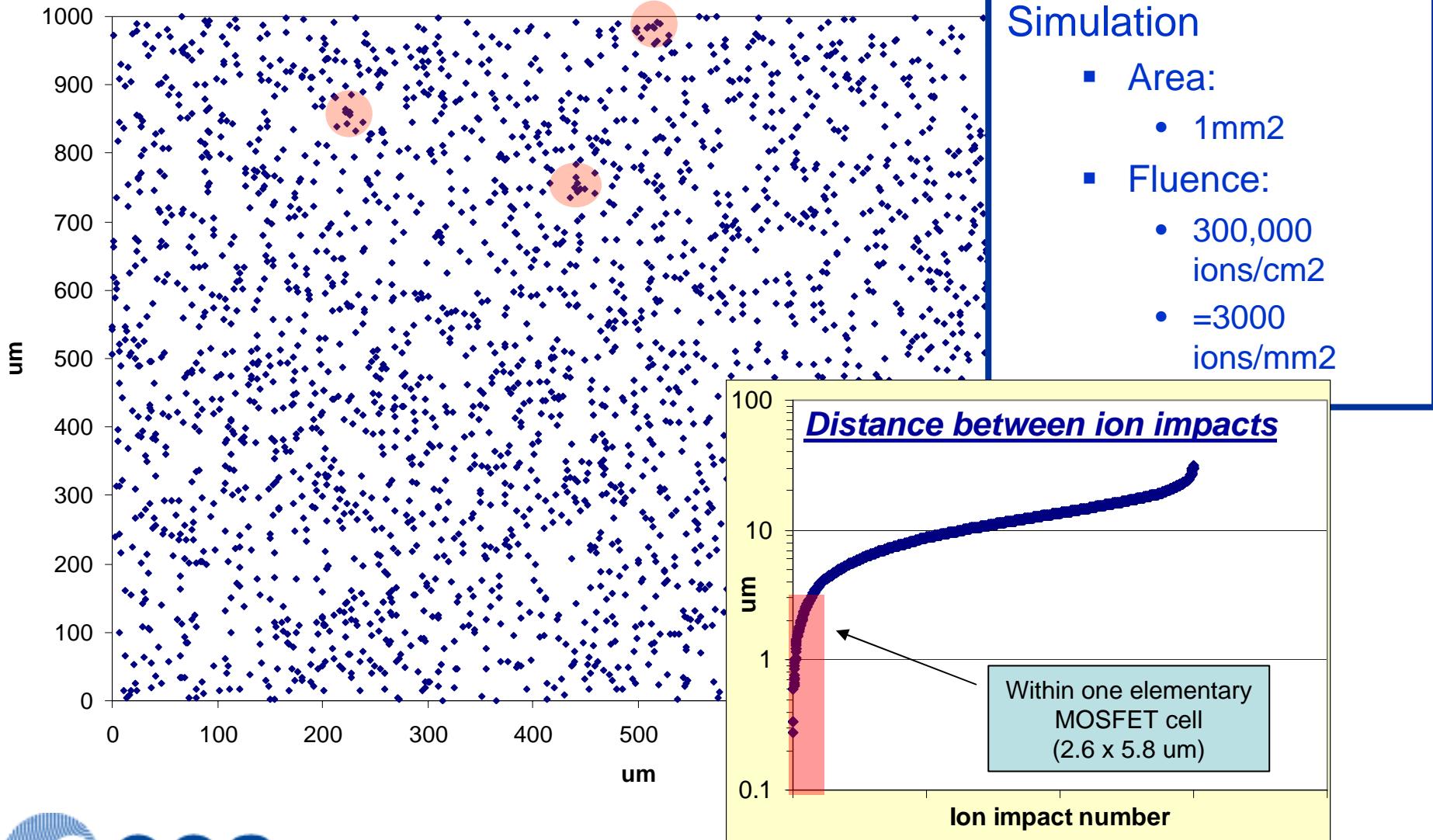
## Possible explanations:

- Wide threshold of SEGR vs Vds
  - Only at low gate voltages
    - Abrupt threshold at higher negative gate voltage



- Or artifact from Cumulative effects
  - The probability for ion impacts from more than one ion in an elementary cell increases with increased fluence

# Discussion Fluence effects



# Fluence Effects

## ➤ CONCLUSION

- Fluence effect observed in SOA
  - Multi impact effects can not be excluded
    - Miss experimental evidence & physical mechanism behind
- Fluence effects and Post Irradiation Gate stress will be further studied at ESA and CNES

# Results Safe Operation Area Krypton

