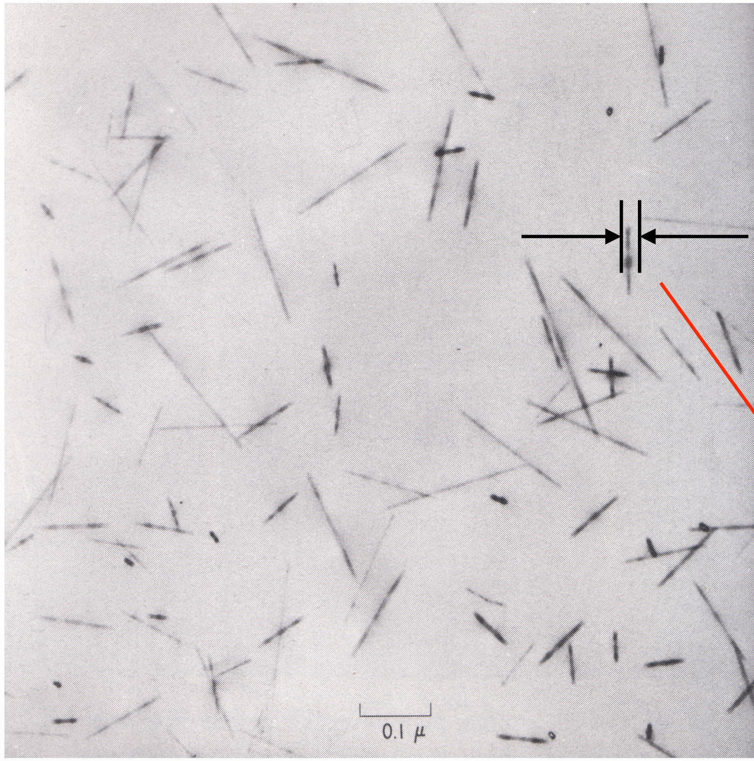
From Latent Tracks to Latent Defects

A. D. Touboul
Antoine.Touboul@ies.univ-montp2.fr

IES-UMR 5214
Montpellier 2 University, France

History and Motivation : Latent Tracks First Observation



^{238}U *fission fragment tracks on mica*

Historically first direct observation of fission fragment tracks : Silk & Barnes (1959)

Price & Walker (1962)
J. Appl. Phys. 33, 3407-3412

Ion Track diameter ~20 nm

What kind of effects might have such latent tracks on microelectronics ?

OUTLINE

Material study
based on Atomic Force
Microscopy observations of basic
SiO_2-Si structures

Morphological characterization of ion latent tracks in SiO_2 and at the SiO_2-Si interface

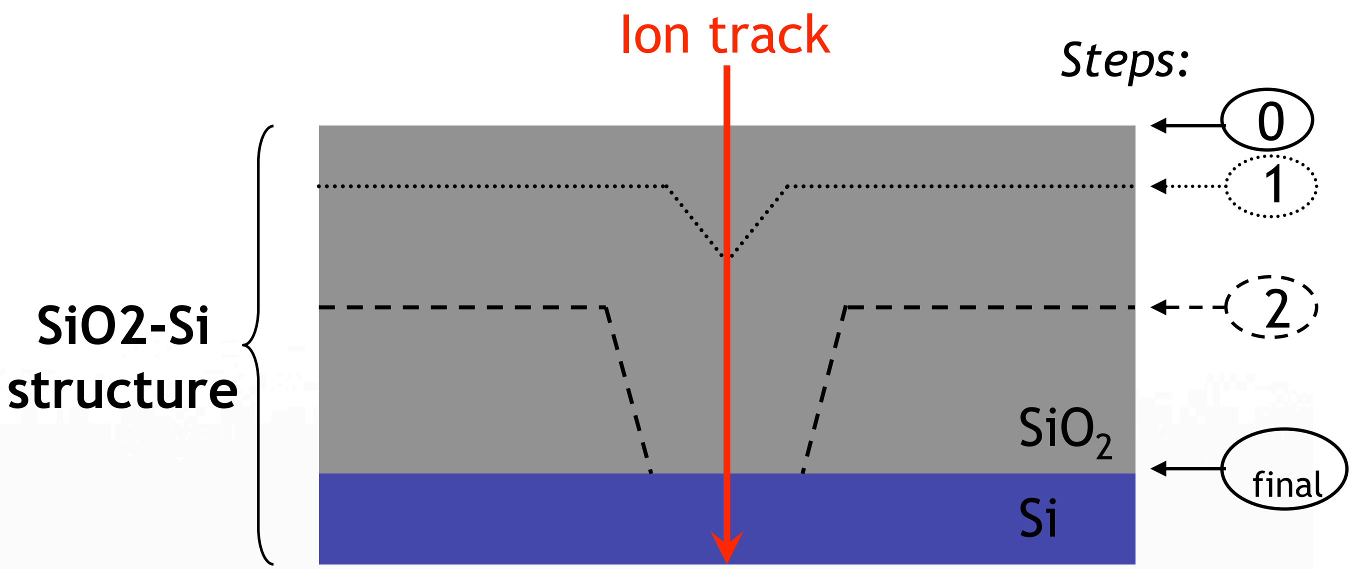
Electrical study
based on classical characterizations of MOS transistors (IgVg and IdVg subthreshold measurements) after irradiation.

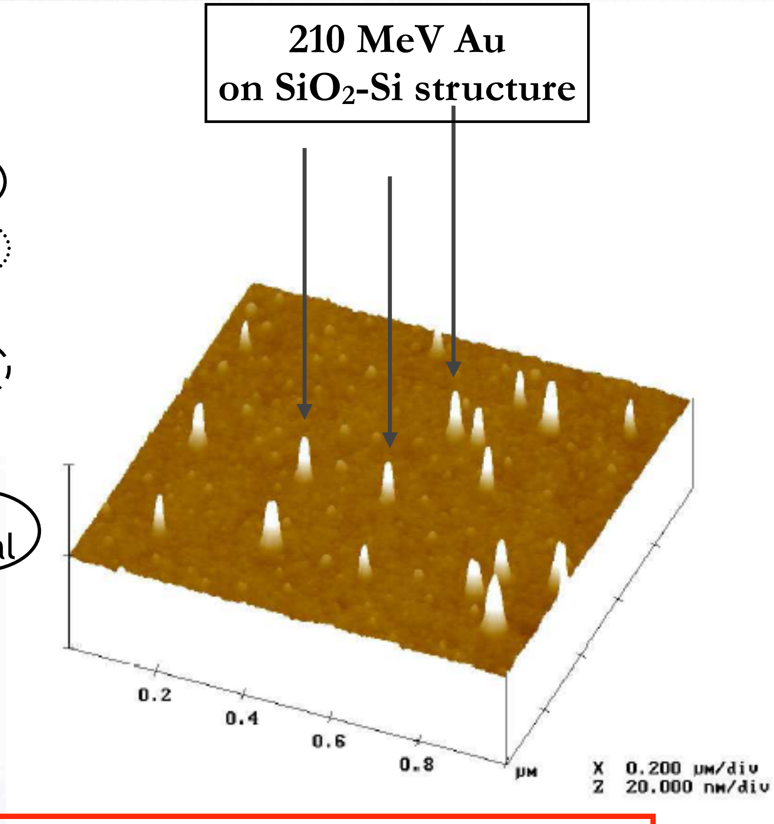
Summary of the effects occurring on the device operating

Post Irradiation Electrical Stress,
Thermal Annealing as a discriminating process

**Latent Defects Activation, Lifetime evolution,
Correlation with structural modifications**

Chemical Revelation of Ion Tracks in SiO2





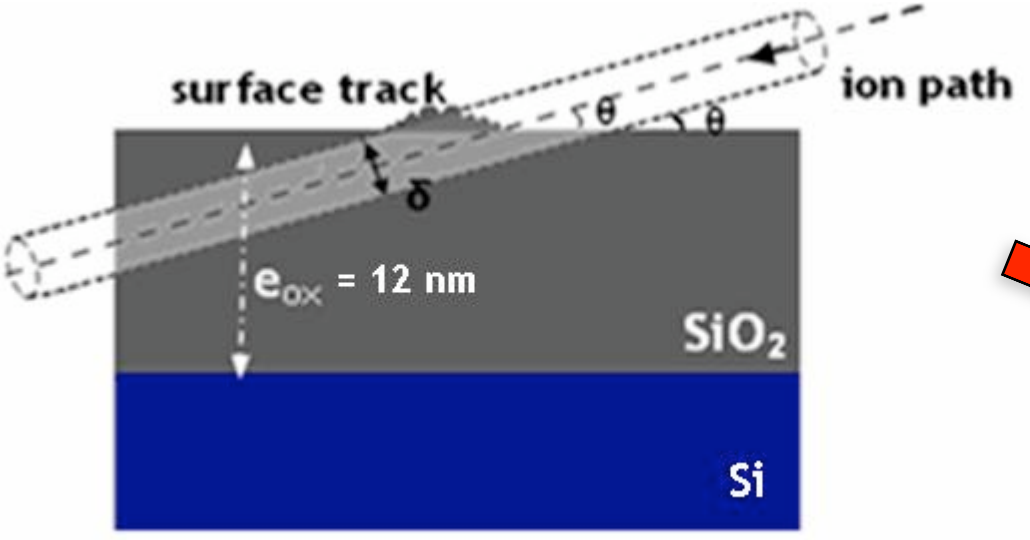
- Observation of heavy ion-induced silicon bumps at the SiO_2-Si interface

[Appl. Phys. Lett., vol 88, 041906-1 (2006)]

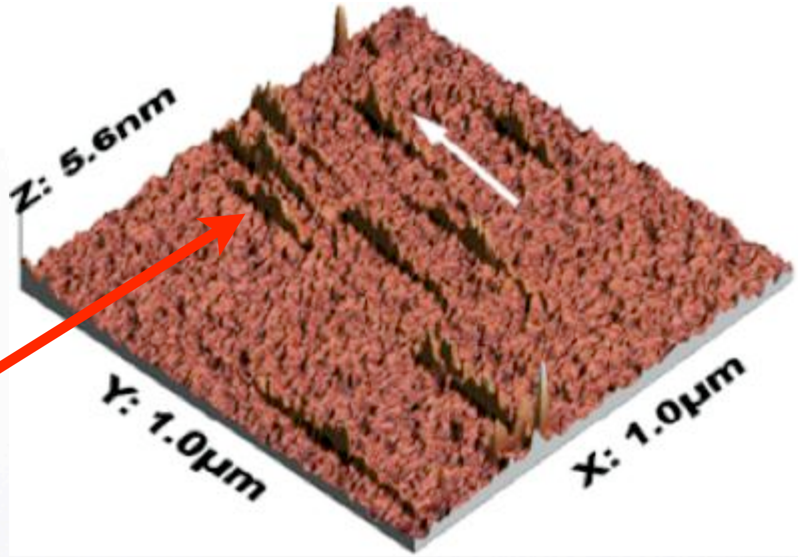
Correlation to other contribution works:
- Chaudhari et al. reported a crystallization effect within the SiO2 layer after a similar irradiation
- Rodichev reported a crystallization threshold LET about 3 keV/nm on SiOx-Si structures

Ion Tracks Observation at the SiO2 Surface

- Grazing angle, $\theta = 1°$



Pb, 940 MeV on SiO_2-Si at 1°
e_{ox}: 11.8 nm
Φ : 5.10^{10} cm^{-2}
LET : 104 $MeV.cm^2.mg^{-1}$



- Heavy ion induced structural modifications on SiO_2
- Typical shape: Nanodot trail
- Discontinuous energy deposition along the ion path

[Appl. Phys. Lett. 90, 073116 (2007)]

Ion Tracks Oxide Thickness Dependance

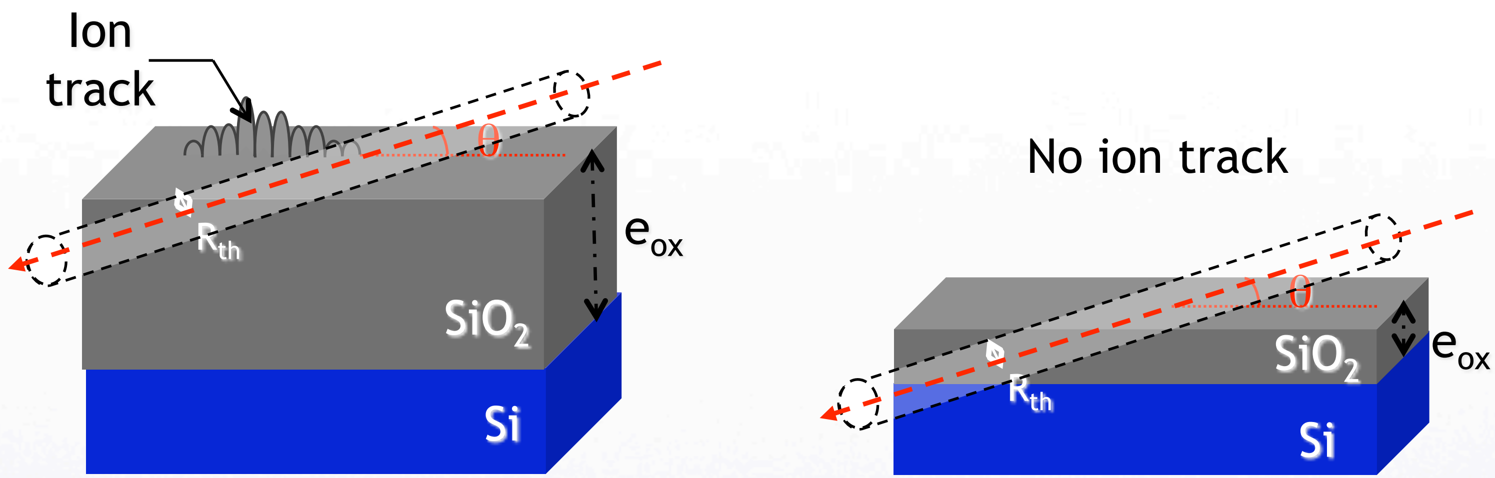
Pb, 940 MeV on SiO_2-Si at 1°

e_{ox}: 11.8 nm

Φ : 5.10^{10} cm^{-2}

LET : 104 $MeV.cm^2.mg^{-1}$

GRAND ACCELERATEUR NATIONAL D'IONS LOURDS
LABORATOIRE COMMUN DSM/CEA-IN2P3/CNRS



e_{ox} = 50 nm, 10 nm, 4 nm

e_{ox} = 2 nm

- Ion tracks are formed for oxide thickness upper than 2 nm
- Thin oxides might be immune regarding track formation

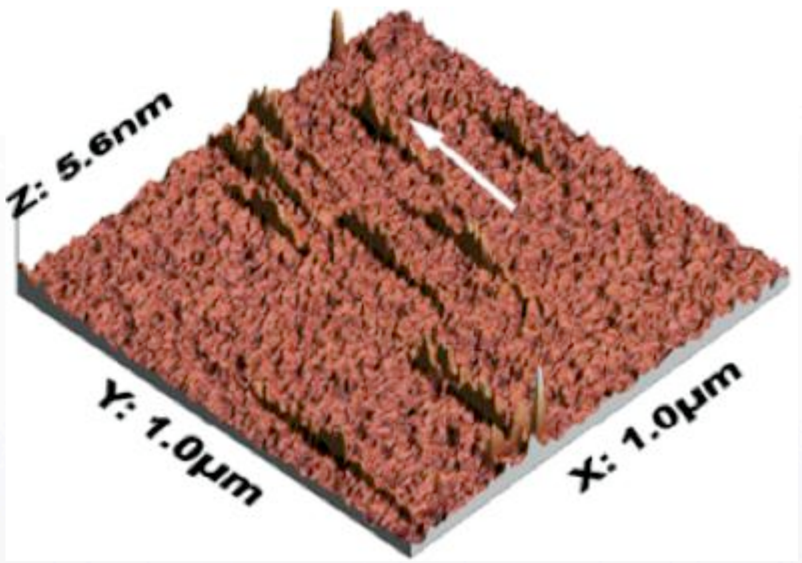
[J. Appl. Phys. vol 102, 124306.1-4 (2007)]

Ion Tracks Thermal Stability

- Isochronal annealing Step: 50°C during 10 min
  T: 150°C to 350°C

Pb, 940 MeV on SiO_2-Si at 1°
e_{ox}: 11.8 nm
Φ : 5.10^{10} cm^{-2}
LET : 104 $MeV.cm^2.mg^{-1}$

Before annealing



After annealing

- Structural modifications (i.e.Nanodot trails) are still visible after isochronal annealing

- No annealing effect on ion-induced morphological defects

EXPERIMENTS

Heavy ion irradiation of MOS transistors

Experimental Set-Up, Electrical Characterization

- Heavy ion irradiation (GANIL, Caen, France)
  - 940 MeV Pb, LET = 104 $MeV.cm^2.mg^{-1}$,
  - Fluence: $1x10^7$ to $1x10^8$ cm^{-2}

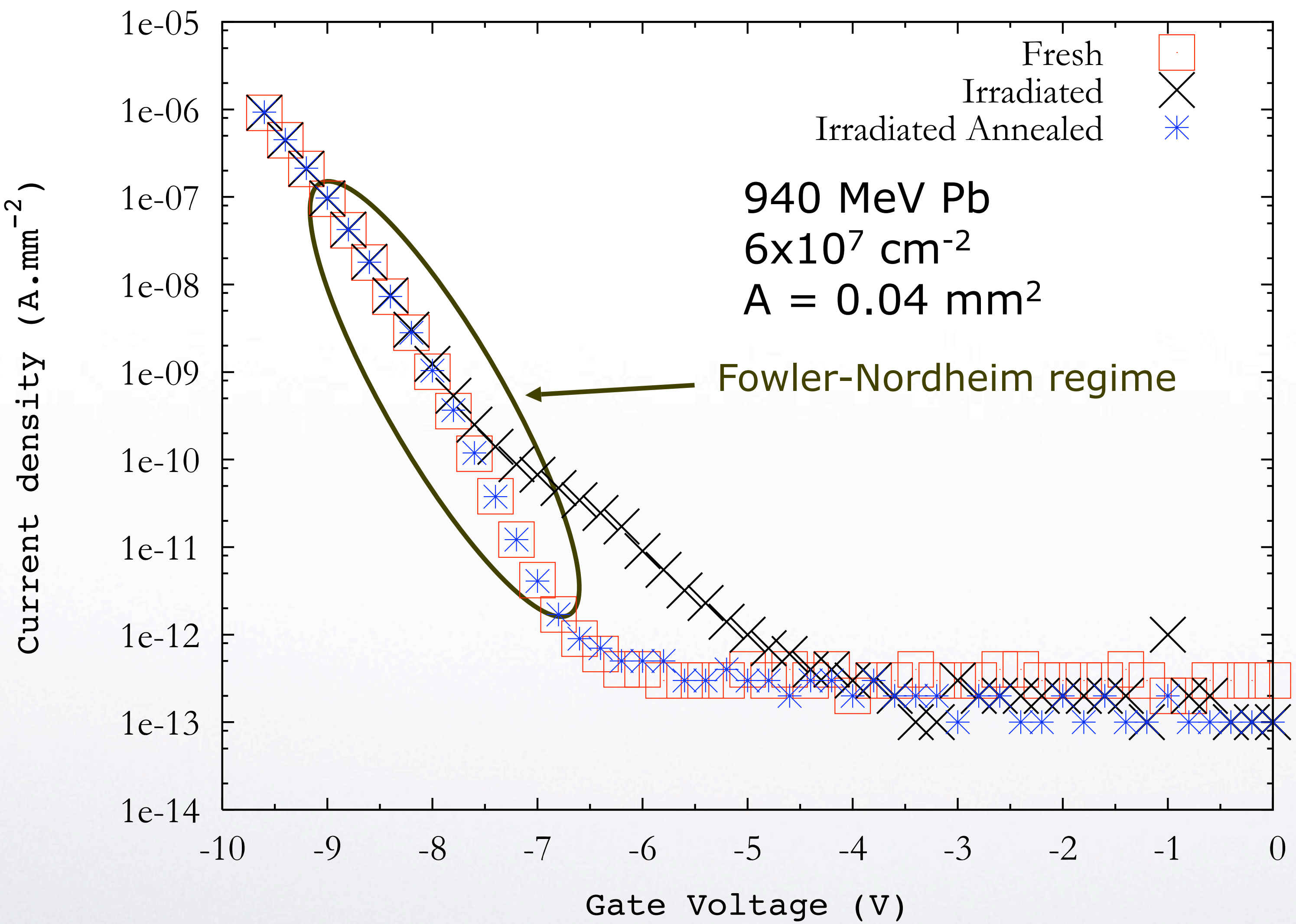
GANIL
GRAND ACCELERATEUR NATIONAL D'IONS LOURDS
LABORATOIRE COMMUN DSM/CEA-IN2P3/CNRS

- MOS devices
  - t_{ox} = 9.5 nm (technology node 0.5 µm)
  - A_G = 0.04 mm^2
  - p-Si substrate

- I_G (V_G) **Gate leakage current**
- Subthreshold I_{DS} (V_G)
  - **Interface states density (N_{it} variation)**
  - **Oxide trapped charges density (N_{ot} variation)**

Before irradiation / After irradiation / After isochronal annealing

HEAVY ION-INDUCED LEAKAGE CURRENT



Heavy ion irradiation induced:

➔ RILC (Neutral traps)

➔ Slight increase of Nit

Full recovery of RILC @ 300°C / Nit @ 350°C

Summary of Energetic Heavy Ion-Induced Electrical Effects

- Heavy ion irradiation
  - RILC
  - ΔN_{it} increase
  - No ΔN_{ot} variation

- Isochronal annealing and eventual recovery of both RILC and ΔN_{it} **[IEEE Tran. Nuc. Sc., 55-6 (2008)]**

=> Apparent recovery of the electrical characteristics of the irradiated parts…

Experiments

Post Irradiation Electrical Stress

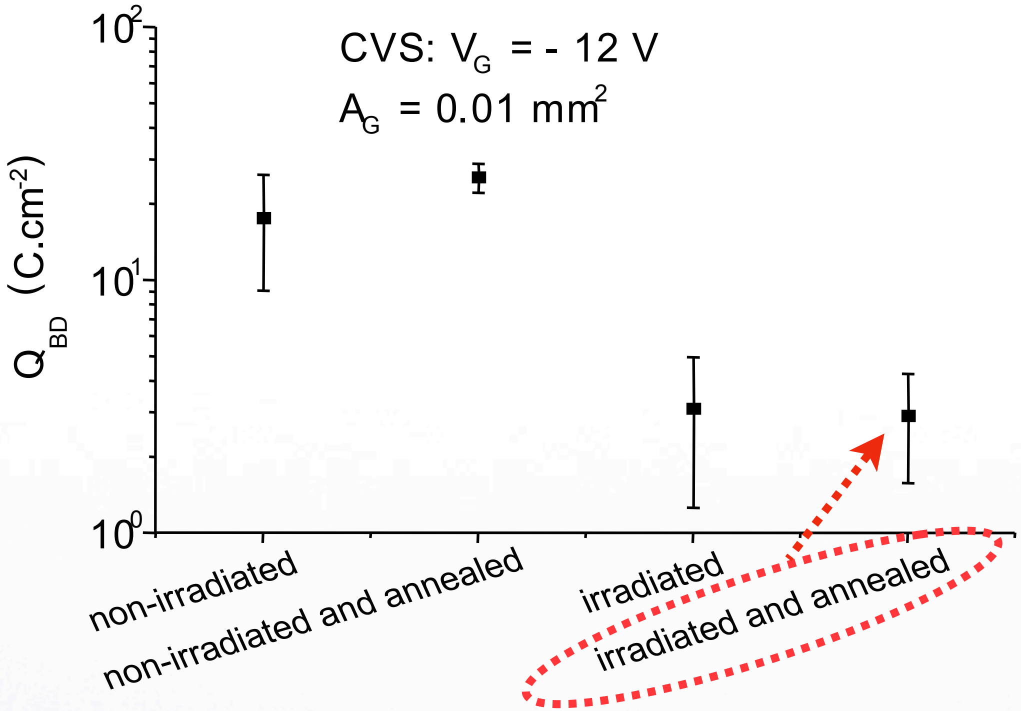
EXPERIMENTAL SET-UP AT A GLANCE

- MOS devices
  - Non-irradiated devices subjected or not to thermal annealing
  - Irradiated devices subjected or not to thermal annealing

- Constant Voltage Stress (CVS) @ V_G = -12 V

  ➡ $\mathbf{t_{BD}}$, $\mathbf{Q_{BD}}$

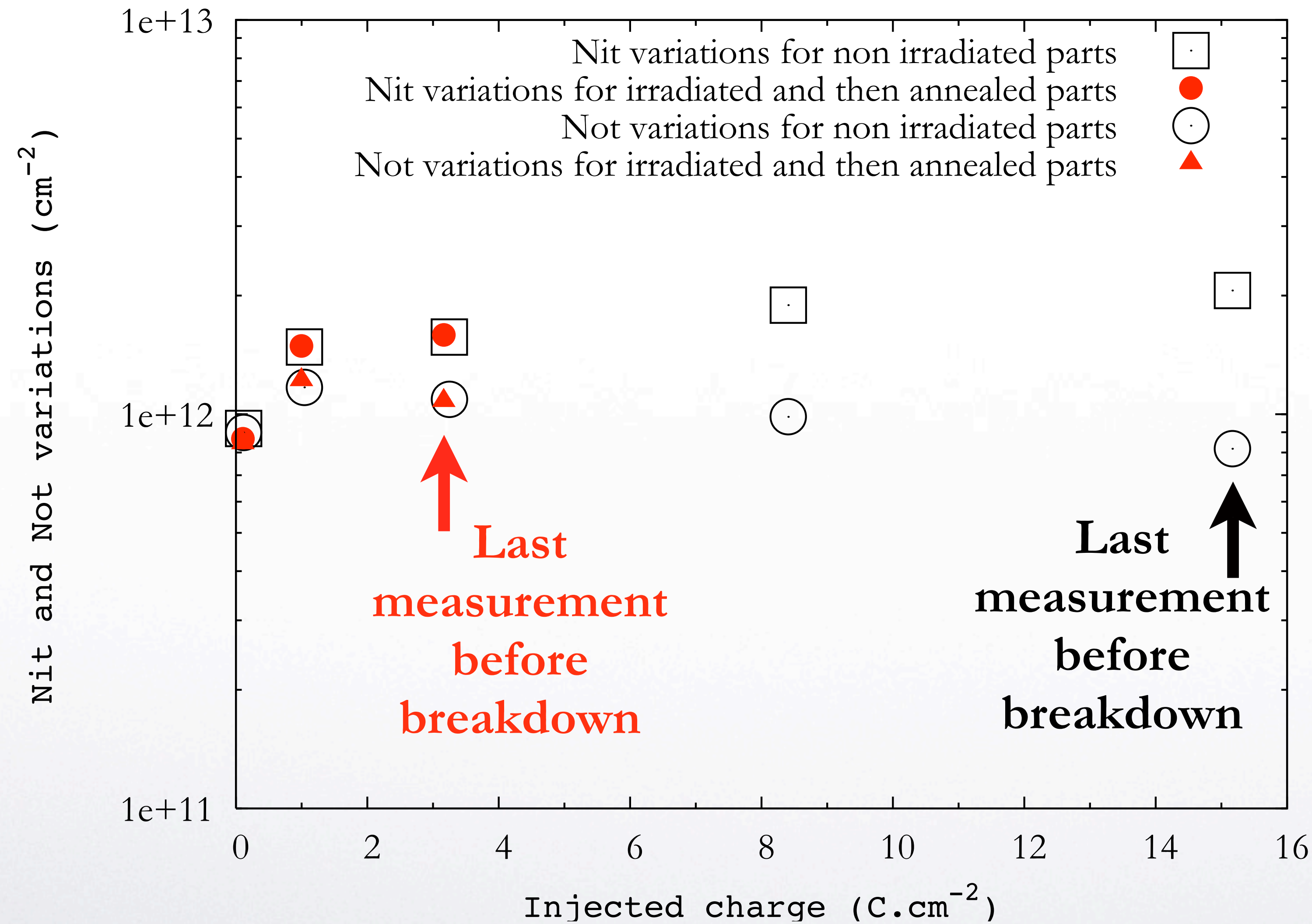
Charge to Breakdown Evolution, Q_{BD}



Decrease of Q_{BD}
after heavy ion irradiation,
even on thermally
annealed devices

- ☑ **No full recovery after heavy ion irradiation**
- ☑ **Structural modifications are kept in material's memory**
- ☑ **Influence of structural modifications on triggering breakdown**

Nit and Not Evolution during Post Irradiation Electrical Stress



Interface state and oxide trap densities do not influence the triggering of premature breakdown.

Structural modifications might act as an extra contribution leading to premature breakdown

KEY POINTS AND CONCLUSION

- **Preliminary study on elementary MOS transistors**
  - Heavy Ion latent tracks might not be formed on ultrathin oxide devices
  - Latent defects, when created, are not removable using thermal annealing
  - After irradiation : decrease of t_{BD} and Q_{BD}
  - Decrease of t_{BD} , Q_{BD} even after thermal annealing : That might connect latent tracks (i.e. Structural modifications) to latent defects

- **On the Post Irradiation electrical Stress :**
  - Needs to be carefully and precisely defined ...
  - Indeed, from the physics, no oxide can be immune to breakdown, it is just a matter of time
  - Some reliable indicators might be t_{BD} or even better Q_{BD}