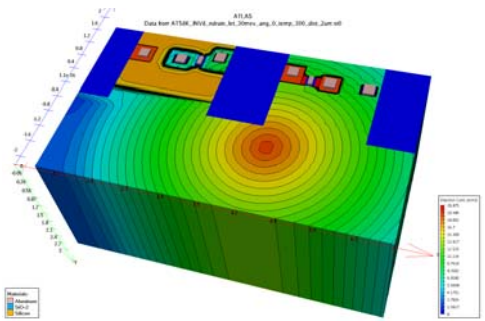
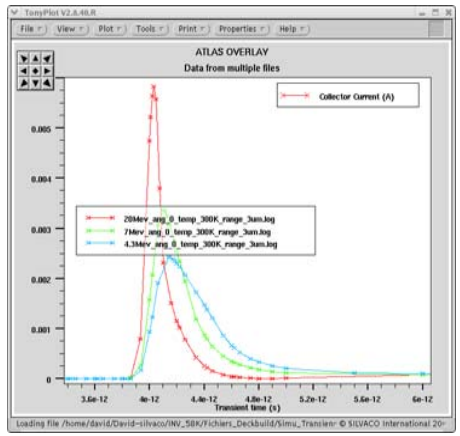
Single Event Transient characterization and mitigation for logic circuits using the 0.18µm CMOS AT58KRHA process for space use

Final Presentation

Contract : CNES n° 04/1643/00





Guy MANTELET
ATMEL Nantes
+ 33 2 40 18 19 42
guy.mantelet@atmel.com

Agenda

- Context and objectives of this study
- 3D simulations
- V42 SET test vehicle content
- Heavy ions test results
- Protons test results
- Correlation between simulations and test results
- Design recommendations

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- **Context and objectives of this study**
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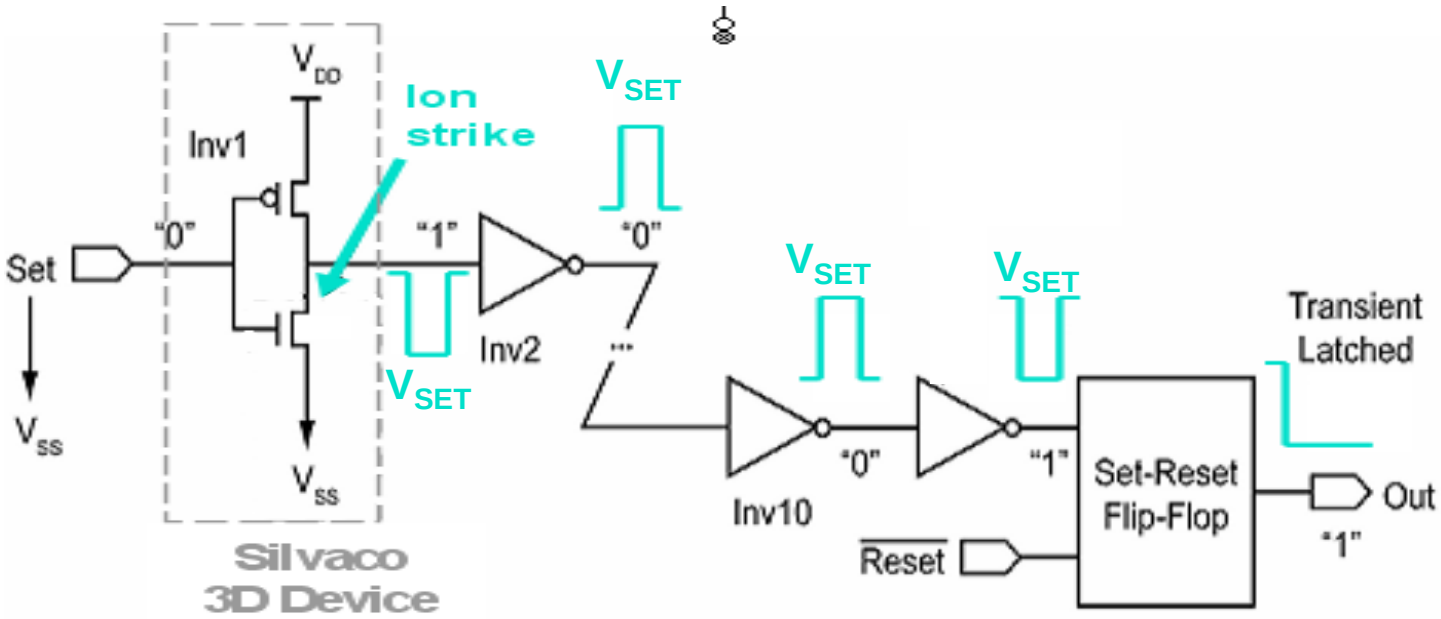
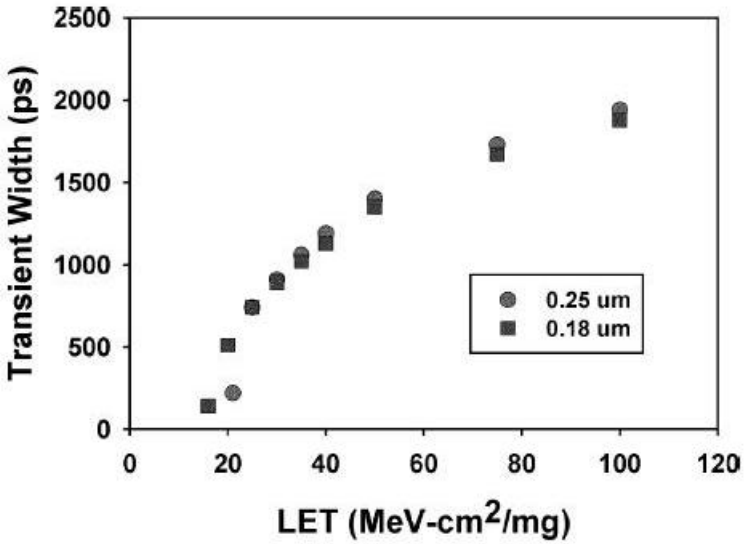
Single Event Transient

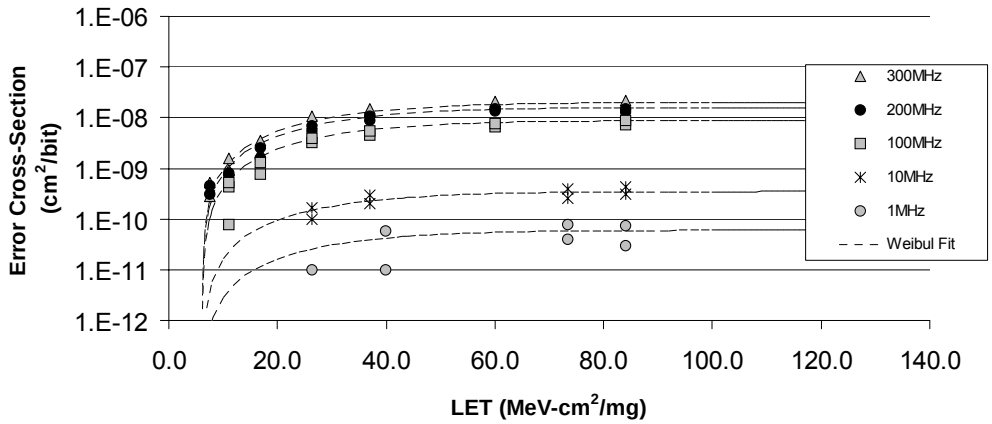


Dodd et al IEEE TNS, 2004

Context (1/2)

- **In 2004 and 2005 : a number of IEEE papers presented at NSREC or RADECS**
  - **Show SET events on CMOS 0.25µm and below**





Context (2/2)

- **ATC18RHA V34 test vehicle included a few SET structures**
  - **Some events seen at high energy**
  - **Small number of runs**
  - **Reduced set of cells / no pulse duration measurement**
  - **Some correlations when using Spice simulations**

Gate Number	*nd04d11x Min LET (MeV/(mg/cm2))*	*nd04d14x Min LET (MeV/(mg/cm2))*	*nd04d21x Min LET (MeV/(mg/cm2))*	*nd04d41x Min LET (MeV/(mg/cm2))*
1024th / 1022nd	2.34	3.12	10.94	23.44
834th / 832th	11.72	27.34	67.97	157.03
648th / 646th	64.84	173.44	-	-
424th / 422nd	-	-	-	-
202nd / 200th	-	-	-	-
18th / 16th	-	-	-	-

- **Drive and load influence, Cell type influence, SET Filtering**

Objective of the CNES contract

- **Accurate characterisation of SET on ATC18RHA**
  - **3D simulation**
  - **Test vehicle to measure SET under radiation**
    - **Occurrence of events**
    - **Pulse width measurement**
- **Mitigation techniques**
  - **Investigate and implement different solutions**
  - **Recommendations for ASIC customers**

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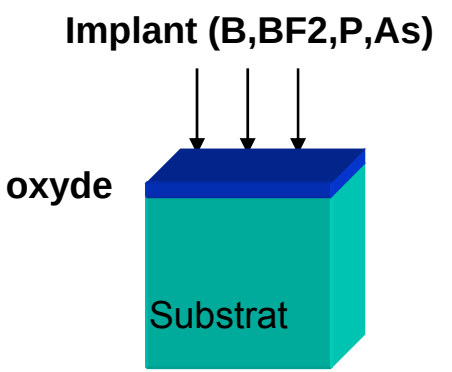
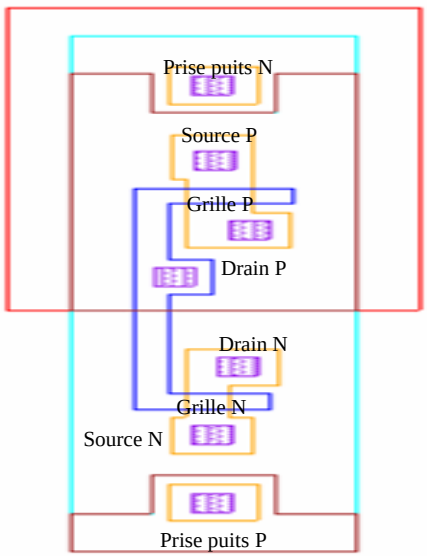
3D simulations

- **Thesis on SET on ATC18RHA with CEM2 – University of Montpellier, France – from 2005 to 2007**
- **Modelling of the technology and of simple structures, using 3D tools**
- **3D simulation runs on SRAM and inverters**
- **Parameters**
  - **LET**
  - **Distance between ion impact and the structure**
  - **Temperature**
  - **angle**
- **Layout influence**

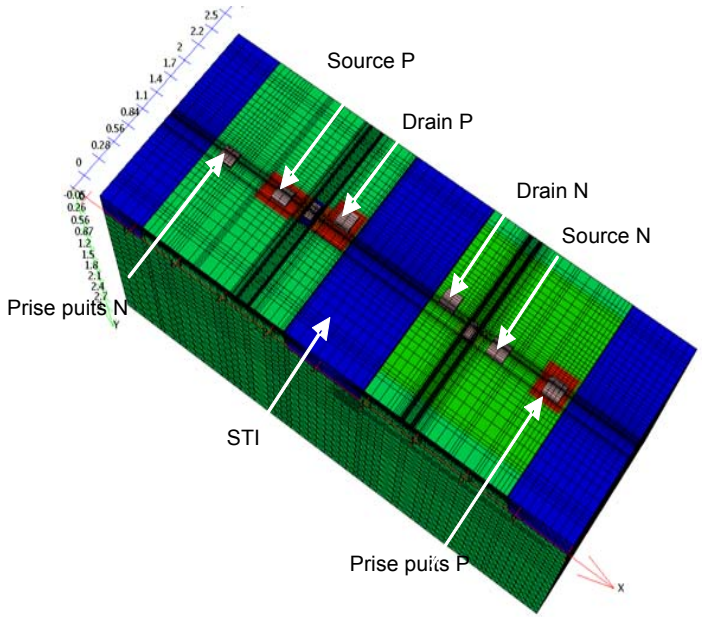
Device Modelling

Transistor level





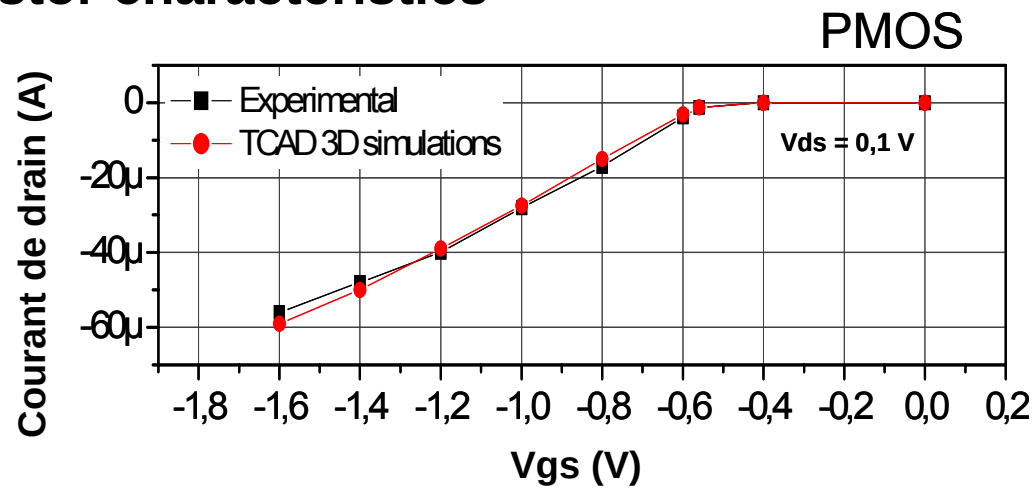
Devedit3D

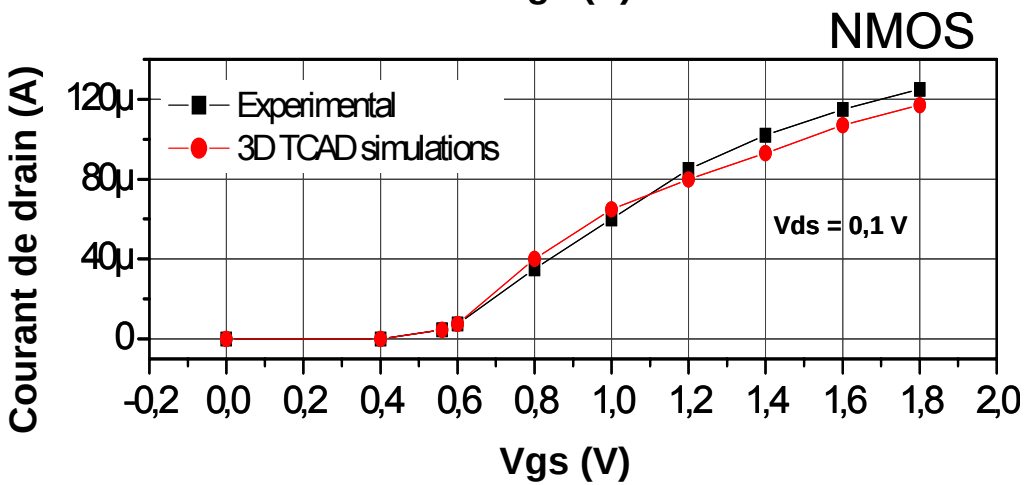


➢ **The real topology is reproduced**

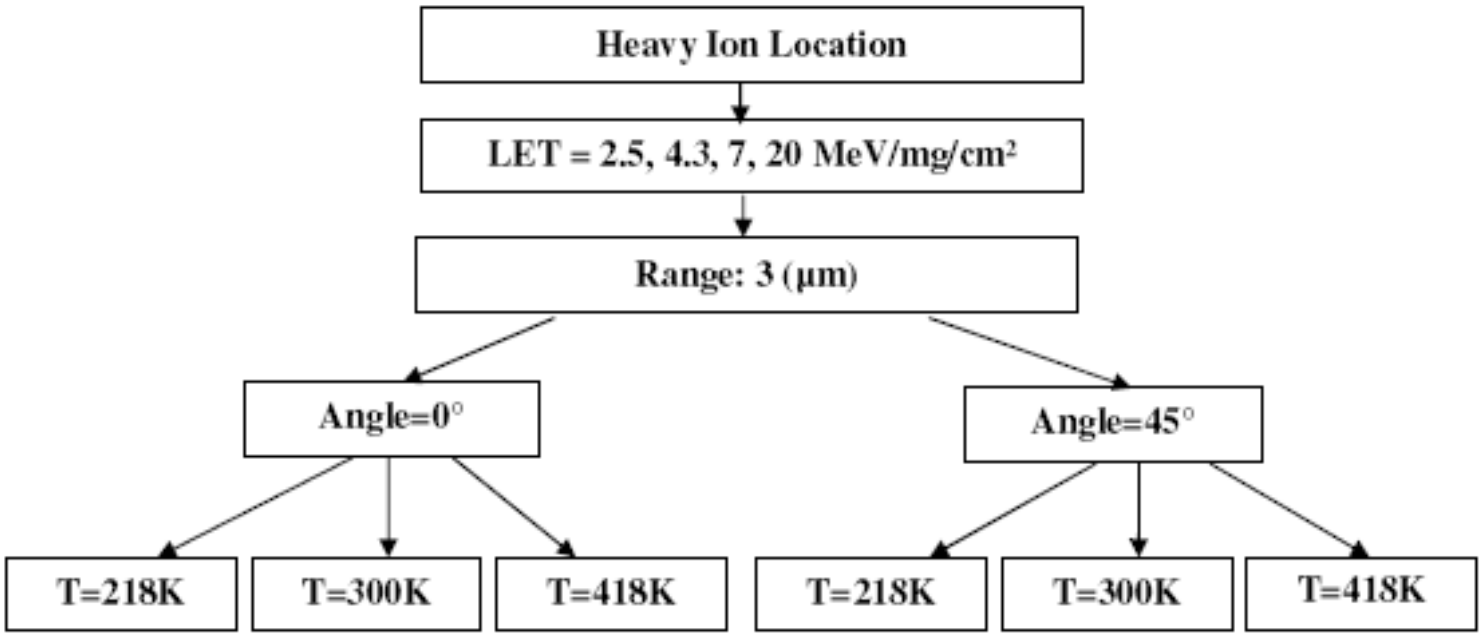
Validation of the 3D devices

Transistor characteristics





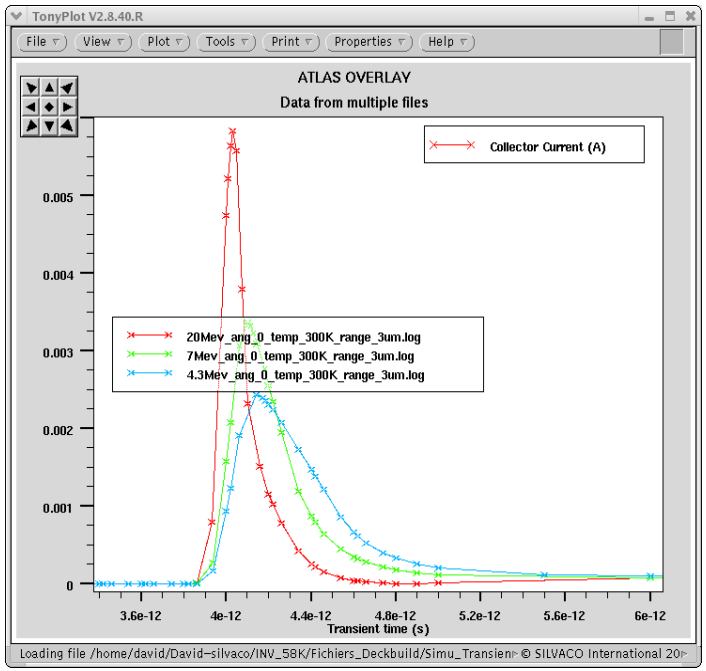
Simulation plan

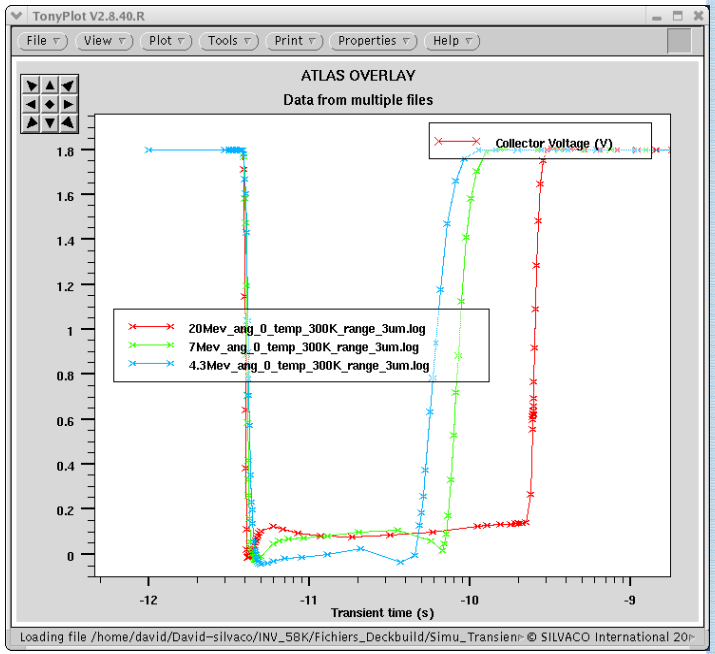


Simulations results – Inverter - LET

- **SET CURRENTS EXAMPLE :**

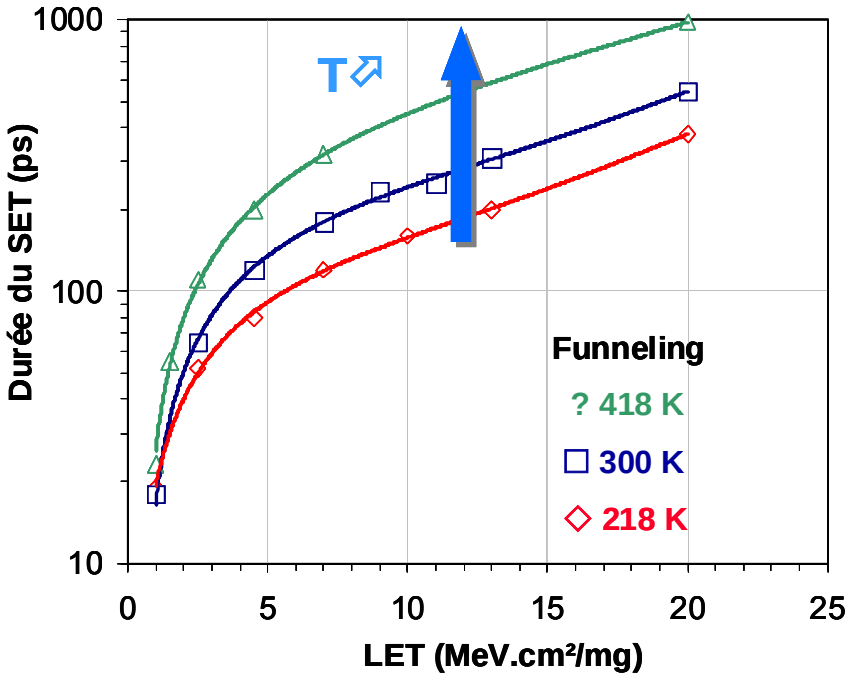
Idrain & Vdrain (Nmos Off) Versus LET

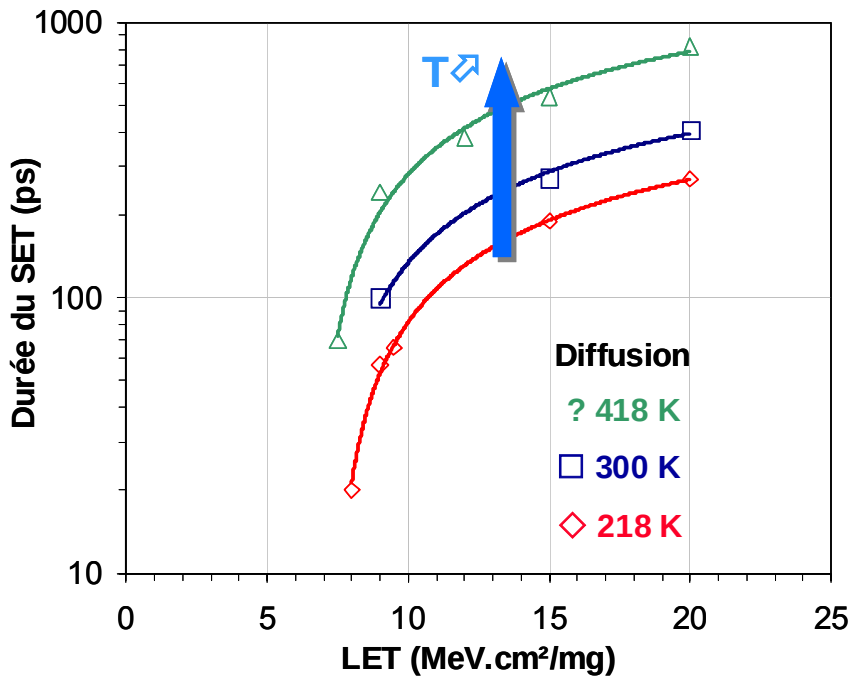




The Voltage duration increases with LET.

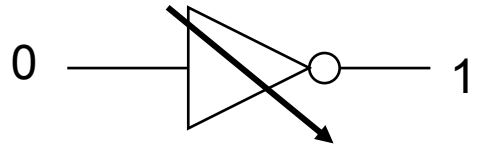
Simulation results – inverter - temperature

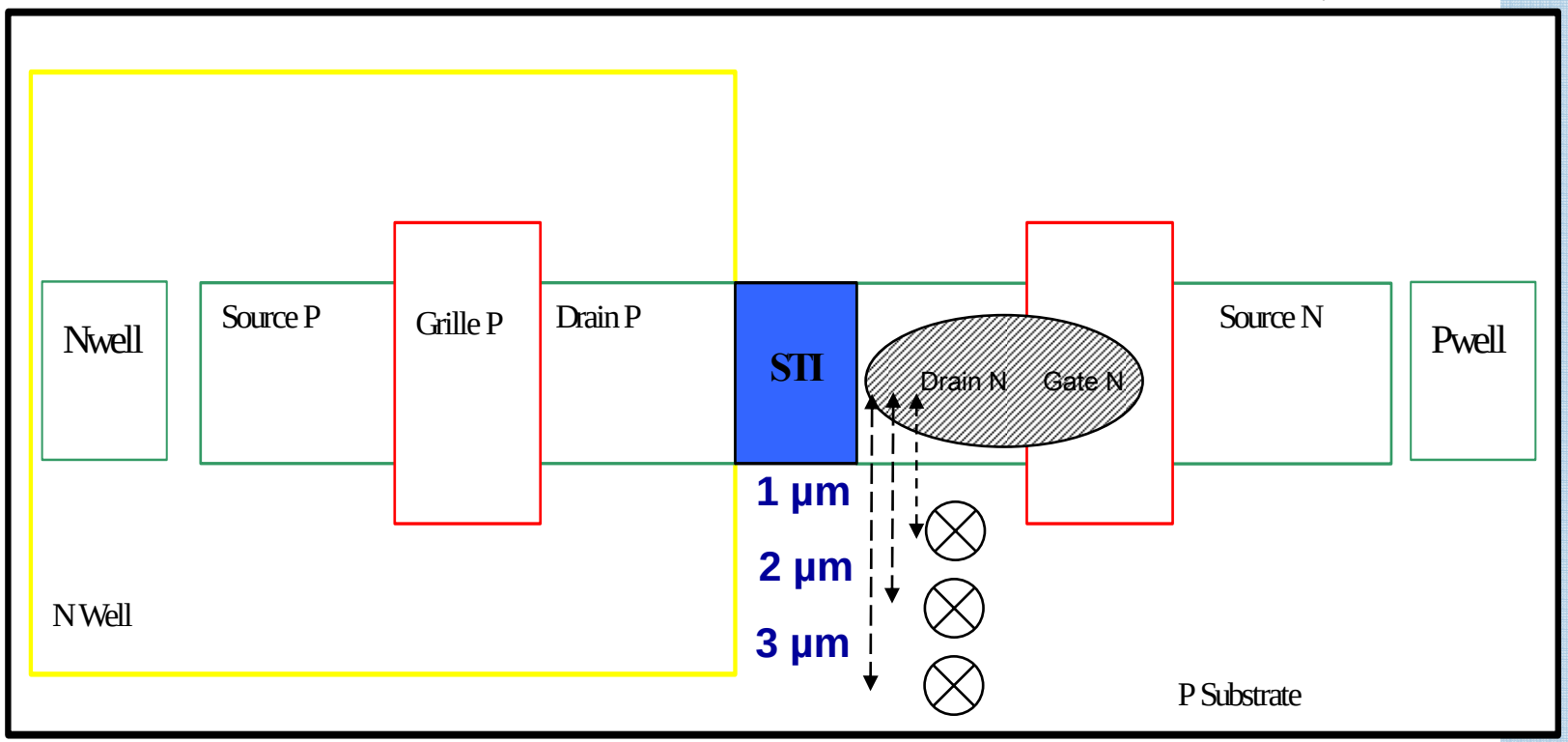




Influence of heavy ion impact location

- **Inverter**

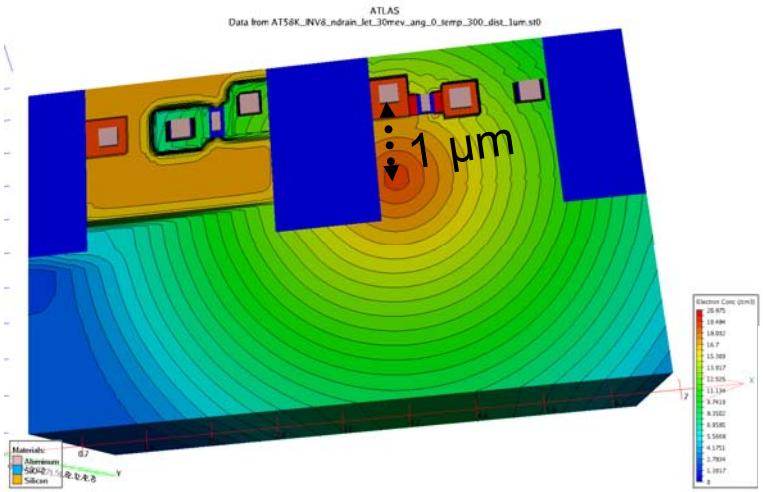


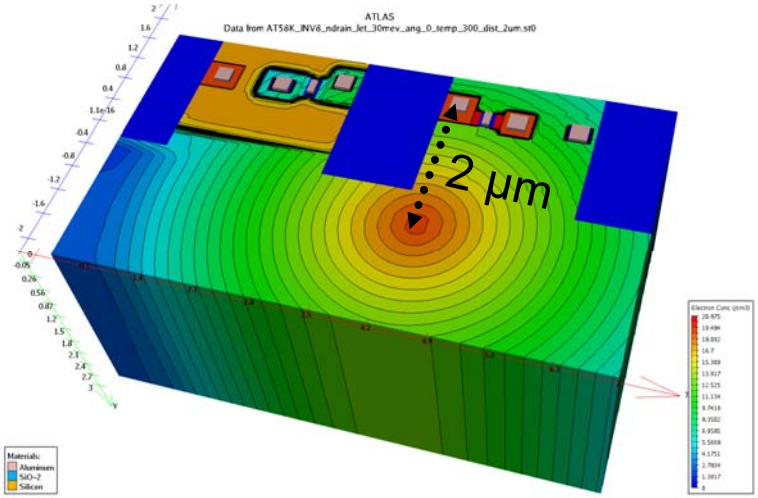


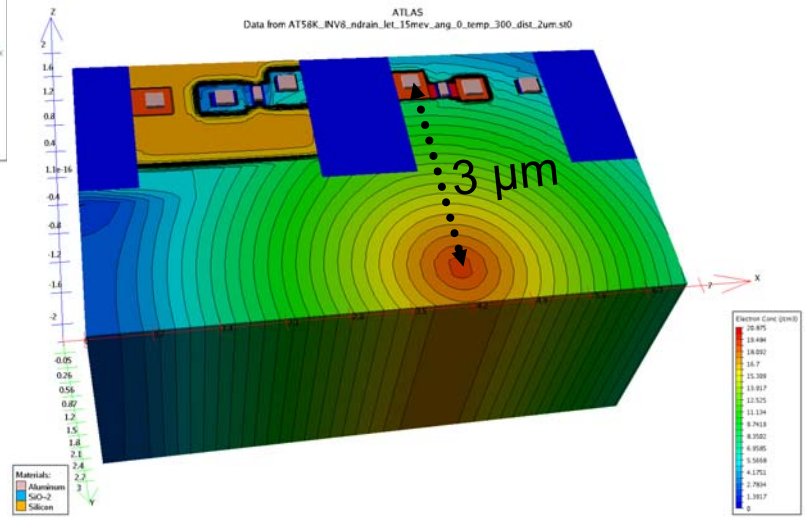
: The most sensitive area

: Heavy-ion impact

Heavy ion impact

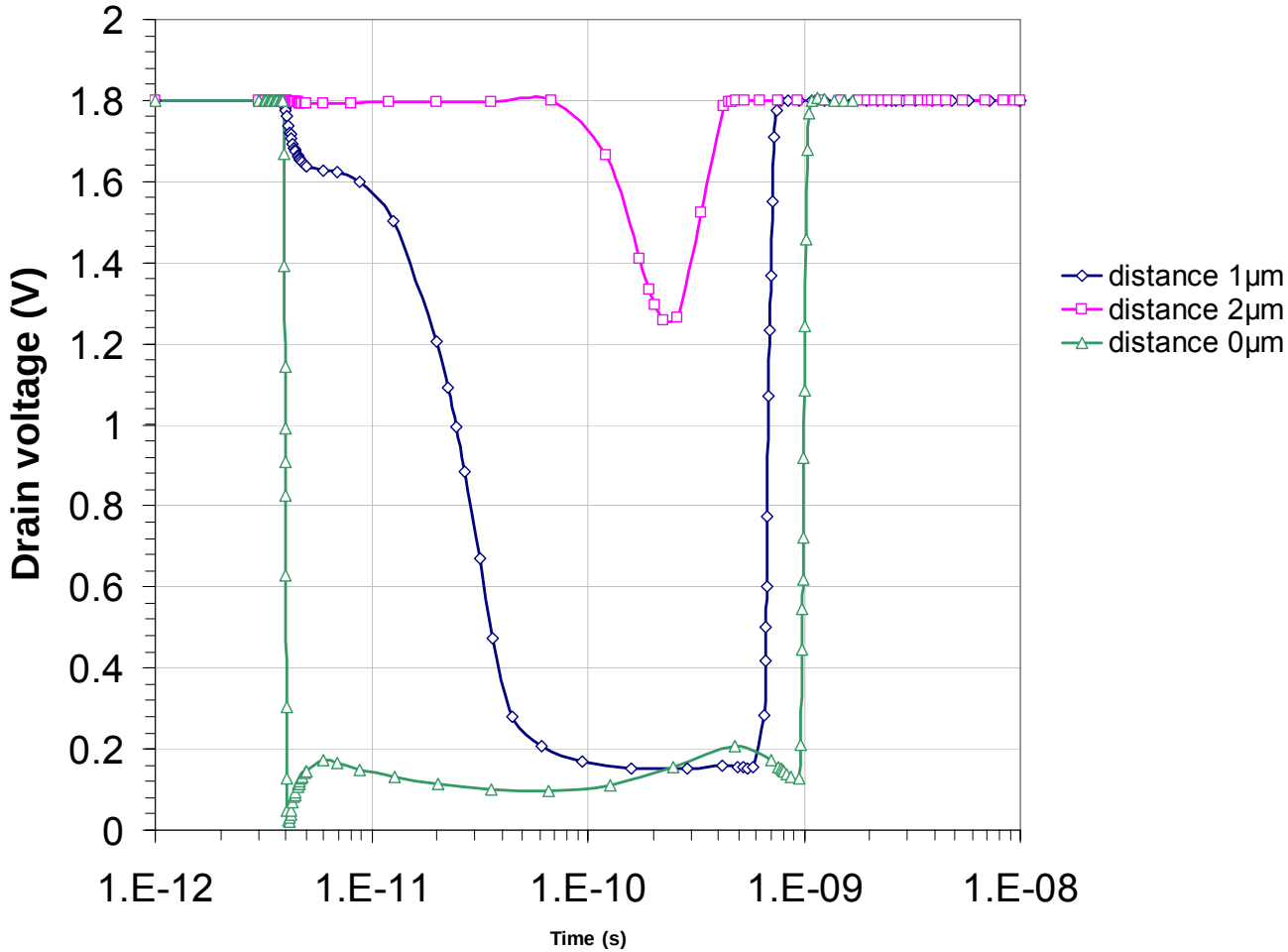






Example of location impact influence

- **LET = 30 MeV/mg/cm2**



3D simulation results - summary

- **For a given LET value, when the distance increases:**
  - **The current magnitude and duration decrease**
  - **The voltage magnitude and duration decrease**
  - **Moreover, both current and voltage pulse are delayed.**

- **No trivial law to assess V and I variation with the LET and the ion location**

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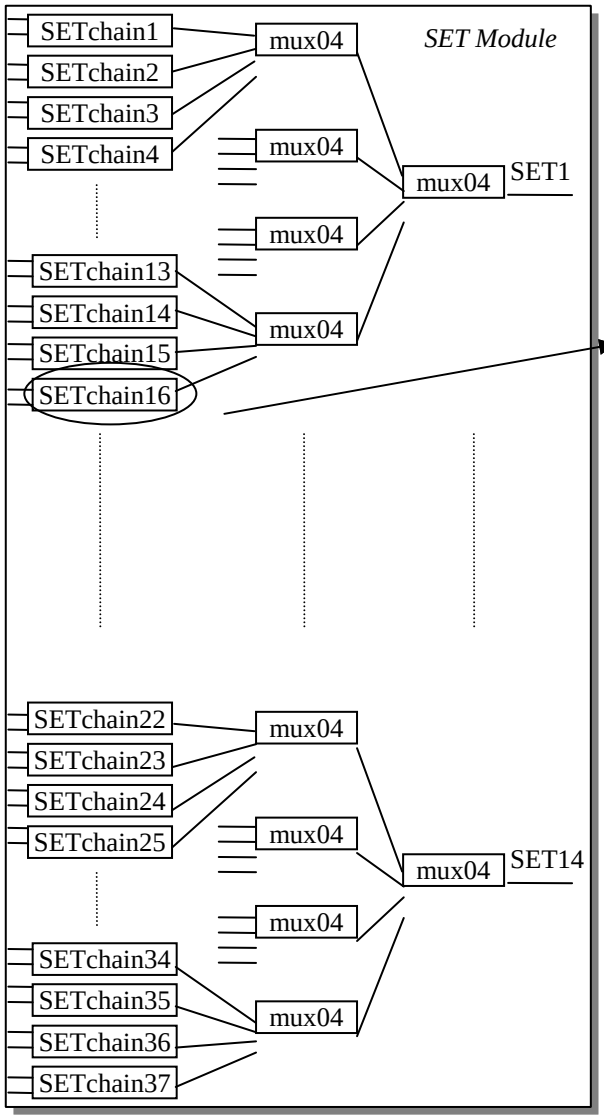
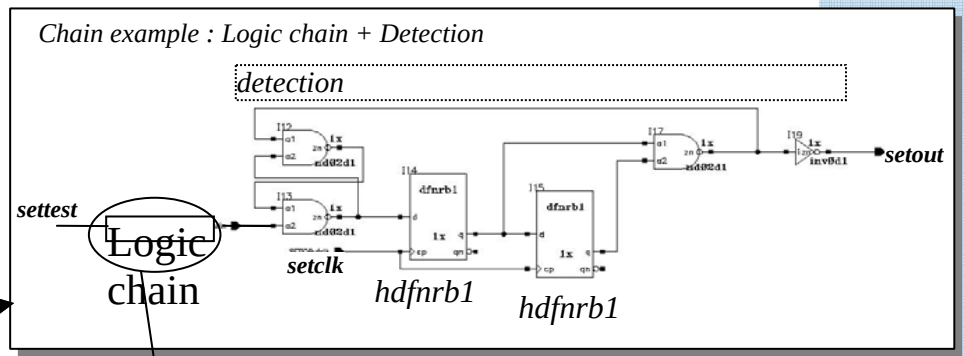
Overview of V42 SET test vehicle

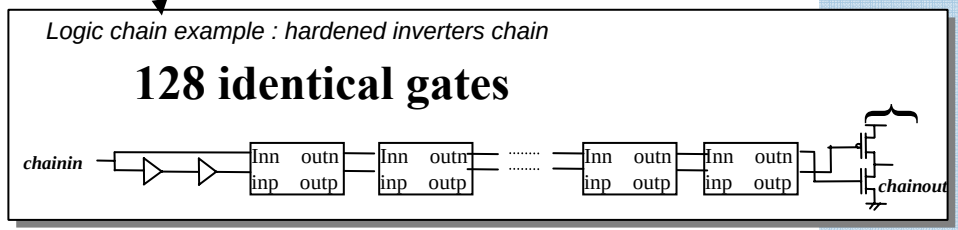
- **A statistical block**
  - **Count the number of SET events**
  - **Chains of different combinatorial cells**
  - **Chains of shift registers**
  - **Includes different mitigation techniques**
- **A characterisation block**
  - **Three methods to measure the SET pulse width**
  - **Chains of different combinatorial cells**
- **An SRAM 8kx8 bit**
  - **Well-known behavior under radiation**
- **A PLL**
- **Specification : “ATC18RHA V42 test chip” – V1.3**

V42 – Statistical block - SET Module



222 chains



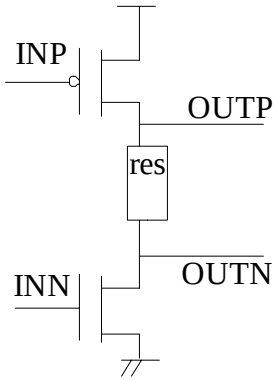


- The logic chain is made of ***128*** identical gates. All glitches induced in this chain are propagated to an asynchronous detector.
- Each chain is duplicated ***6*** times to have an area large enough to capture significant events.
- Different cases of logic chains are implemented. Gates with different :
  - ~ *types*
  - ~ *drive outputs*
  - ~ *load outputs*
  - ~ *hardening methods*
  - ~ *topology*

V42 - SET module – mitigation techniques

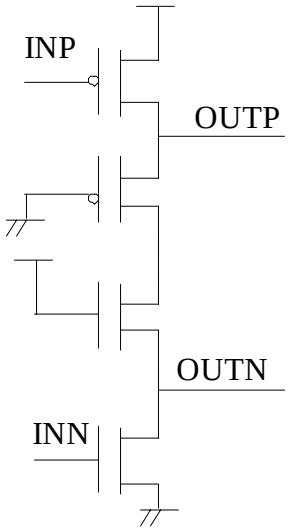
~ *Hardening Methods*

Resistive polysilicon



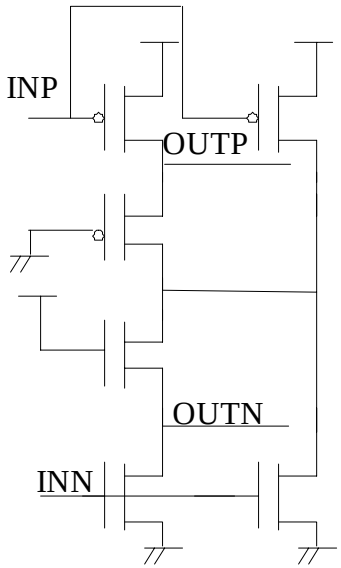
hresinv0d0
hresinv0d2
hresinv0d4
hresinv0d7
hresnd02d2
hresnd02d4
hresnd04d2
hresnd04d4
hresnr02d2
hresnr02d4
hresnr04d2
hresnr04d4
hresxr02d2
hresxr03d2

Isolation transistors



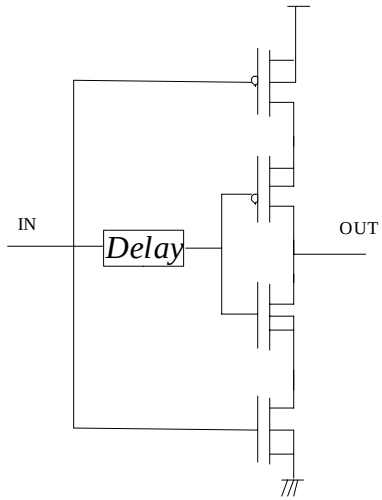
htrsinv0d0
htrsinv0d2
htrsinv0d4

Isolation and shunt transistors

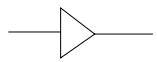


htrsfastinv0d2
htrsfastinv0d4

Tolerant and filtering inverter

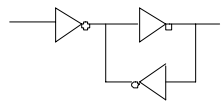


Delay1:Buffer



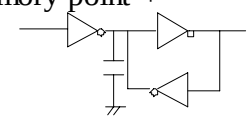
hdlyfinv0d2

Delay2:Memory point



h0finv0d2

Delay3:Memory point + capacitor



h54finv0d2

h9finv0d2

V42 – Statistical block - SET Module - cells

~ *Type of gate* (to test different diffusion areas sensitive to ion impact)

- inverters
- nand (2 or 4 inputs)
- nor (2 or 4 inputs)
- xor (2 or 3 inputs)

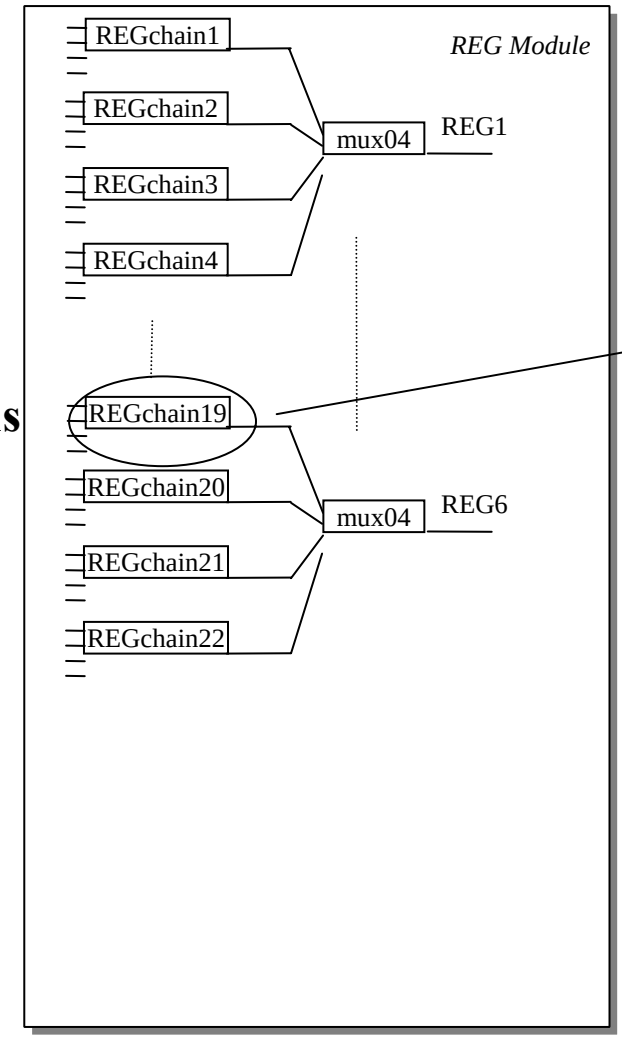
~ *Output drive* (an increasing output drive leads to less sensitivity to ion impact)
From 0 to 7 according to the gate.

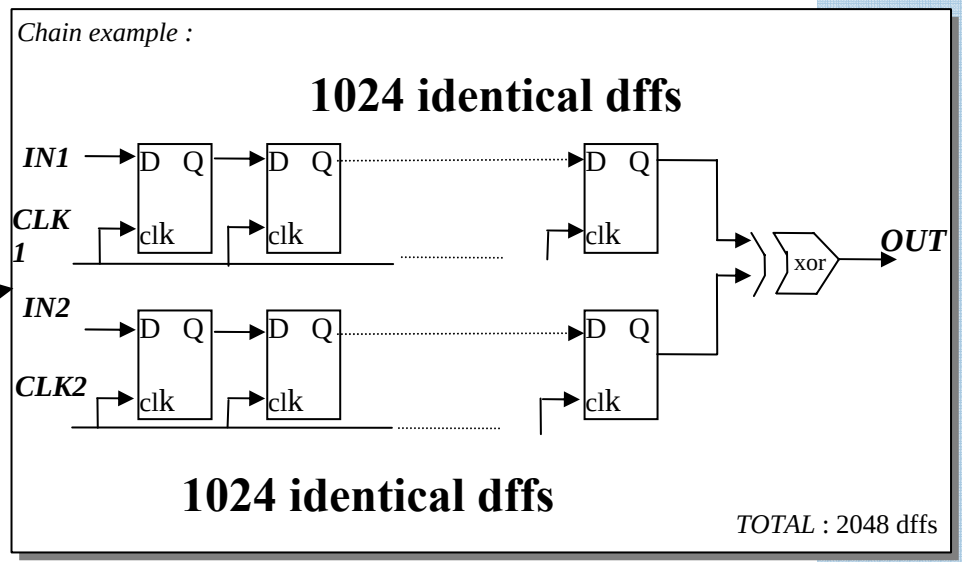
~ *Output load* (an important load leads to less sensitivity to ion impact)
1 for each gate and 4 for several of them.
(minimum 1x is the gate loaded by the following one, maximum 4x is the gate loaded by the following one + 3 identical in parallel).

~ *Topology*
an inverter has been designed with 2 different layouts - *splittrsinv0d2*

V42 – Statistical block - REG Module

22 chains





- Each chain is made of two identical subchains with a XOR to compare their outputs

=>if an upset occurs, in one flip-flop then the XOR OUT will be pulsed.

- ***22*** chains of ***1024*** stages each are implemented with various cases :

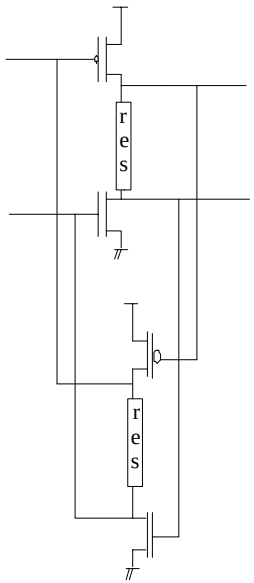
~ *different D flip-flops types*

~ *different hardening methods*

V42 - REG Module – Hardening techniques

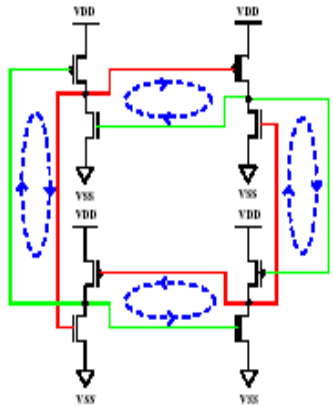
Hardening methods:

Resistive polysilicon



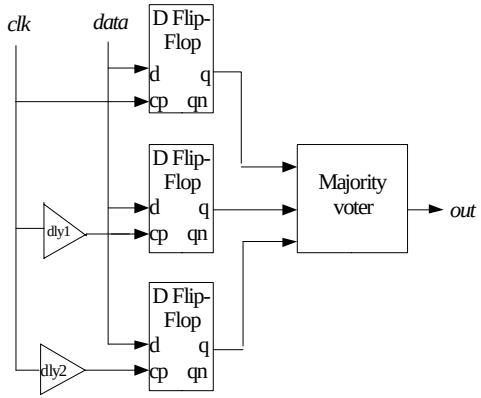
hresdfnrb1
hressdcrb1
hressdnrb1
hressdprb1

Dual Inter-locked Storage Cell (DICE)



hdfnrb1
hsdcrb1
hsdnrb1
hsdprb1

Triple Modular Redundancy (TMR)



Two different layouts are tested :
- D flip-flops are far from each other to avoid unexpected simultaneous activation (soft method)
- D flip-flops are close in a same block (hard method)

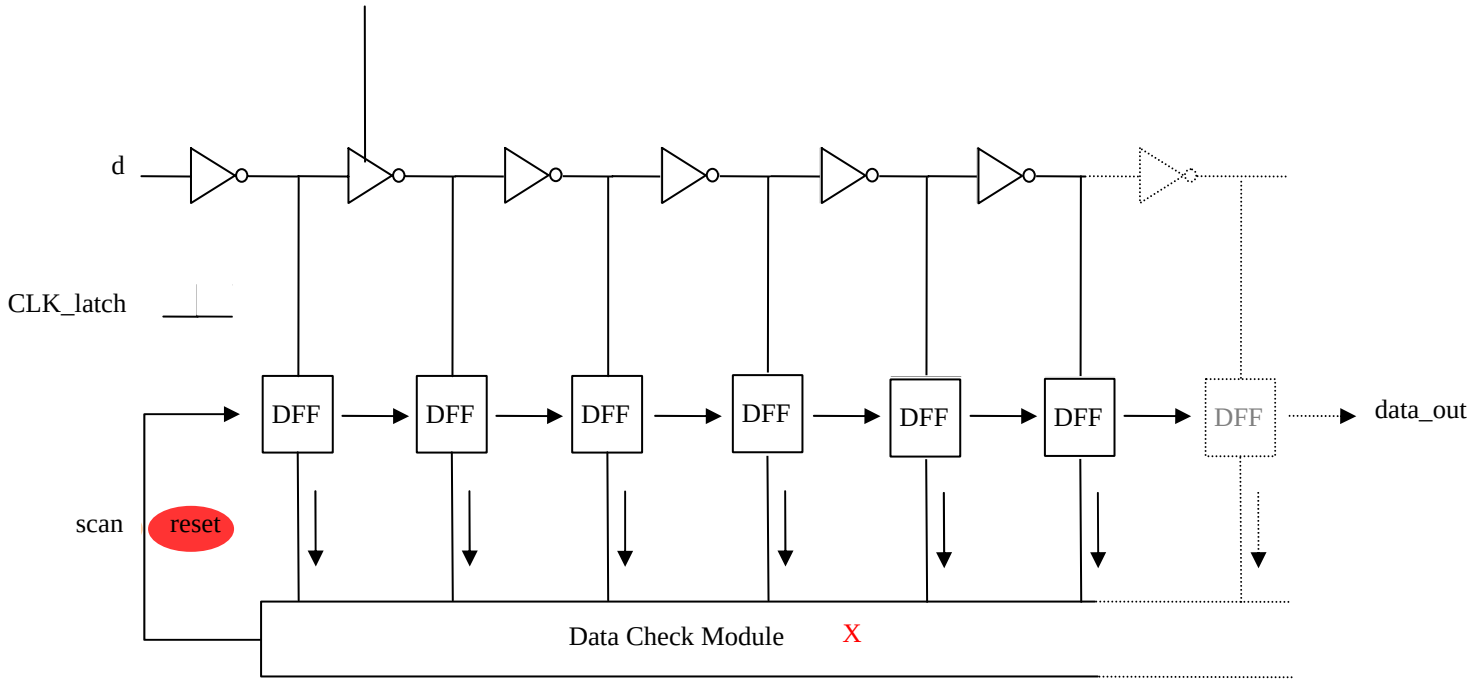
dfnrb1_x3
sdcrb1_x3
sdnrb1_x3
sdprb1_x3

=> For each layout, 2 modes :
- no delay between the different channels
- possible delays between the different channels

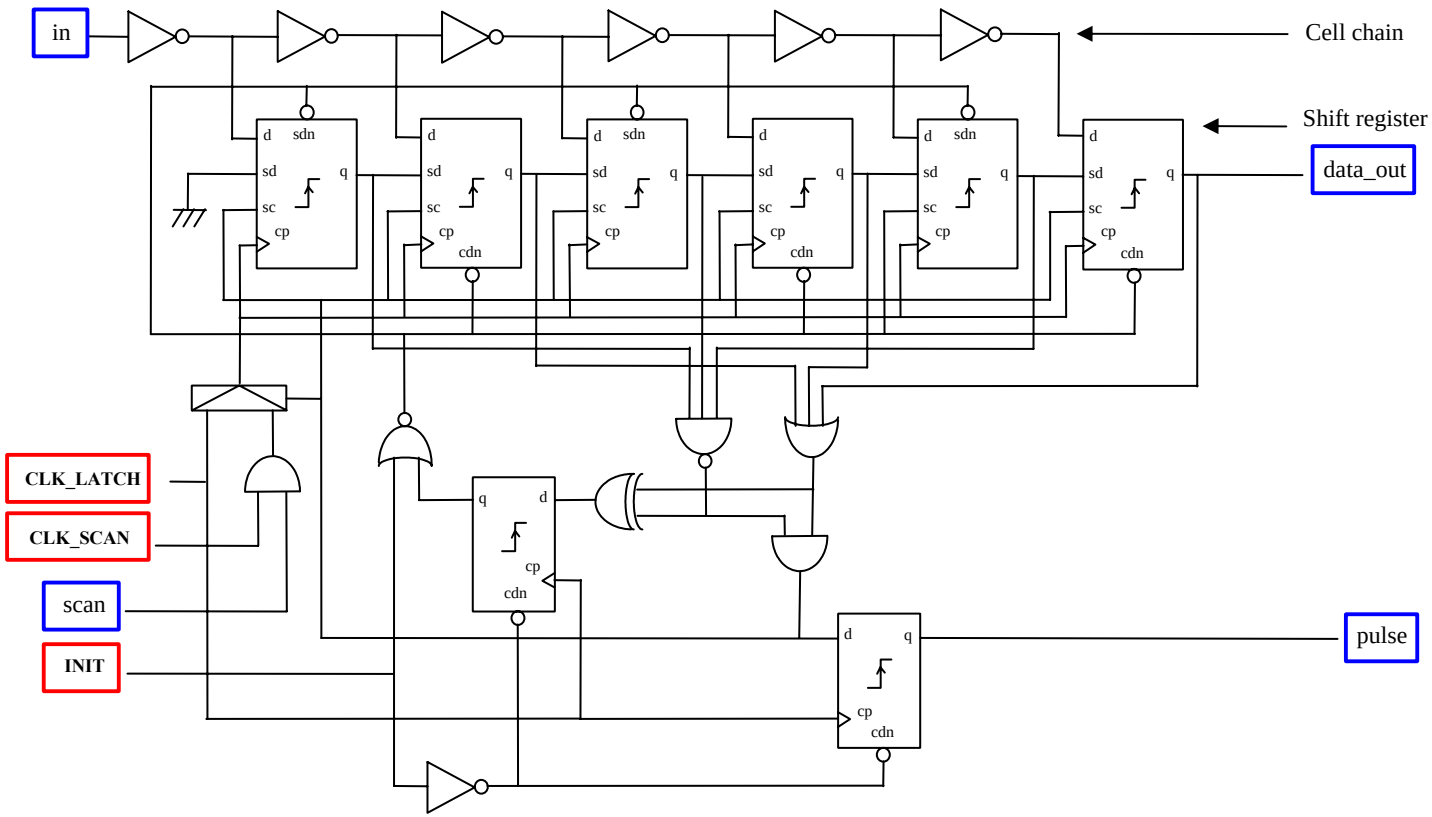
Characterization block

- **SET pulse width measurement methods**
  - periodical capture
  - capture on event

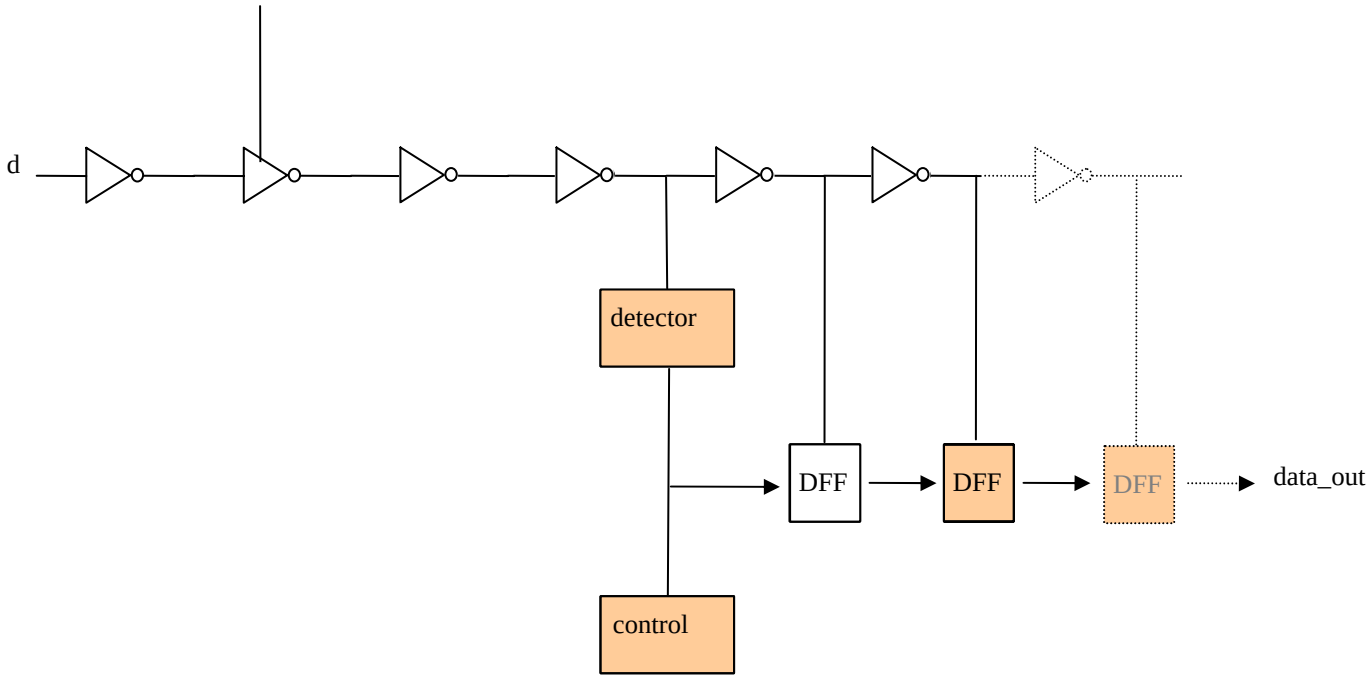
Charact. block - Periodical capture



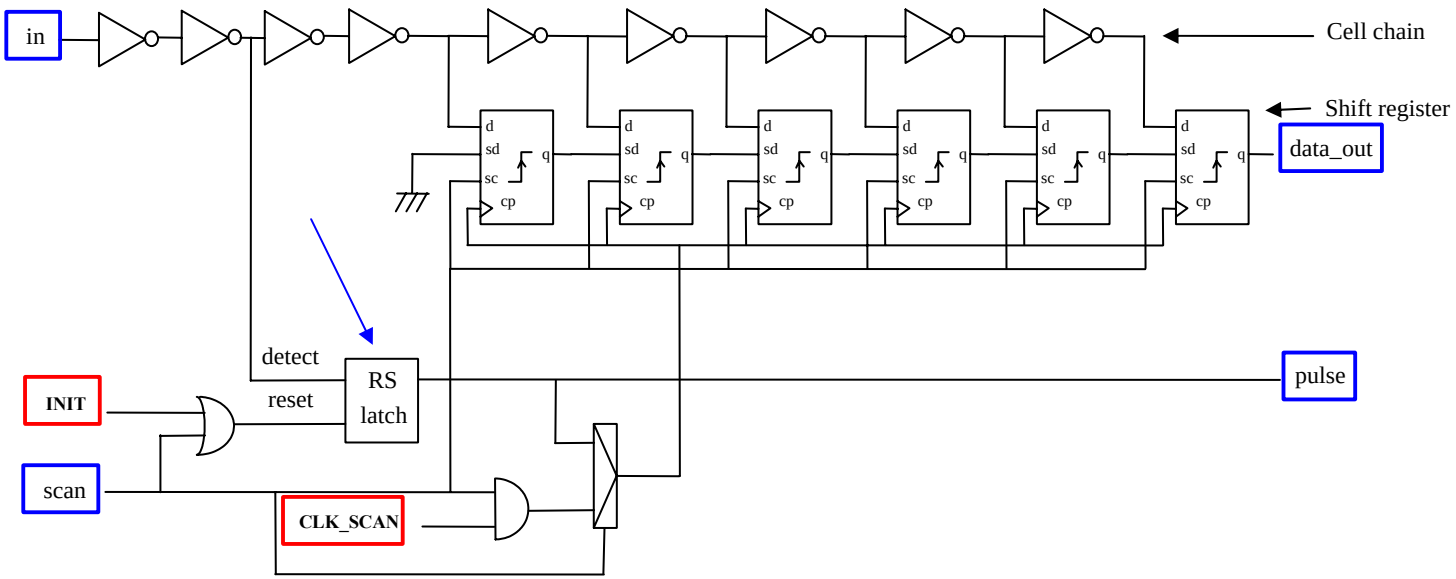
Periodical capture - details



Charact. Block – capture on event



Capture on event - details



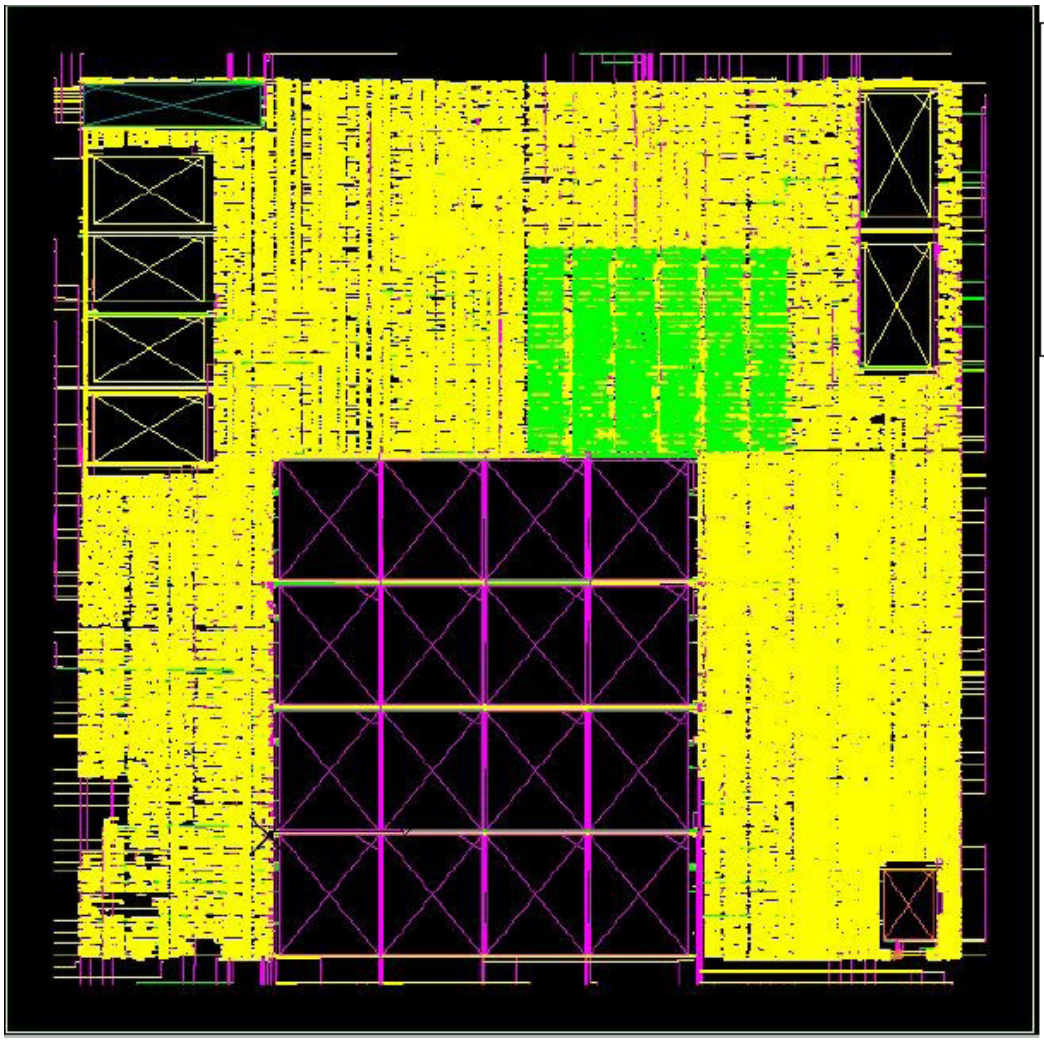
Charact. Block - cells

Cells

invbd2	drive x2 balanced inverter
Invbd2 (C_L=50fF)	drive x2 balanced inverter with 50fF load capacitance
invbd4	drive x4 balanced inverter
Invbd4 (C_L=50fF)	drive x4 balanced inverter with 50fF load capacitance
nd04d1	drive x1 4 inputs NAND
nd04d4	drive x4 4 inputs NAND
nr04d1	drive x1 4 inputs NOR
nr04d4	drive x4 4 inputs NOR
inv0d1	drive x1 inverter
inv0d4	drive x4 inverter
xr02d1	drive x1 2 inputs XOR
xr02d4	drive x4 2 inputs XOR

64 cells per chain, 16 chains per cell type

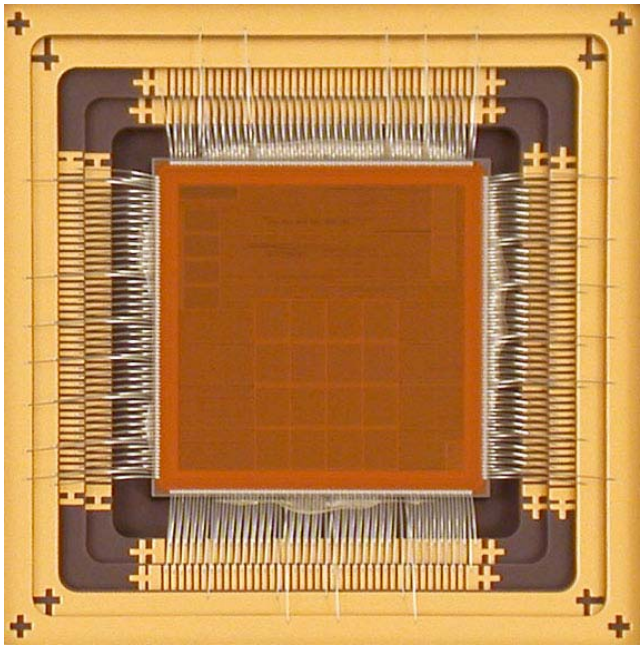
V42 floorplan



- *CHARACTERIZATION - Charac instance*
- *MITIGATION - Shift registers*
- *MITIGATION - set*
- *MEMORY*
- *PLL*

Die size : 8.625 x 8.625 = 74.4 mm^2

V42 die and package



V42 electrical characterisation

- **Functional tests on each part**
- **Electrical parameters**
- **For pulse width measurement : precise measurement of the propagation time for each cell**

Cells	1 cell (pS) (1)	1 Cell+% (pS) (2)
invbd2	49.22	45.04
invbd2 (C_L)	112.81	105.24
invbd4	45.78	41.44
invbd4 (C_L)	82.03	76.79
nd04d1	107.19	97.10
nd0404	170.62	162.67
nr04d1	153.75	140.19
nr04d4	195.47	189.76
inv0d1	57.03	53.13
inv0d4	40.00	36.56
xr02d1	141.09	143.24
xr02d4	185.94	188.26

(1) : from measurement
(2) : from design simulations

- **Report : "ATC18RHA V42 test chip – electrical test report"**

Agenda

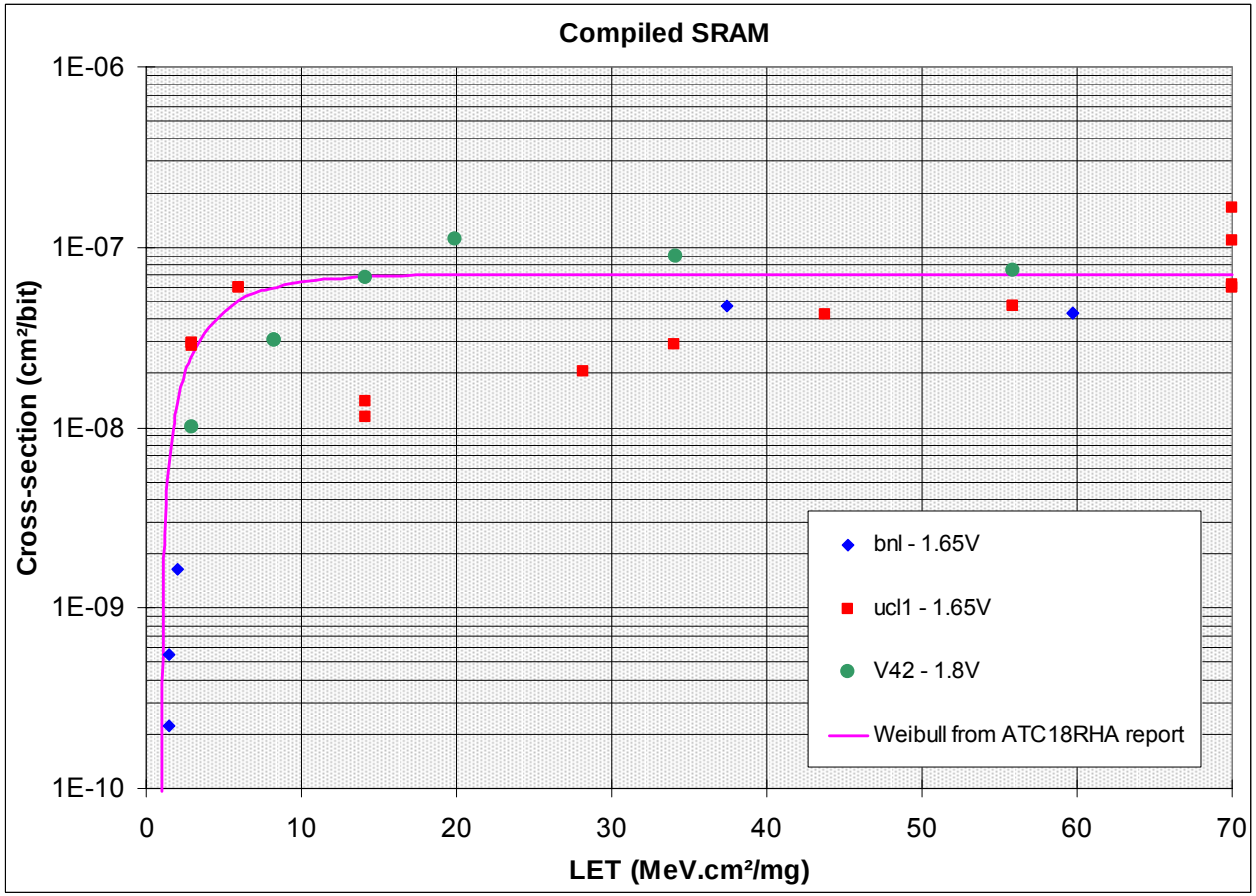
- Context and objectives of this study
- 3D simulations
- V42 SET test vehicle content
- Heavy ions test results
- Protons test results
- Correlation between simulations and test results
- Design recommendations

Some testing issues

- **SEE tester subcontracted to TRAD (Toulouse, France)**
- **First SEE test done end of March 2007**
  - **Problem with the TRAD tester, long to analyse**
- **Debugging on the TRAD tester done in June 07 at UCL**
- **Heavy ions test campaign done end of August 2007**
  - **Problem with the beam (fluence counting, part destroyed by UCL member…)**
  - **Short analysis done, showed the tester and parts were OK**
- **Heavy ions test campaign done the 3rd of October 2007**
  - **Successful, test plan nearly completely performed !**

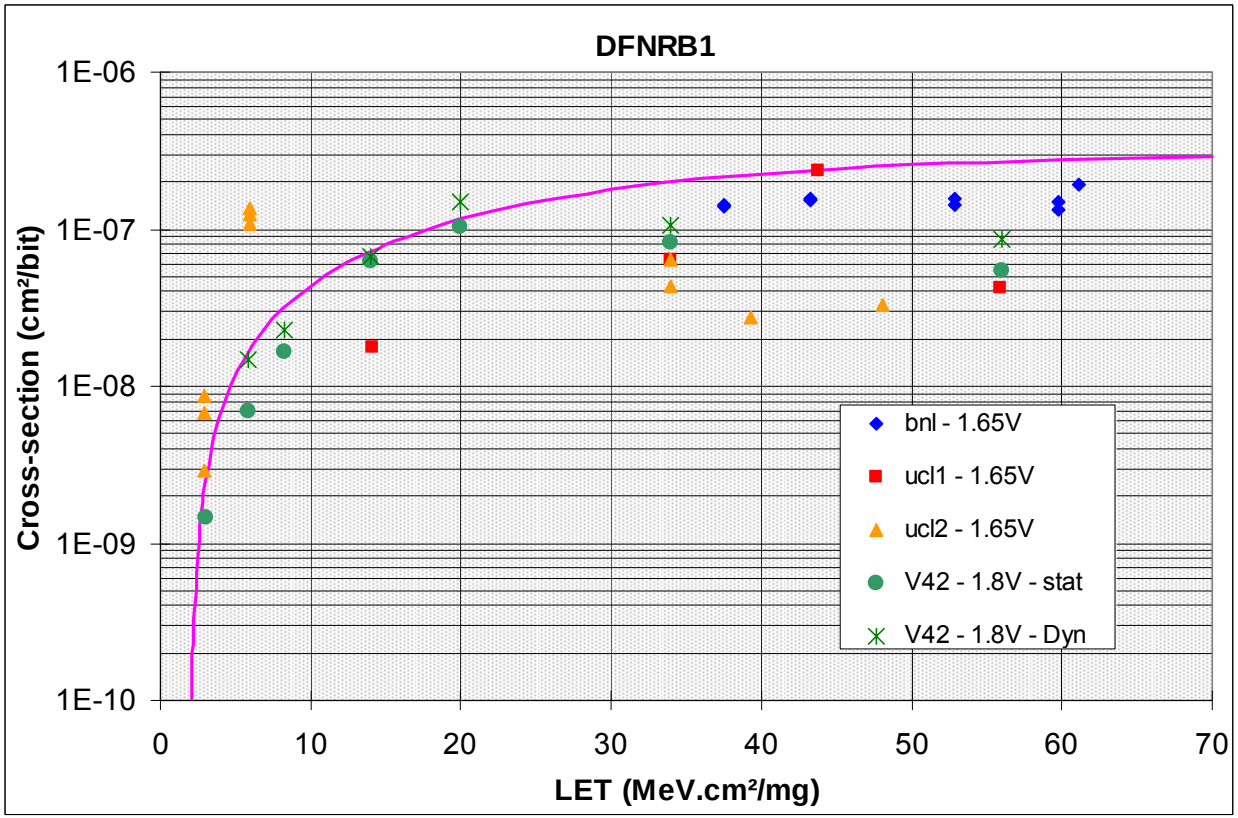
Heavy ions test - SRAM

- **Cross section**



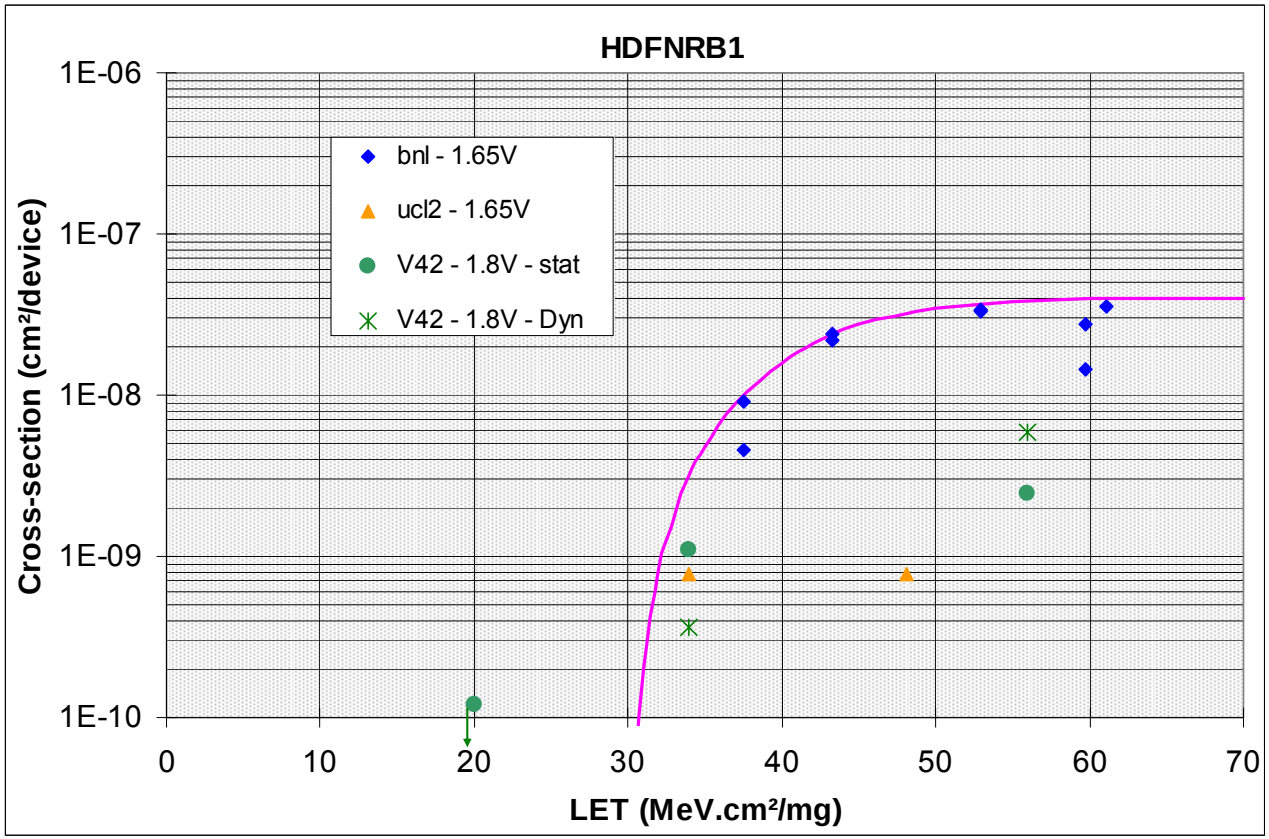
Heavy ions test – Standard Flip-Flops

- **Cross section**



Heavy ions test – SEU-Hardened Flip-Flops

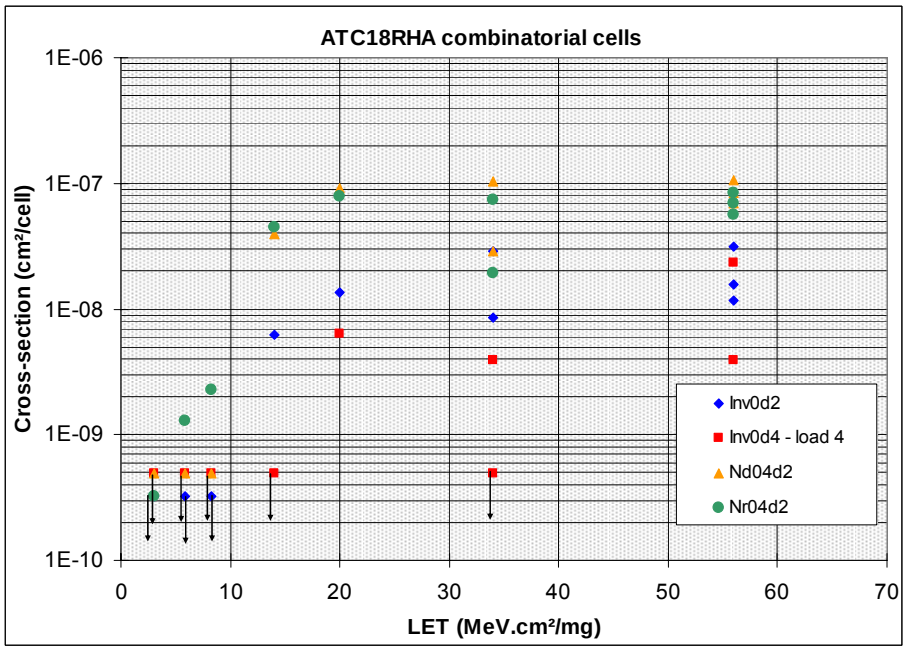
- **Cross section**

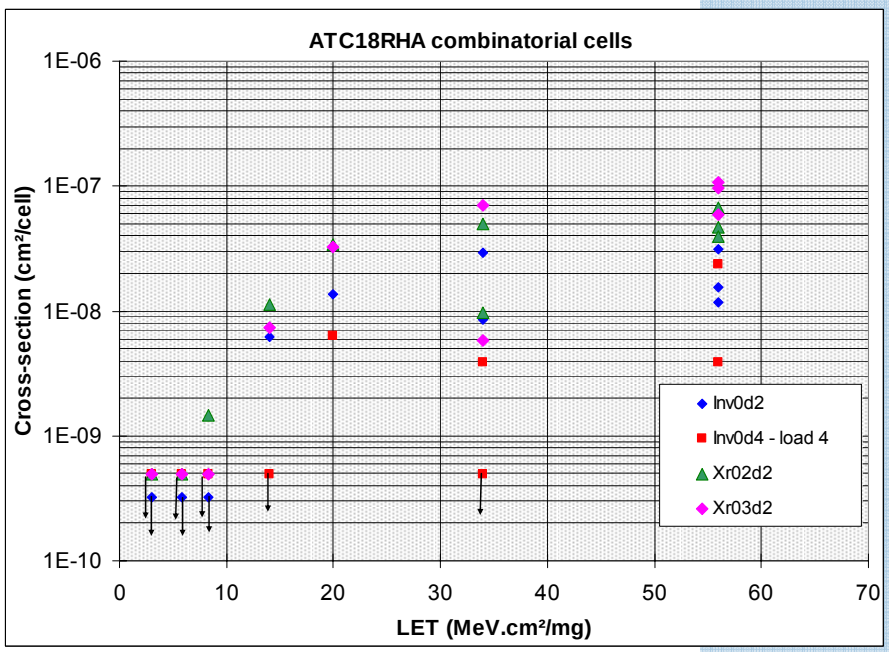


Heavy ions test – Flips-flops

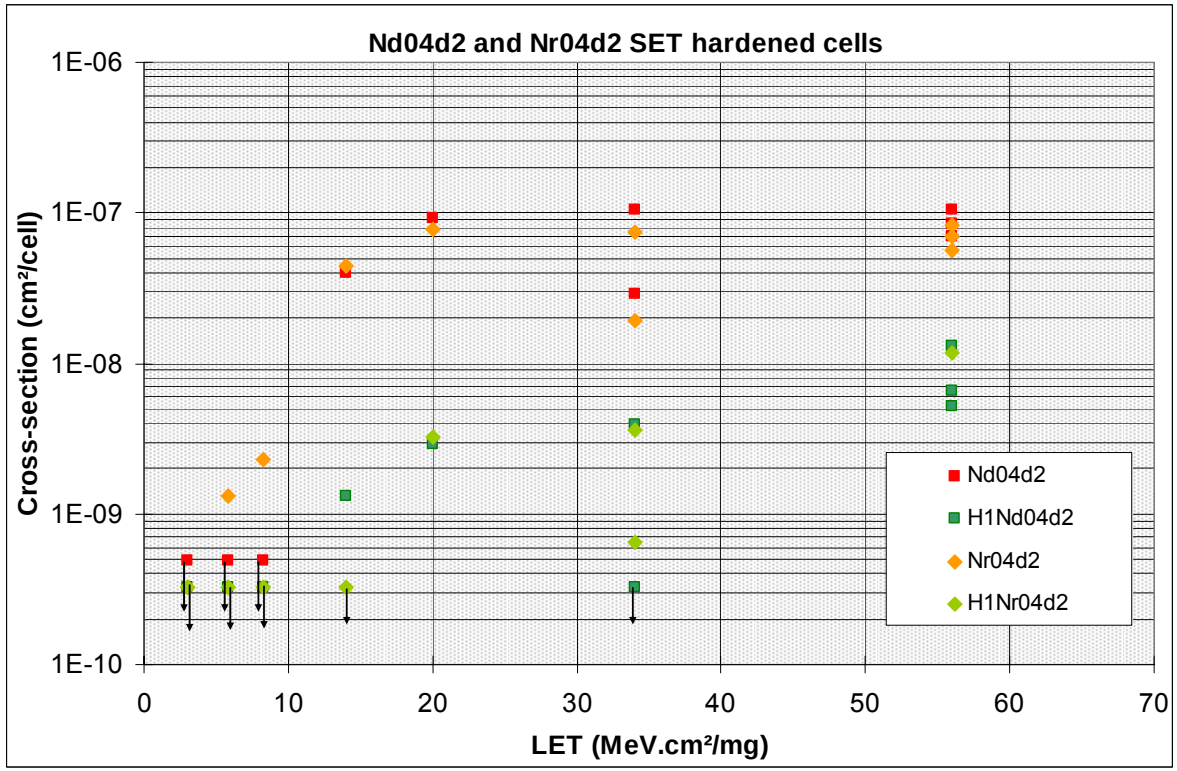
- **Confirmation of the low SEE sensitivity of TMR**
  - **Better than SEU-H FF in term of SEU mitigation**
- **Good results of any of the hardening solutions proposed, for any kind of flip-flops tested**

SET events on statistical block



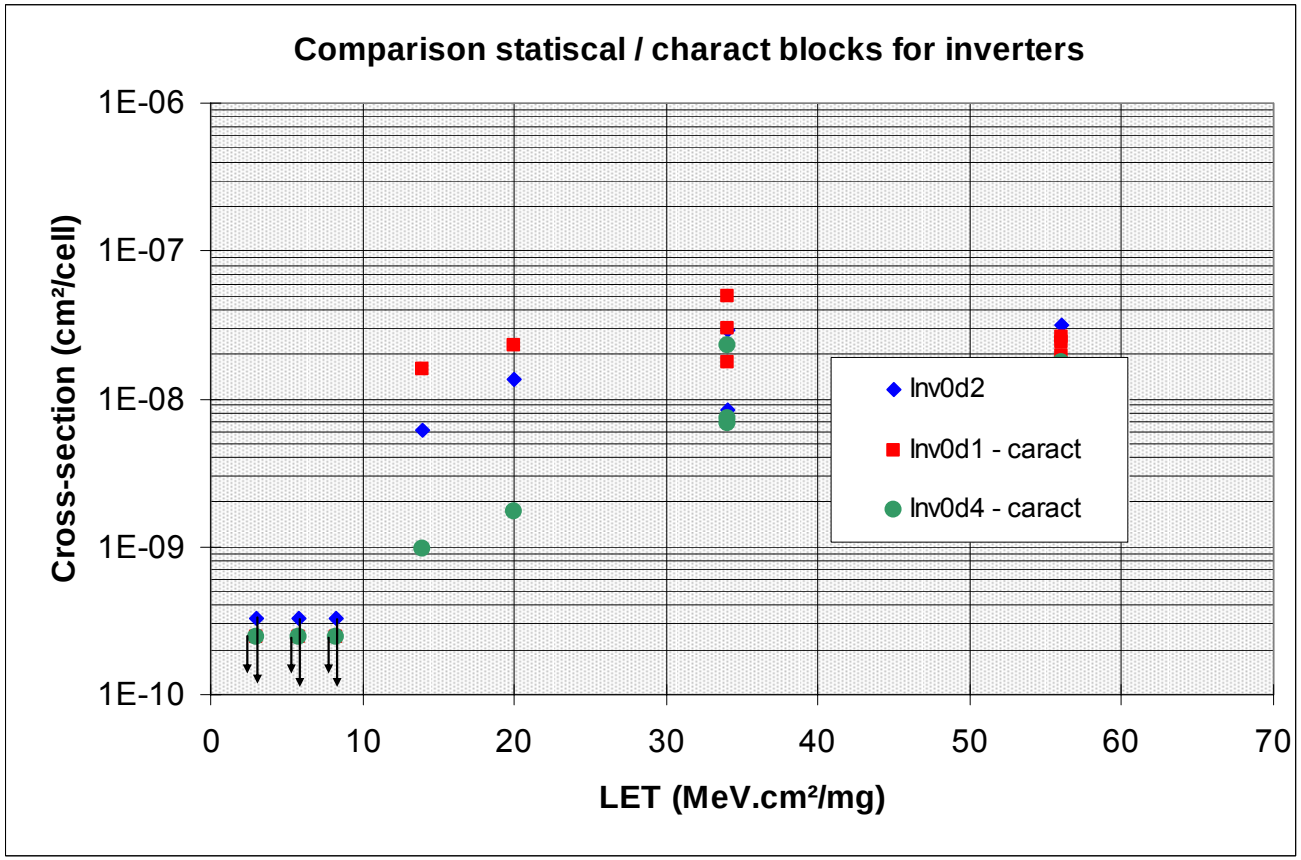


SET events on statistical block - mitigation

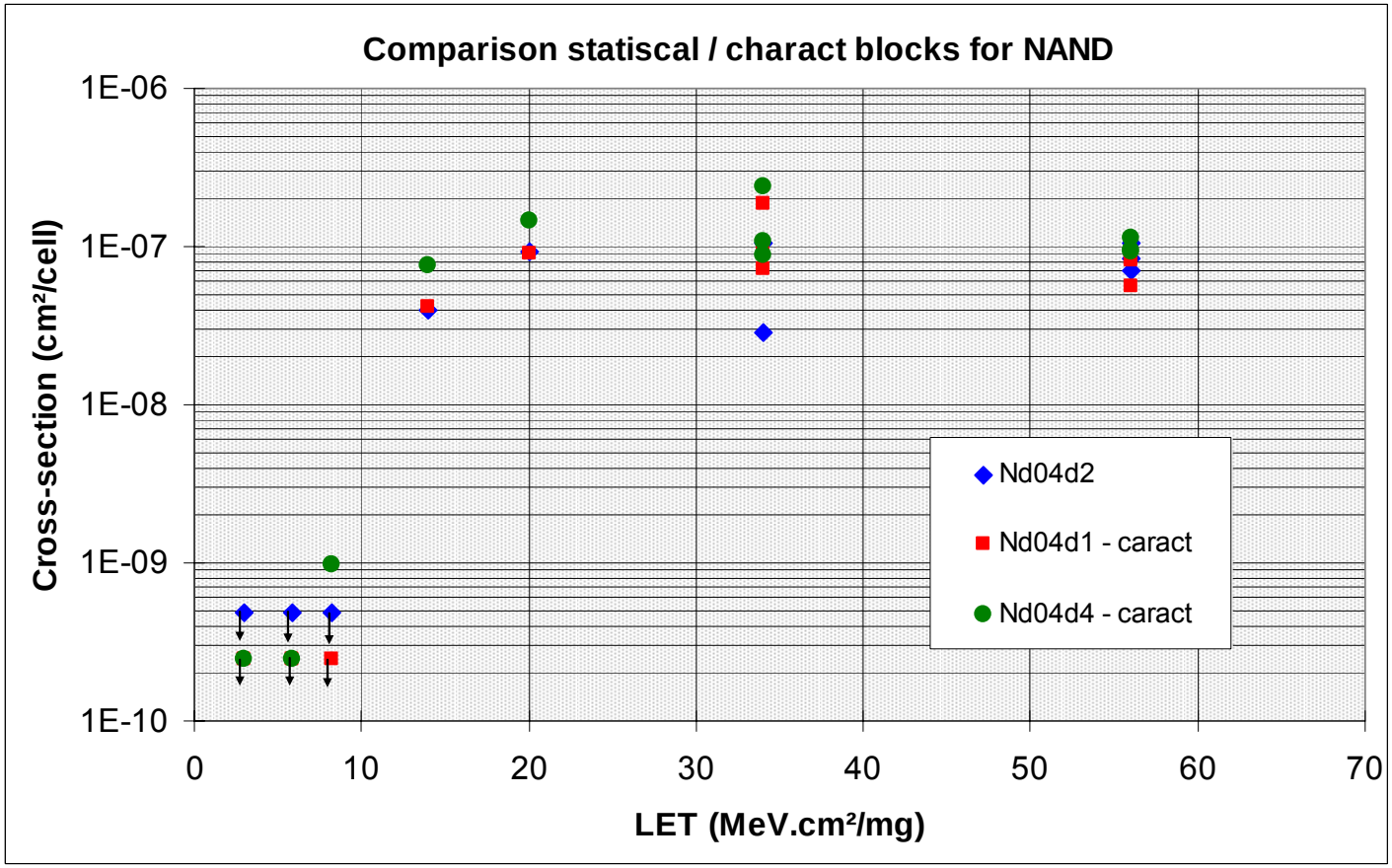


- **three of the SET hardening solutions are very efficient**
  - **use of double input/double output cells with different resistive/isolation paths**

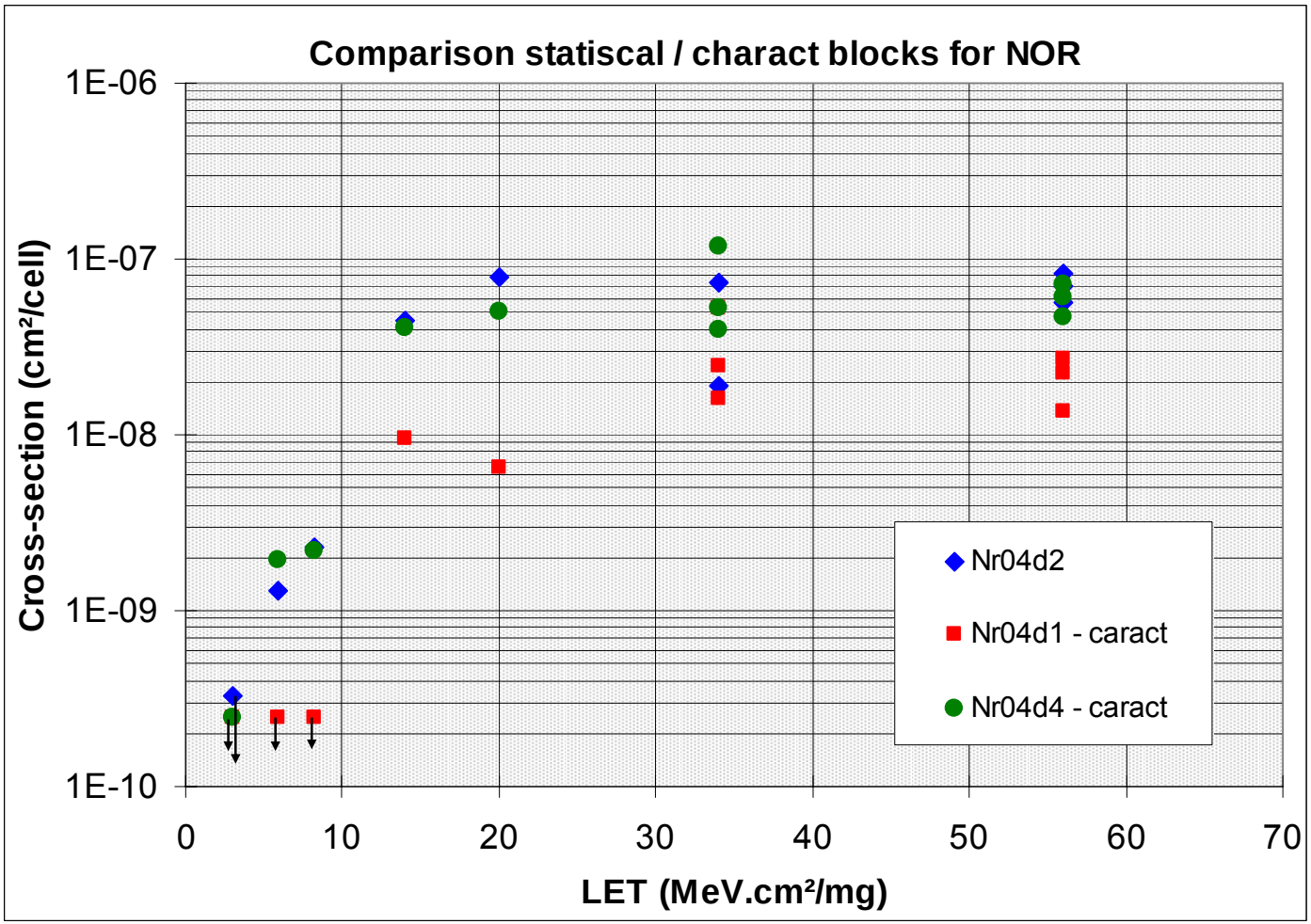
SET events - characterization block - inv



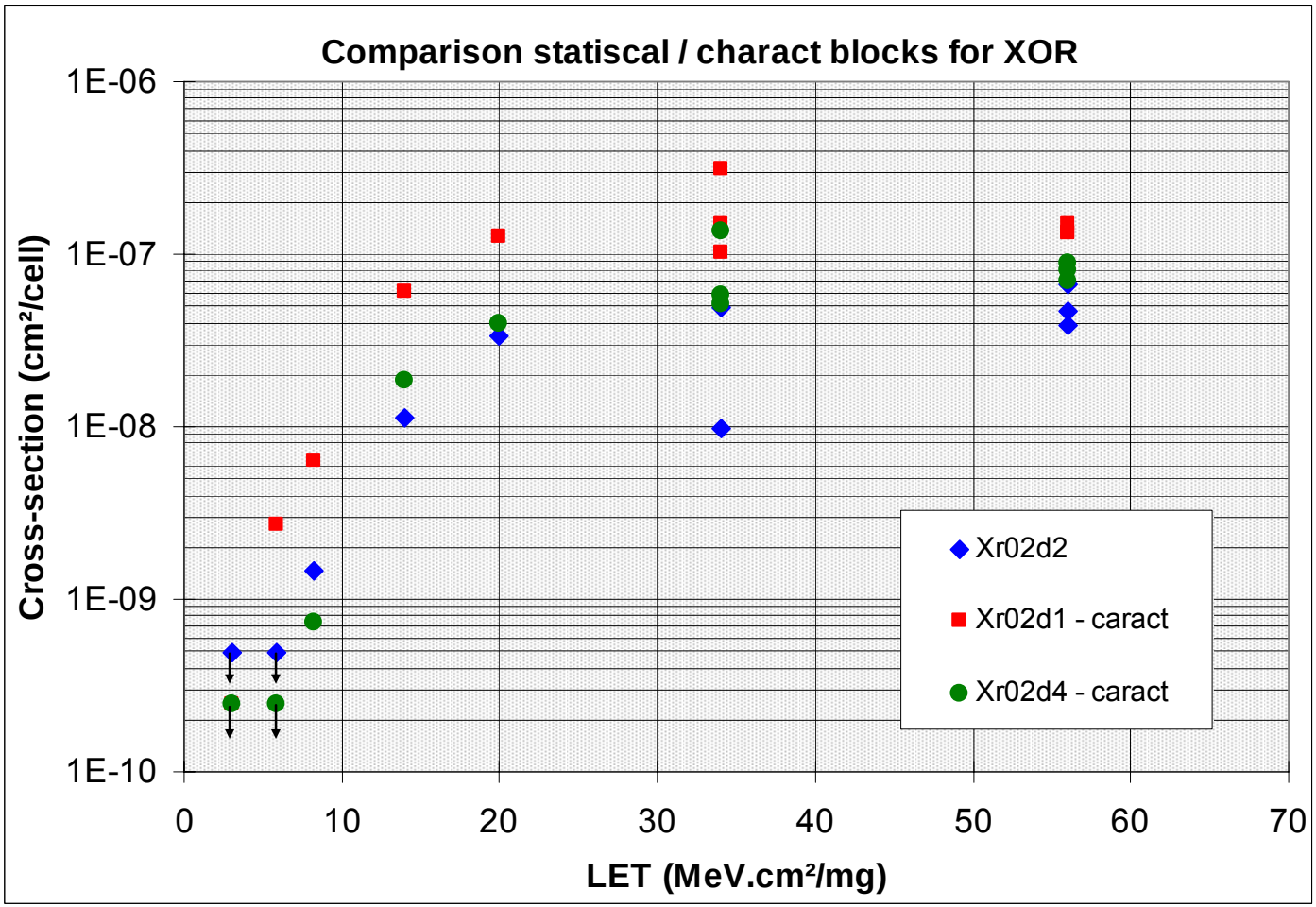
SET events - characterization block - nand



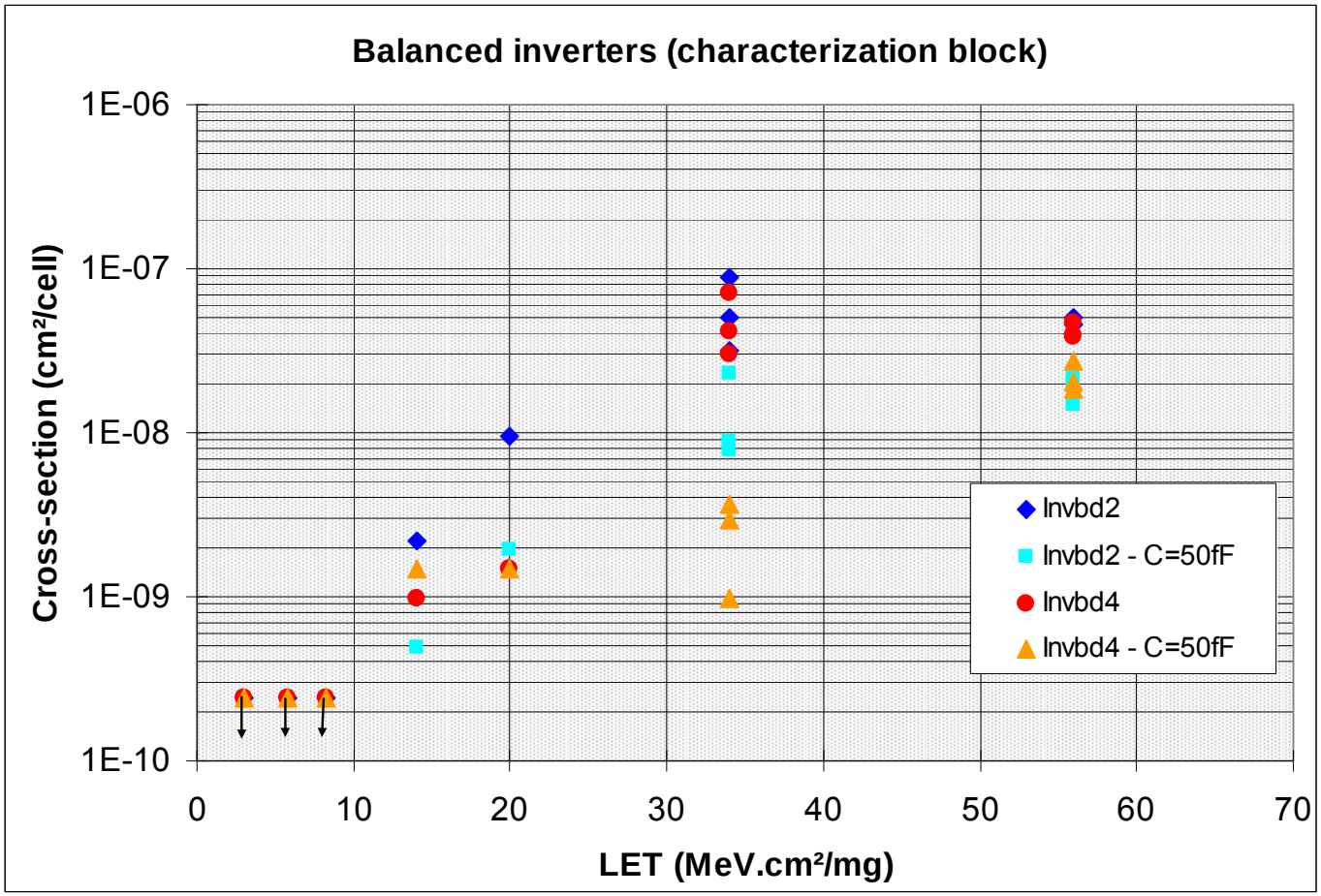
SET events - characterization block - nor



SET events - characterization block - xor

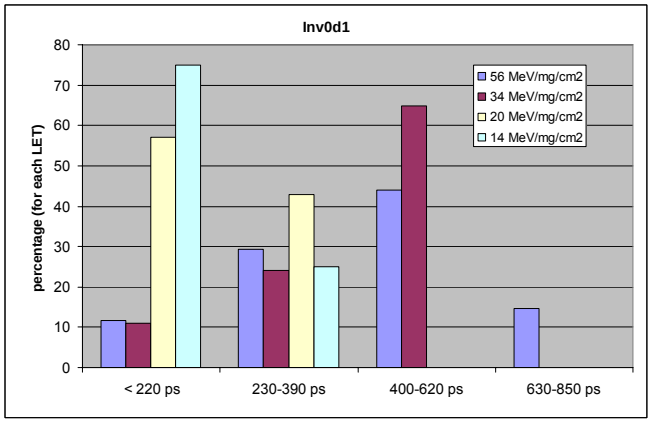


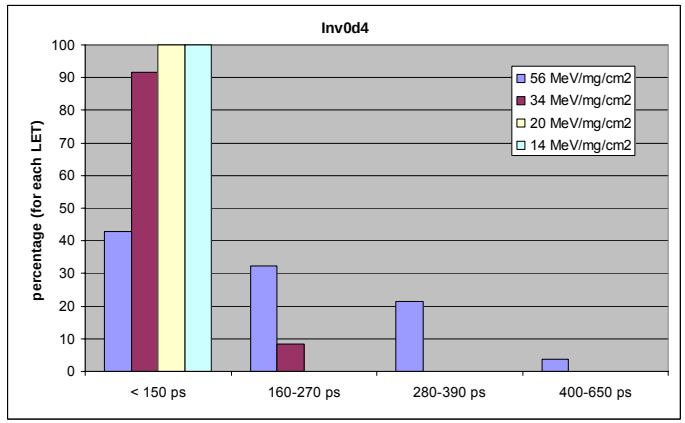
SET events - characterization block - invb

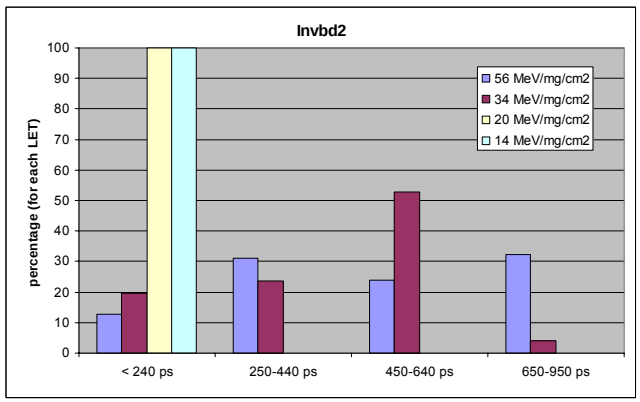


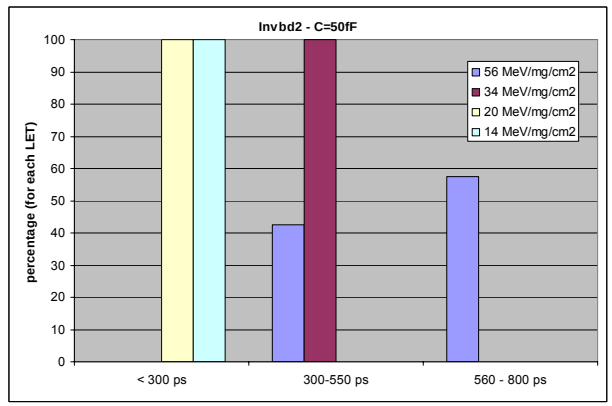
SET pulse width measurement

- **Measurement based on the number of cells**
  - **Multiple of propagation time of each cell**
  - **Inv0d1, inv0d4, invb2, invbd2 with C=50fF**



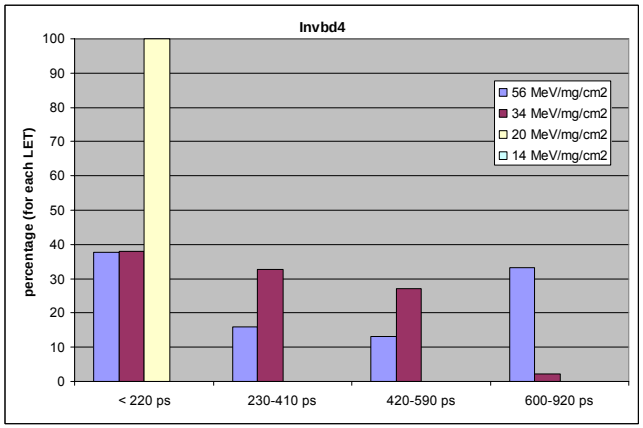


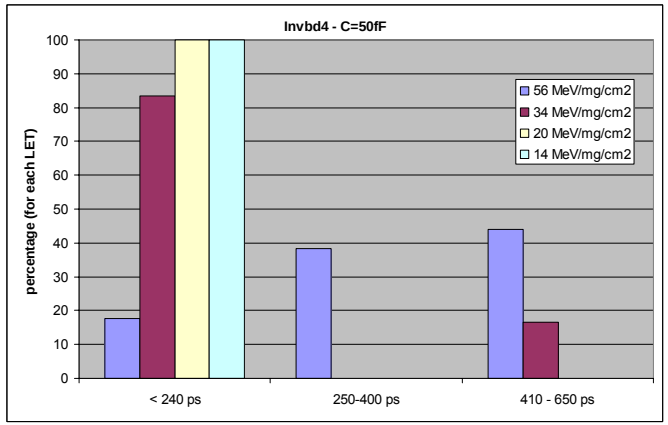


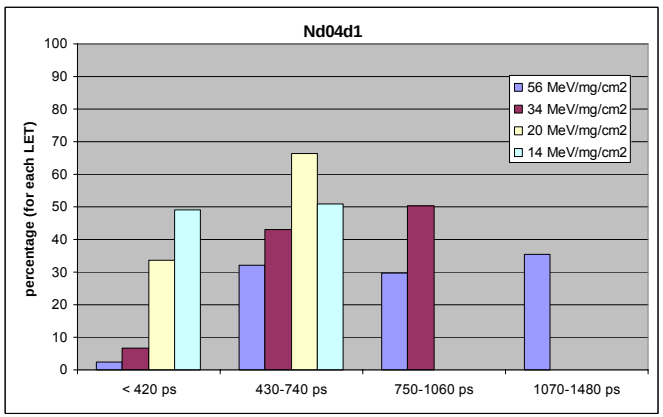


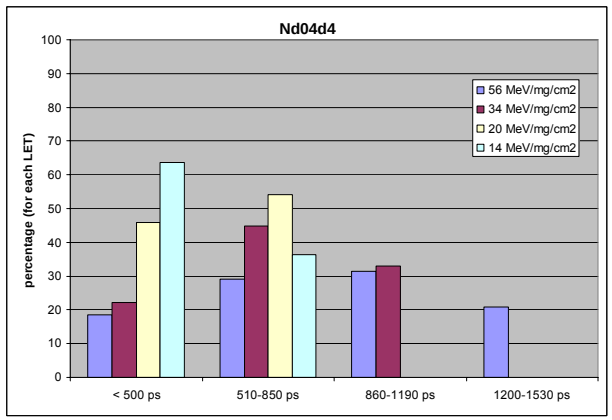
SET pulse width measurement (2)

- **Invb4, invbd4 with C=50fF, Nd04d1, Nd04d4**



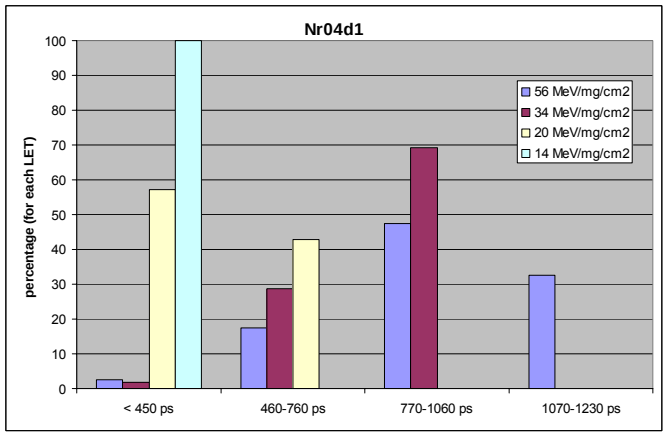


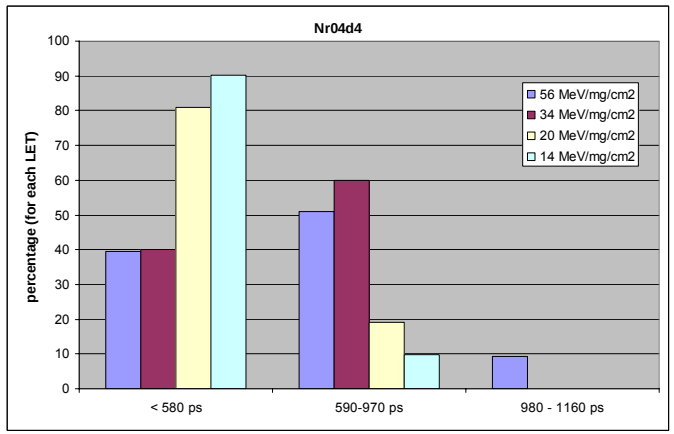


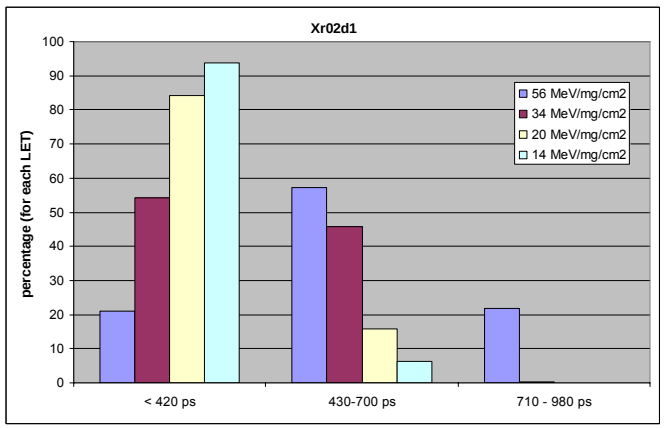


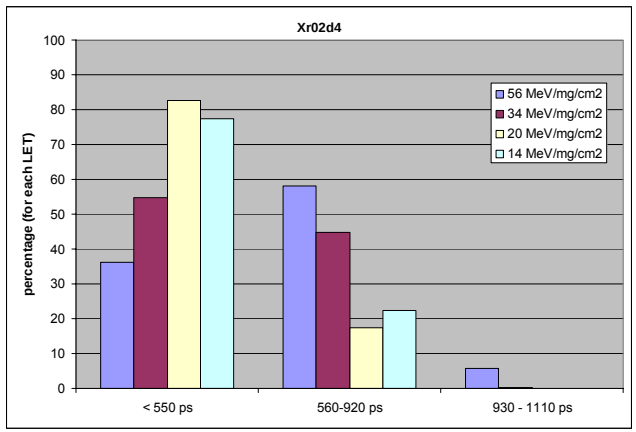
SET pulse width measurement (3)

- **Nr04d1, Nr04d4, xr02d1, xr02d4**









- **For all cells : strong decrease of SET pulse width when LET decreases**

“SET event” rate in space

- **Cross sections and Weibull parameters derived from each cell tested in V42**
- **“SET event” rate can be calculated using CREME96**

block	cell	GEO	LEO 1000km-53°	LEO 852km-98°	LEO 600km-98°	LEO 450km-51°
Statistic	NHL1Inv0d2	2.98E+05	4.45E+04	9.67E+04	3.15E+05	5.65E+05
Statistic	NHNd04d2	2.98E+04	5.41E+03	1.18E+04	3.60E+04	6.74E+04
Statistic	NHNr04d2	1.96E+04	3.19E+03	6.93E+03	2.17E+04	3.91E+04
Statistic	NHInv0d4 (load4)	8.83E+05	4.58E+05	8.35E+05	2.11E+06	5.48E+06
Statistic	NHXr02d2	7.82E+04	1.35E+04	2.95E+04	9.34E+04	1.63E+05
Statistic	NHXr03d2	6.22E+04	1.50E+04	3.08E+04	9.13E+04	1.69E+05
Statistic	H1Nd04d2	1.37E+06	1.36E+05	2.98E+05	1.03E+06	1.71E+06
Statistic	H1Nr04d2	1.37E+06	1.24E+05	2.82E+05	9.57E+05	1.61E+06
Caract	invbd2	3.11E+05	1.16E+05	2.30E+05	6.22E+05	1.35E+06
Caract	invbd2 (C=50fF)	1.61E+06	6.84E+05	1.28E+06	3.34E+06	7.91E+06
Caract	invbd4	3.60E+05	7.51E+04	1.62E+05	4.80E+05	8.92E+05
Caract	invbd4 (C=50fF)	9.44E+05	2.45E+05	4.95E+05	1.46E+06	2.85E+06
Caract	nd04d1	3.34E+04	6.29E+03	1.36E+04	4.15E+04	7.58E+04
Caract	nd04d4	1.83E+04	3.81E+03	8.12E+03	2.44E+04	4.53E+04
Caract	nr04d1	2.28E+05	2.47E+04	5.69E+04	1.84E+05	3.22E+05
Caract	nr04d4	3.08E+04	4.52E+03	9.67E+03	3.15E+04	5.53E+04
Caract	inv0d1	1.37E+05	1.30E+04	2.95E+04	9.92E+04	1.72E+05
Caract	inv0d4	1.44E+06	2.46E+05	5.40E+05	1.67E+06	3.10E+06
Caract	xr02d1	1.30E+04	2.26E+03	5.03E+03	1.51E+04	2.79E+04
Caract	xr02d4	5.17E+04	1.13E+04	2.42E+04	7.02E+04	1.32E+05

Other elements

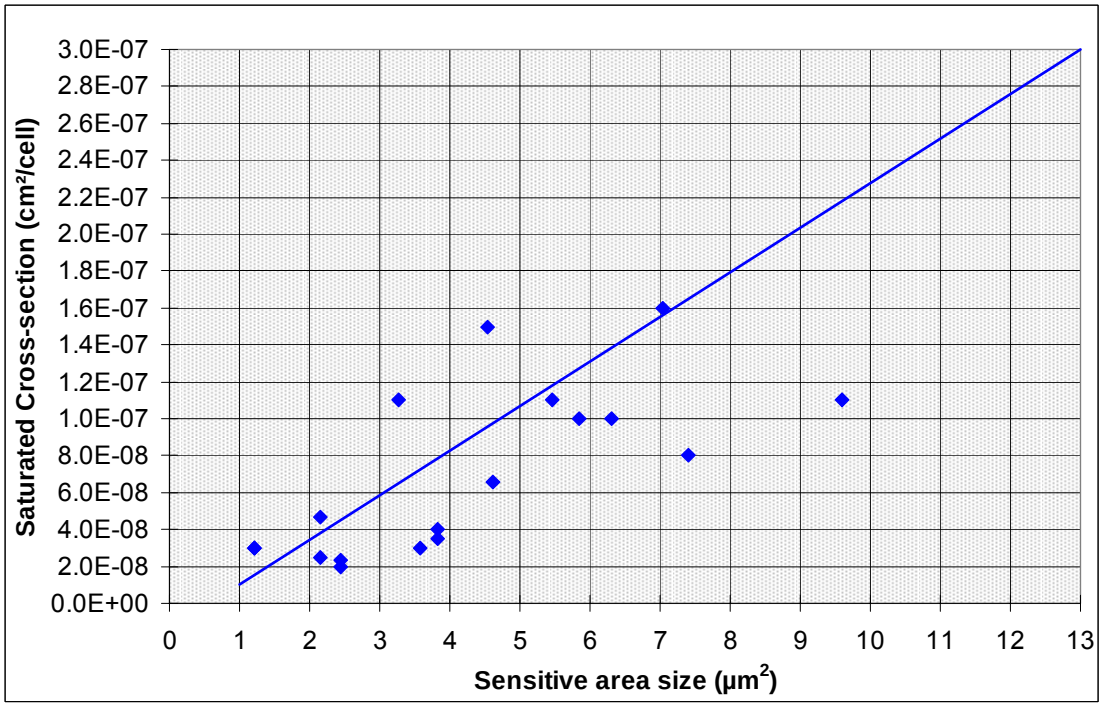
- **Previous calculation is a worst case :**
- **Influence of the pulse width**

min pulse width (ps)	clock	data	set	clear
standard FF	100	150	100	70
SEU hardened FF	200	350	100	70

- **SET pulse attenuation or filtering**
- **SET removed by the logic equation**
- **On the data path, need clock to propagate an error**
- **An SET error may not propagate at the application level (refreshment before the data is used)**

Extension to other ATC18RHA cells

- **Not an easy task**
- **First approximation : use of the sensitive area**



- **Does not take into account drive or multi-collection**
- **The plotted line allows to derive an “SET event” rate for any cell**

Agenda

- Context and objectives of this study
- 3D simulations
- V42 SET test vehicle content
- Heavy ions test results
- Protons test results
- Correlation between simulations and test results
- Design recommandations

V42 Protons test

- **Performed the 12/11/2007 at KVI (the Netherlands)**
  - **Some problems with the beam (unstable)**
- **Same tester than for heavy ions (TRAD)**
  - **Some cabling issues (long to discover)**
- **Test runs**

Run	Product	SN	Temp (°C)	Board & tester used	VCC [V] Core / IO	Energy [MeV]	Flux [p/s,cm²]	Fluence [p/cm²]	Run Time [s]	SET	REG stat	REG dyn	Charact.	SRAM
1	V42	#5	25°C	TRAD	1.8V / 3.3V	140	2.30E+08	2.00E+11	876	nt	18	nt	nt	368
2	V42	#5	25°C	TRAD	1.8V / 3.3V	140	2.50E+08	2.00E+11	796	nt	nt	13	nt	nt
3	V42	#5	25°C	TRAD	1.8V / 3.3V	140	2.50E+08	3.00E+11	1223	0	nt	nt	nt	nt
4	V42	#6	25°C	TRAD	1.8V / 3.3V	140	2.50E+08	2.00E+11	817	nt	18	nt	nt	340
5	V42	#6	25°C	TRAD	1.8V / 3.3V	140	3.70E+08	8.00E+11	2161	nt	nt	nt	8	nt
6	V42	#6	25°C	TRAD	1.8V / 3.3V	100	4.80E+08	5.00E+11	1043	nt	nt	nt	4	nt

Protons SEU test results - SRAM

SRAM

Run	Part	Proton Energy (MeV)	Total events SEUs	Cross section SEU events (cm^2/bit)
1	5	**140**	368	2.8E-14
4	6	**140**	340	2.6E-14

- **Previous ATC18RHA test**
  - **At 140 MeV : between 2.4 and 2.8E-14 cm2/bit**

Protons test results - DFF

- **Static (left) and dynamic (right) mode**

		Part 5		Part 6	
		Run N°1 (140 MeV)	Cross Section (cm²/bit)	Run N°4 (140 MeV)	Cross Section (cm²/bit)
CELL TYPE	**Dfnrb1**	**4**	**9.8E-15**	**8**	**1.9E-14**
	H2dfnrb1	0	< 2.4 E-15	0	< 2.4 E-15
	H1dfnrb1	0	< 2.4 E-15	0	< 2.4 E-15
	DFNRB1_X3	0	< 2.4 E-15	0	< 2.4 E-15
	dfnrb1_TMR2	0	< 2.4 E-15	0	< 2.4 E-15
	dfsrd02psli_RH	0	< 2.4 E-15	0	< 2.4 E-15
	sdcrb1	**4**	**9.8E-15**	**5**	**1.2E-14**
	H2sdcrb1	0	< 2.4 E-15	0	< 2.4 E-15
	H1sdcrb1	0	< 2.4 E-15	0	< 2.4 E-15
	sdcrb1_x3	0	< 2.4 E-15	0	< 2.4 E-15
	sdcrb1_TMR2	0	< 2.4 E-15	0	< 2.4 E-15
	Dfsrd02psli_RH	0	< 2.4 E-15	0	< 2.4 E-15
	sdnrb1	**2**	**4.9E-15**	**1**	**2.4E-15**
	H2sdnrb1	0	< 2.4 E-15	0	< 2.4 E-15
	H1sdnrb1	0	< 2.4 E-15	0	< 2.4 E-15
	sdnrb1_x3	0	< 2.4 E-15	0	< 2.4 E-15
	sdnrb1_TMR2	0	< 2.4 E-15	0	< 2.4 E-15
	sdprb1	**7**	**1.7E-14**	**4**	**9.8E-15**
	H2sdprb1	**1**	**2.4E-15**	0	< 2.4 E-15
	H1sdprb1	0	< 2.4 E-15	0	< 2.4 E-15
	sdprb1_x3	0	< 2.4 E-15	0	< 2.4 E-15
	sdprb1_TMR2	0	< 2.4 E-15	0	< 2.4 E-15

		Run N°2 (140MeV)	Cross Section (cm²/bit)
CELL TYPE	**dfnrb1**	**5**	**1.2E-14**
	H2dfnrb1	0	< 2.4 E-15
	dfnrb1_x3	0	< 2.4 E-15
	dfnrb1_TMR2	0	< 2.4 E -15
	sdcrb1	**4**	**9.8E-15**
	H2sdcrb1	0	< 2.4 E-15
	sdcrb1_x3	0	< 2.4 E-15
	sdcrb1_TMR2	0	< 2.4 E -15
	sdnrb1	**3**	**7.3E-15**
	H2sdnrb1	0	< 2.4 E-15
	sdnrb1_x3	0	< 2.4 E-15
	sdnrb1_TMR2	0	< 2.4 E -15
	sdprb1	**1**	**2.4E-15**
	H2sdprb1	0	< 2.4 E-15
	sdprb1_x3	0	< 2.4 E-15
	sdprb1_TMR2	0	< 2.4 E -15

Previous ATC18RHA test :
Between 2 and 4 E-14 cm2/bit

Protons SET test results

- **Statistical block : one run at 3 E11 protons/cm2 at 140 MeV without any error at the output**
  - **Cross section below 6 E-15 cm2/cell at 140 MeV**

- **Characterization block**

	Run 5 140 MeV 8E11 Nb events	Cross section (cm2/cell)	Run 6 140 MeV 5 E11 Nb events	Cross section (cm2/cell)
invbd2	0	< 1.2 E-15	0	< 2 E-15
invbd2-C=50fF	0	< 1.2 E-15	0	< 2 E-15
invbd4	0	< 1.2 E-15	0	< 2 E-15
invbd4-=50fF	0	< 1.2 E-15	0	< 2 E-15
nd04d1	0	< 1.2 E-15	0	< 2 E-15
nd04d4	2	2.4 E-15	0	< 2 E-15
Nr04d1	0	< 1.2 E-15	0	< 2 E-15
Nr04d4	0	< 1.2 E-15	1	2 E-15
inv0d1	0	< 1.2 E-15	0	< 2 E-15
inv0d4	1	1.2 E-15	0	< 2 E-15
Xr02d1	0	< 1.2 E-15	3	6 E-15
Xr02d4	0	< 1.2 E-15	0	< 2 E-15

Among these SET pulses, at 100 MeV, the pulse duration is :
- nr04d4 : 1300 ps
- xr02d1 : 600 ps

Comparison with heavy ion tests

- **Protons measured cross sections 5 to 10 times below what could be predicted using the PROFIT method**
- **Possible explanations**
  - **limited precision on the LET threshold derived from the heavy ions SET test for the combinatorial cells**
  - **Applicability of the Profit method to SET**
- **“SET event” rates derived from the heavy ions test pessimistic**

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Comparison between 3D simulations and SET test results

- **Qualitatively, some good correlation**
  - **The SET pulse width increases with the LET**
  - **A higher drive decreases the SET pulse width**
- **Quantitatively, some important differences**

	LET (MeV.cm²/mg)	SET pulse widths (ps)
TCAD3D	15	110
V42 Tests	15	390
TCAD3D	35	280
V42 Tests	35	620

- **Some possible assumptions**
  - **Distance between struck transistor and the body tie**
  - **Load on the logical chains**
  - **Broadening of the SET pulse during propagation on long chains**
  - **Multiple collection**
  - **Modelling of the heavy ion track**

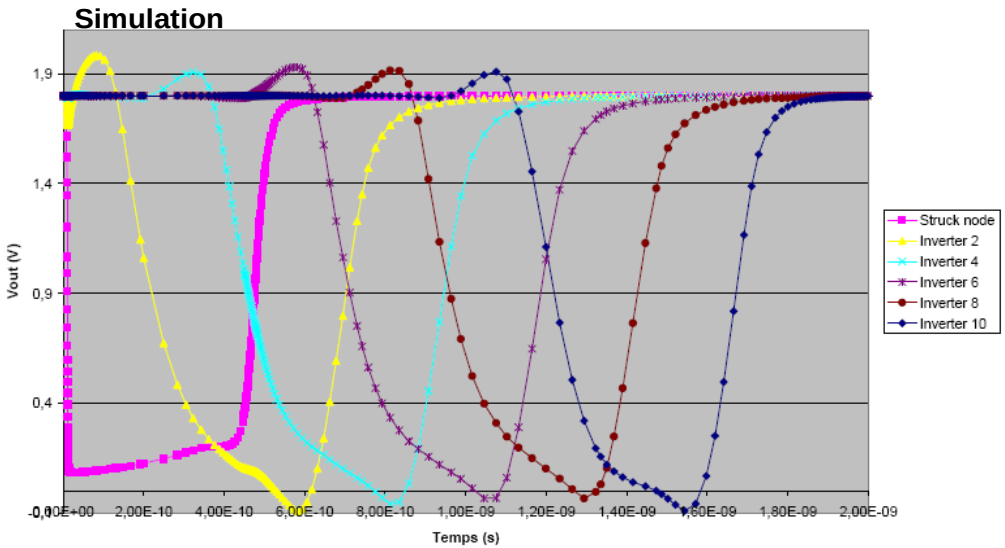
Investigations

- **Effect of the output capacitance : not a major effect**

INV0d1
SET Pulse width

LET(MeV.cm²/mg)	Duration without charge(ps)	Duration with load (C=8fF) (ps)	The increasing (%)
15	105	114	(+) 9%
35	270	280	(+) 4%

- **Mixed mode simulations**
  - **No broadening effect identified as of today**



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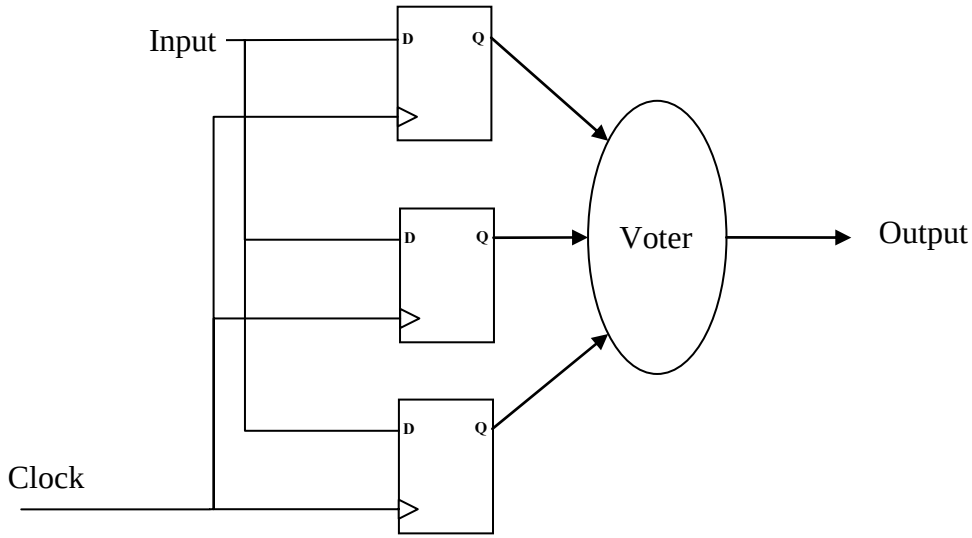
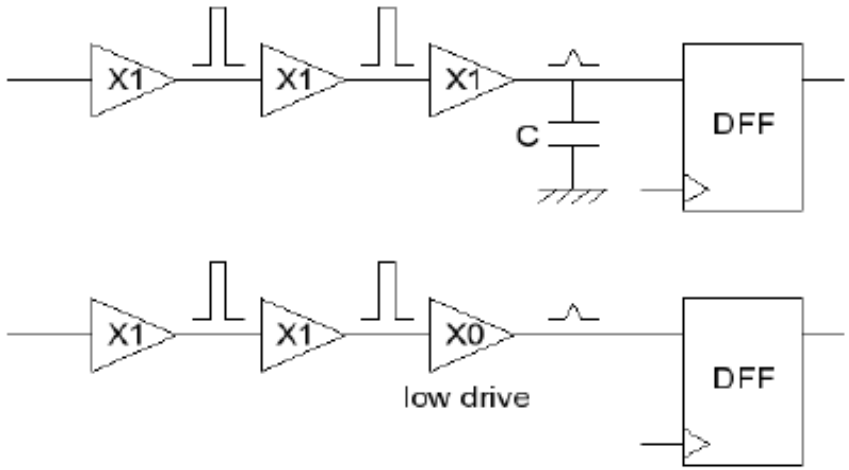
SEU mitigation

- **SEU-hardened flip-flops bring as well a kind of SET protection thanks to their minimum pulse width**
  - **For clock and data inputs only**
- **Triple Modular Redundancy**
  - **Bring a very good SEU protection**

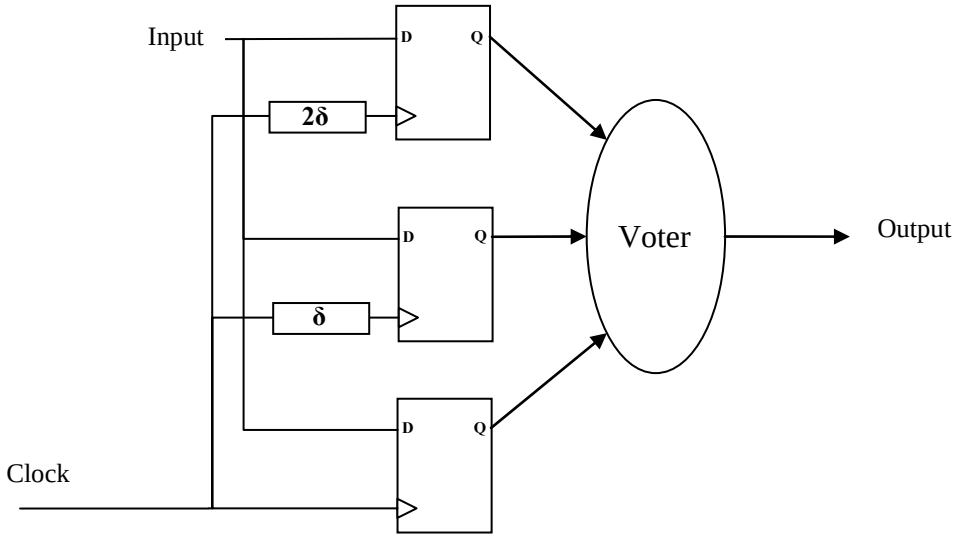


SET mitigation : delay filtering

- **Delay filtering**
  - **Increase the min time that a data has to be stable**
  - **Use of capa/resistance or low drive gate**



TMR with skewed clock

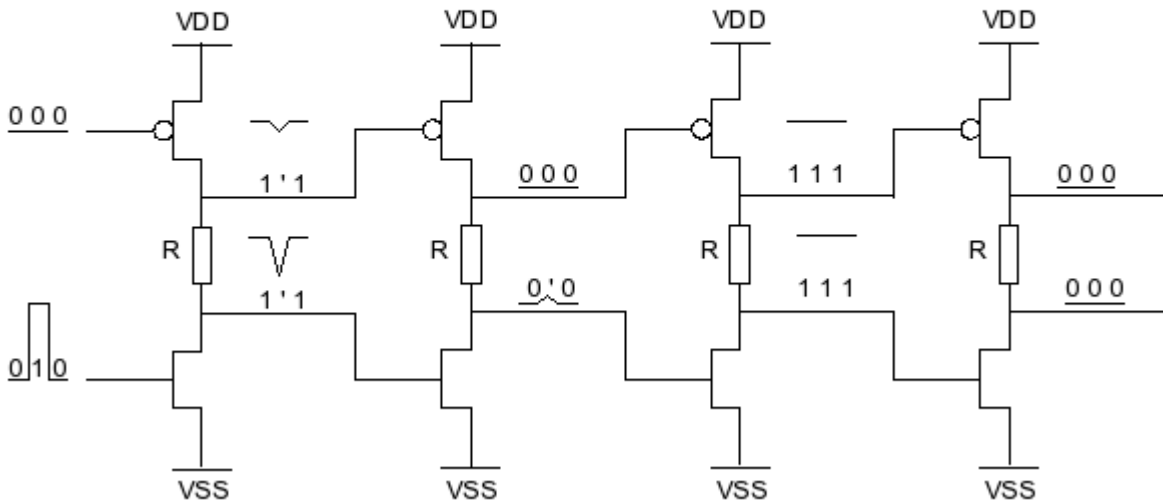


- **Some drawbacks**
  - **Speed**
  - **Area**
  - **Power**
  - **Set fix hold**

Dual stream cells

- **Separation of PMOS and NMOS block with resistance**
- **Duplication of inputs and outputs**

MOS split inverters in series

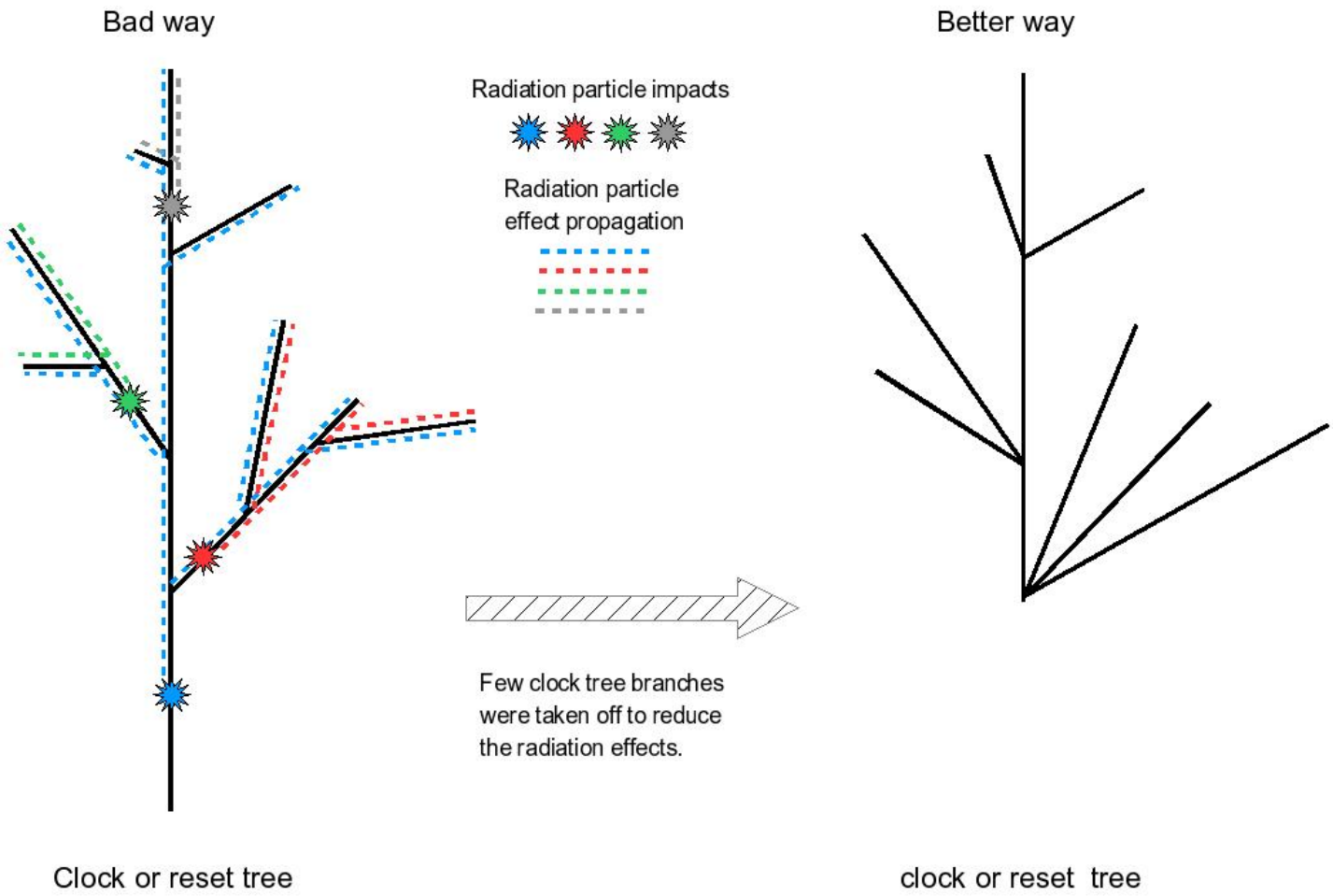


- **Not supported by P&R tools as of today**

Clock and reset trees - principles

- **Critical as a single event may impact a number of cells**
- **Recommended to use high drive cells**
- **When possible, for example on the reset tree, capacitance could be added to filter the SET pulse**
- **If a particular block of FF shall be protected, make sure to minimize the number of cells that can propagate to these FF.**

Clock and reset trees - example



Conclusion

- **This study has given an important quantity of information on SET on ATC18RHA**
- **3D simulations have given a good knowledge of the SET sensitivity of the ATC18RHA library**
- **The SET tests have allowed to derive for any ATC18RHA combinatorial cell an “SET event” rate in space**
- **This “SET event” rate is a worst case as the SET pulse is not propagated in a number of cases.**
- **The main SET concern relies in the clock and reset trees. If these trees are appropriately designed, it is considered that for ATC18RHA, the SET issue is not critical for any ASIC, for the usual requirements of space missions.**