SET study on Actel FPGAs

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Goal

- Analysis of the robustness of designs implemented on Flash-based FPGAs against Single Event Transients

Outline

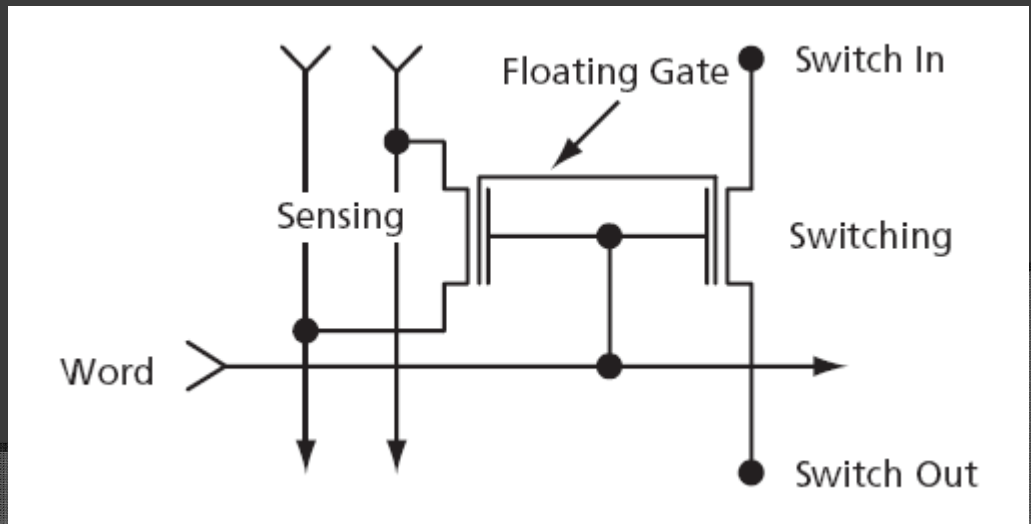
- Collaborations
- Flash-based FPGAs
- Radiation effects on Flash-based FPGAs
- The SET analysis flows
  - Measurement of the SET pulses
  - Analysis of the configuration memory
  - Modeling the Versatile logic
- Experimental results
- Status of the work

Collaborations

- Actel Corporation

Flash-based FPGAs

- Flash-based Field Programmable Gate Arrays (FPGAs) consist of:
  - Configuration memory of Flash-cells
  - Programmable logic blocks (VersaTiles)
  - Programmable interconnections



Radiation effects on Flash-based FPGAs

- Charge-leakage in the floating gate
  - Total Ionizing Dose (TID) lead degradation on switch threshold voltage (V_{TH})
- Single Event Transients (SETs)
  - High charged particles cross the logic and interconnections element

SETs effects on Flash-based FPGAs

- Effect on Sensitive node (i.e. logic gate)
- Effect in the logic configured as a latch
  - SET turns into a SEU (due to the feedback path)
- Effect in the floating gate switch
  - Effects may generate an SET into the logic / routing of the implemented circuit
  - Floating gate technology characteristics
  - Logic / Interconnection switch layout.

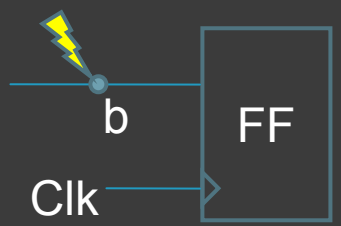
The SET analysis flows

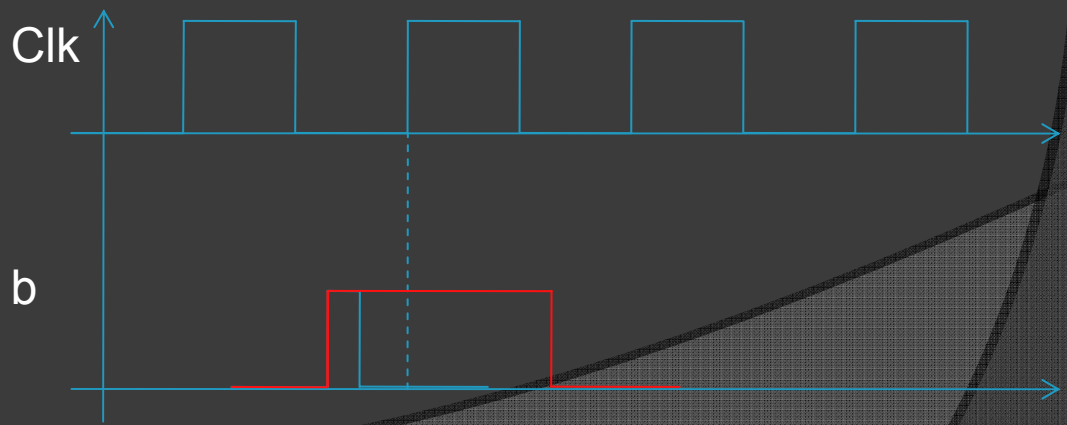
- Current development of analysis at multiple targets of the SET incidence on Actel Flash-based FPGAs
  - Measurement of SET pulses
  - Configuration memory
  - Logic / Interconnection model

Measurement of the SET pulses

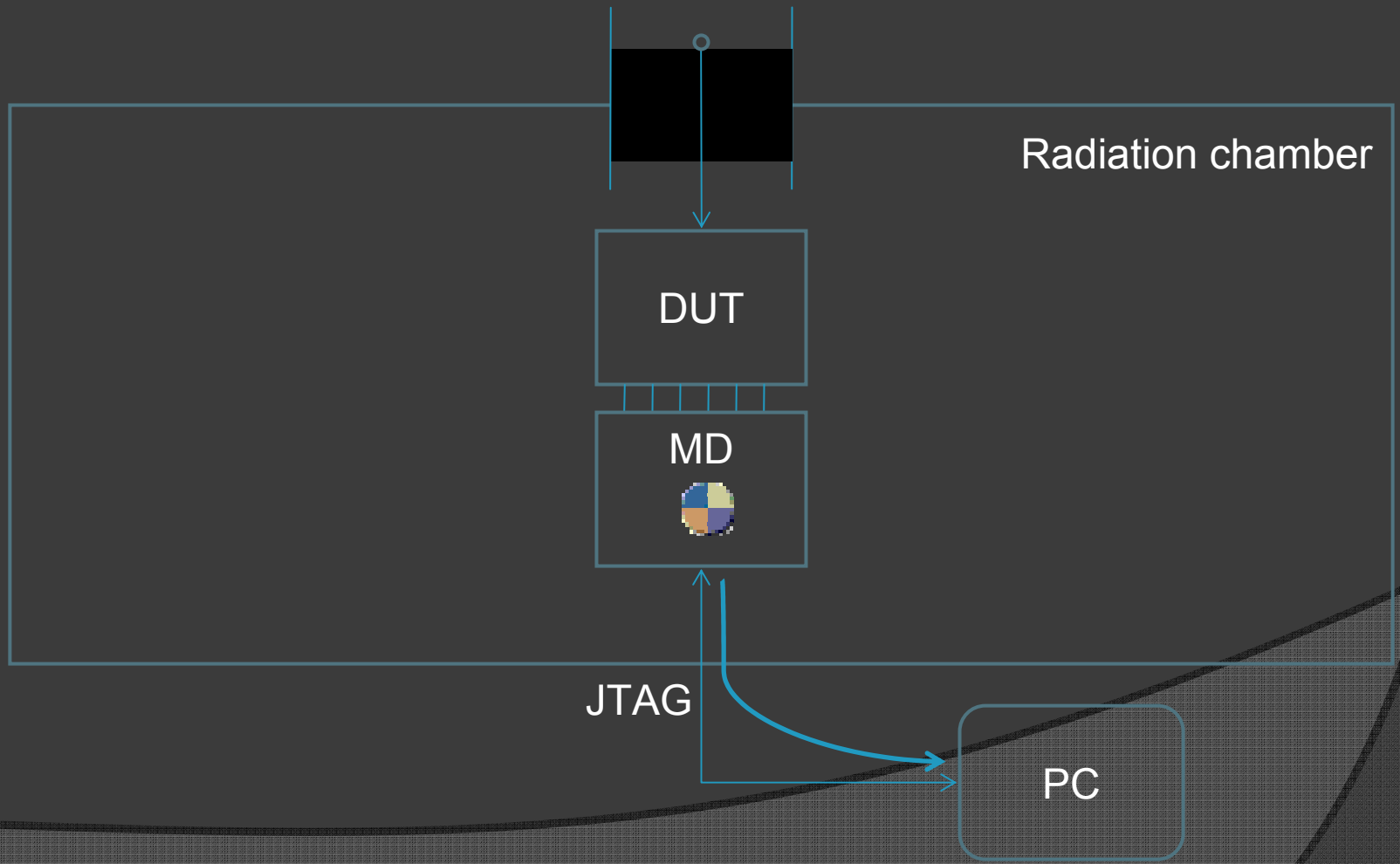
- The effect of an SET is mainly due to:
  - Location
  - Arrival time
  - Pulse's width.

Infinite number of combinations

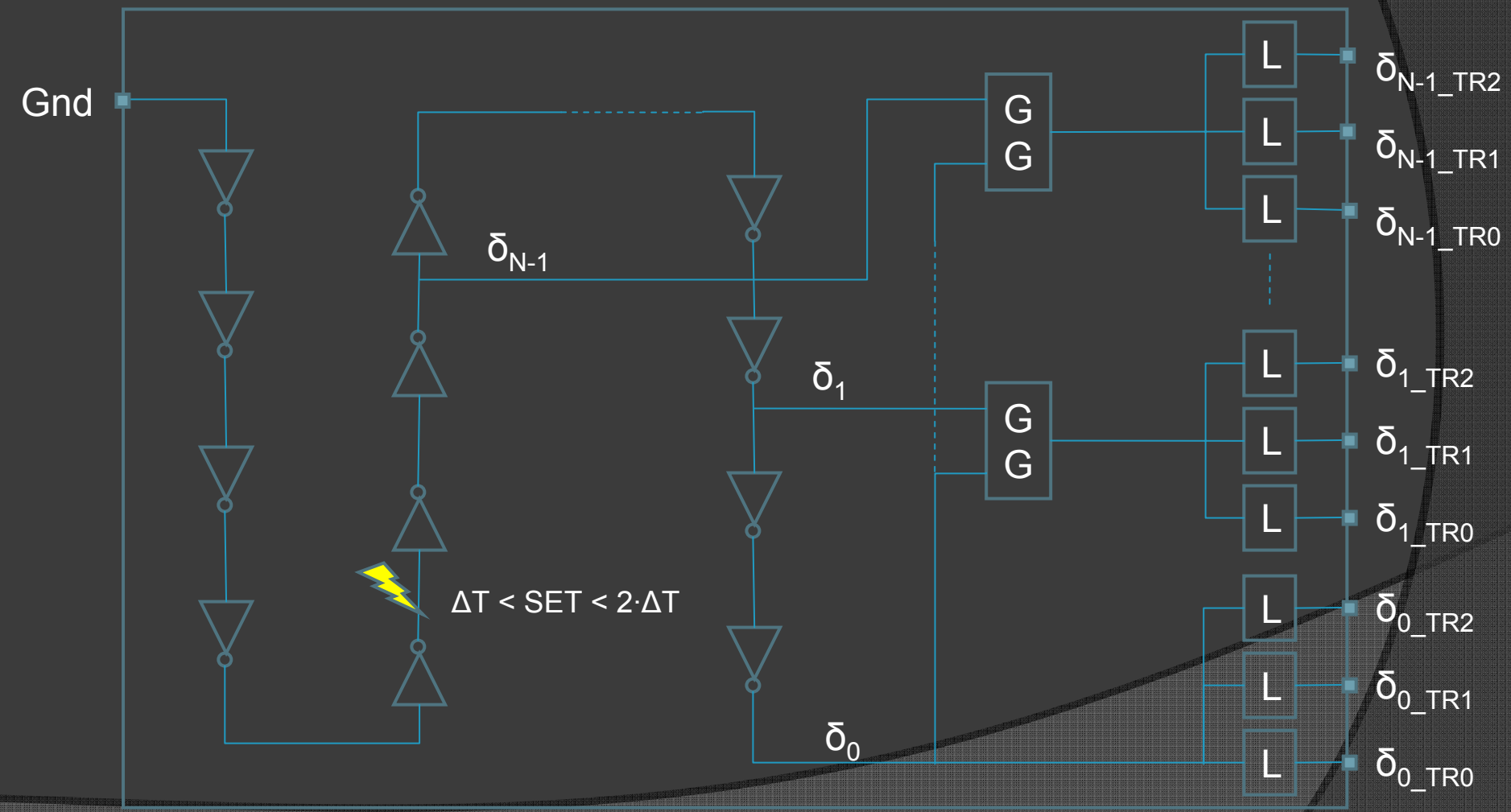




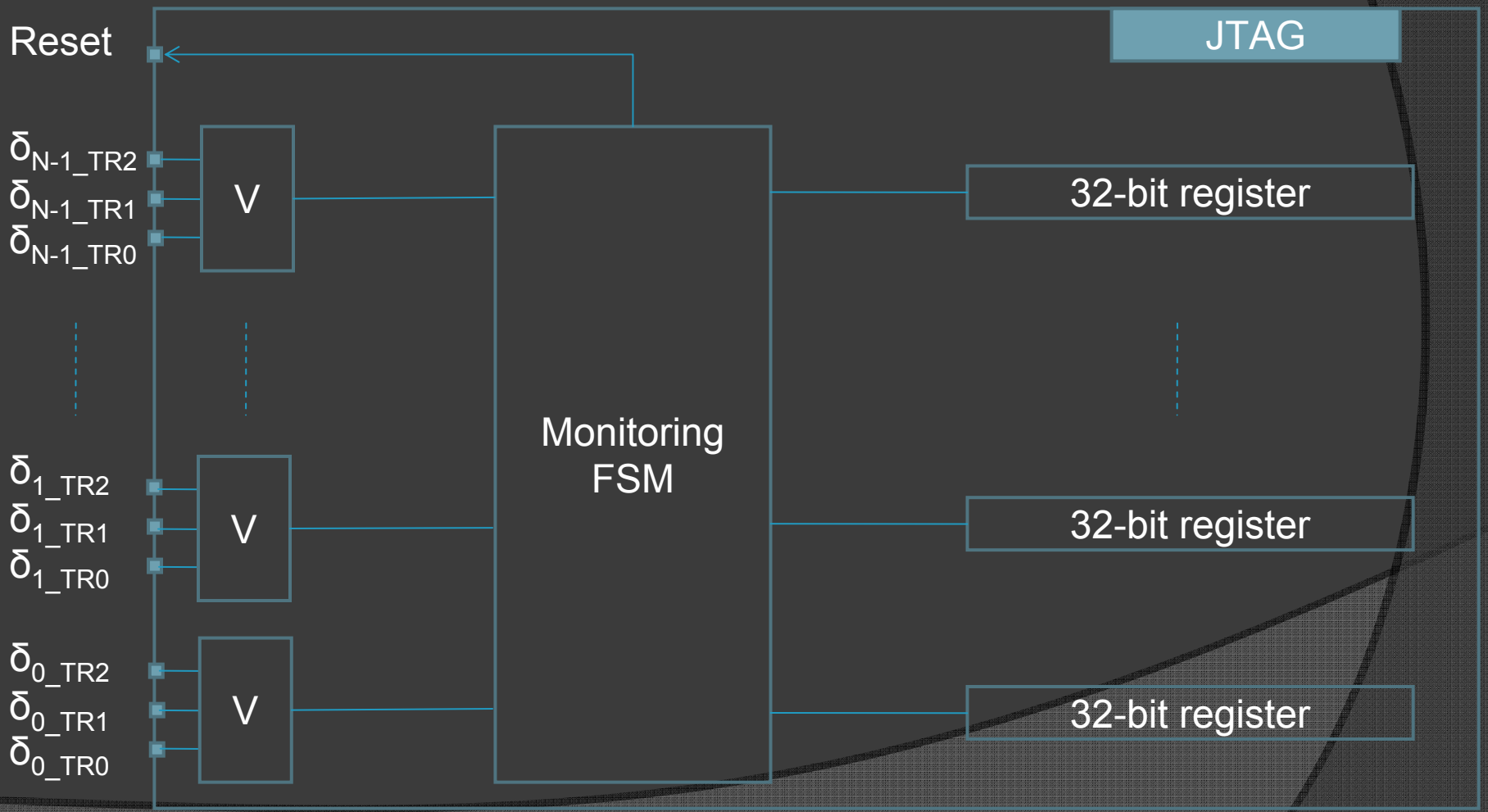
The proposed methodology



The DUT Design



The Monitoring Design

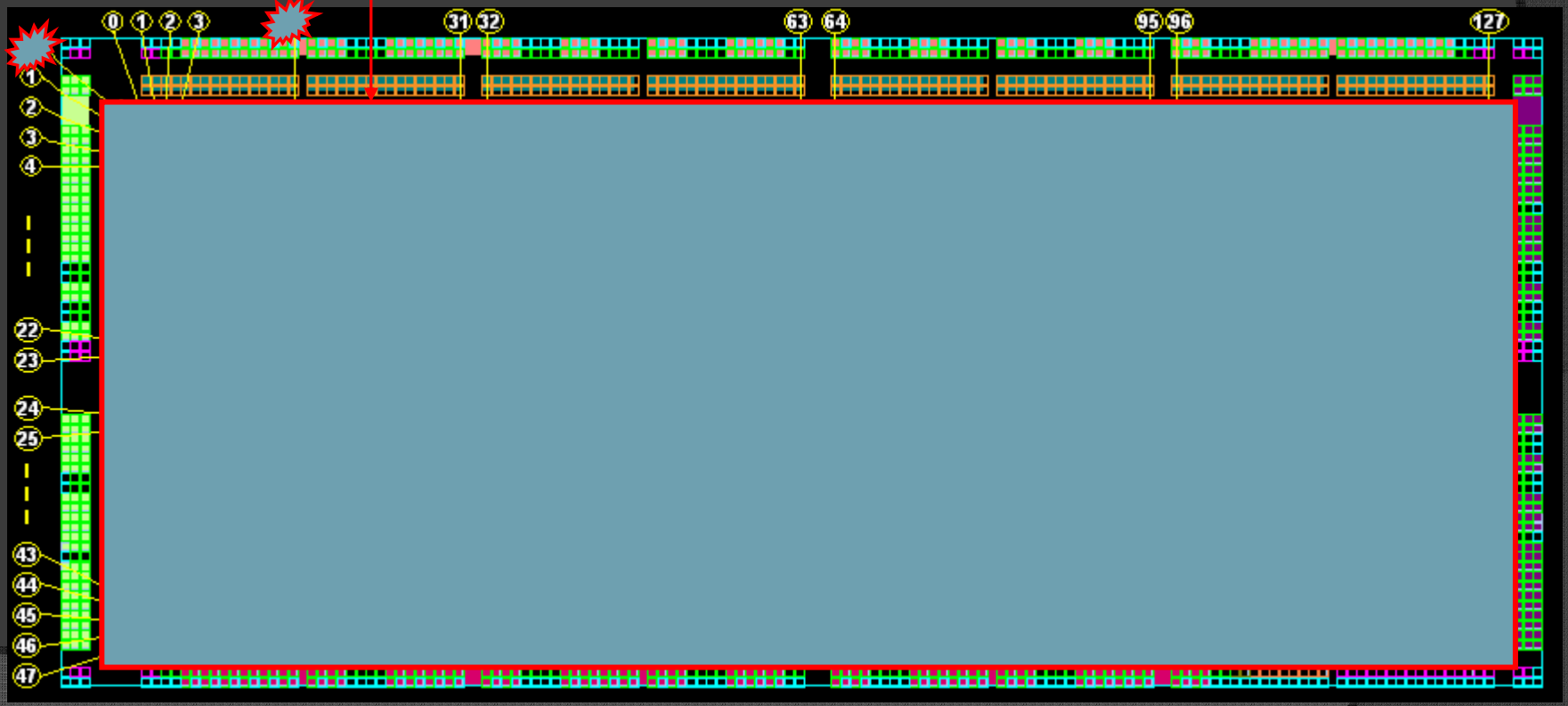


Analysis of the configuration memory

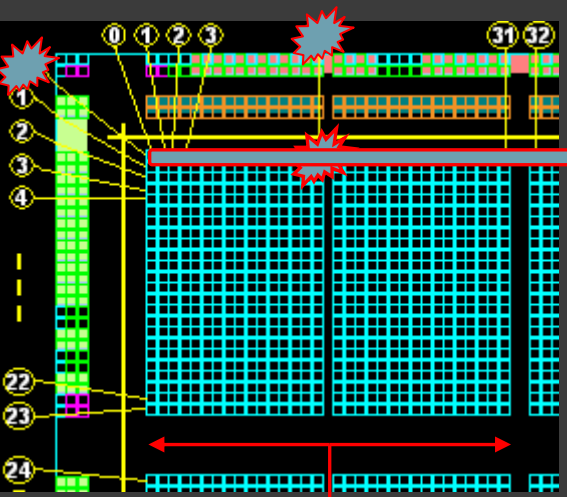
- Analysis of the original bitstream format
  - Finding the rows of tiles
  - Logical to physical mapping process
  - Logic resources allocation
- Analysis of the logic / interconnection topology
- Static Analyzer tool for the estimation of SET sensitiveness
  - First release validated on logic resources

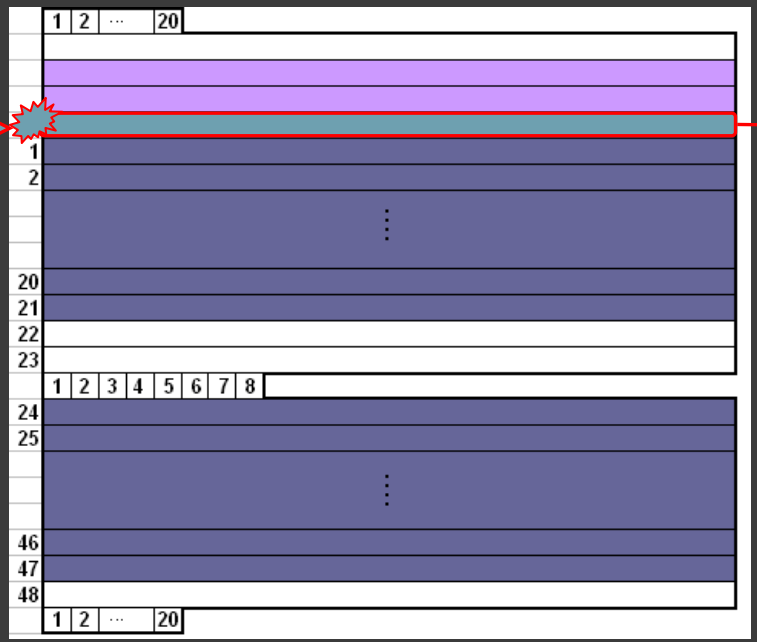
An example: tile [0,15]

- The [redacted] has got 47 rows and 127 columns. The coordinate [0,0] are in the corner in high on the right.



An example: tile [0,15]

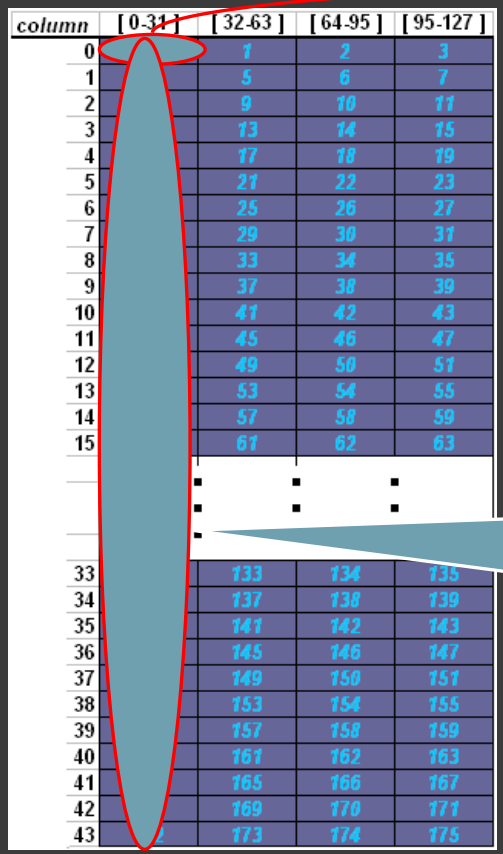




column	[0-31]	[32-63]	[64-95]	[95-127]
0		1	2	3
1		5	6	7
2		9	10	11
3		13	14	15
4		17	18	19
5		21	22	23
6		25	26	27
7		29	30	31
8		33	34	35
9		37	38	39
10		41	42	43
11		45	46	47
12		49	50	51
13		53	54	55
14		57	58	59
15		61	62	63
...		...	...	...
33		133	134	135
34		137	138	139
35		141	142	143
36		145	146	147
37		149	150	151
38		153	154	155
39		157	158	159
40		161	162	163
41		165	166	167
42		169	170	171
43		173	174	175

The column 15 locate the *block* in the frame:
15 mod 4=3
all the *blocks* that program the tile are in position:
(0+i*4) when i ϵ [0-43]

An example: tile [0,15] The Mapping



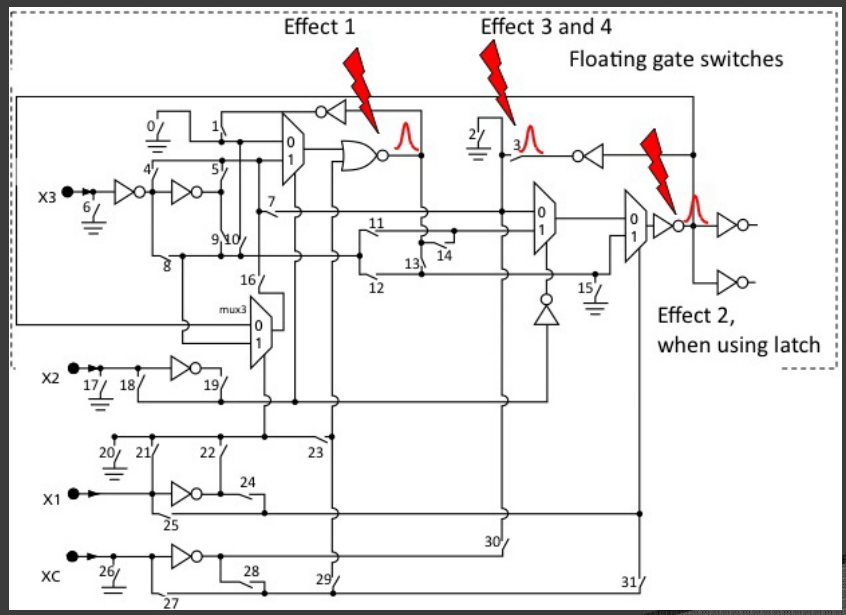
MAPPING

All the blocks that program the tile have got the same mapping.

Column of Tile # 15

Modeling the Versatile logic

- VHDL / Spice model of the Versatile cell
- Functional analysis
  - Fault injection of SET within the model



- Redundant configuration point

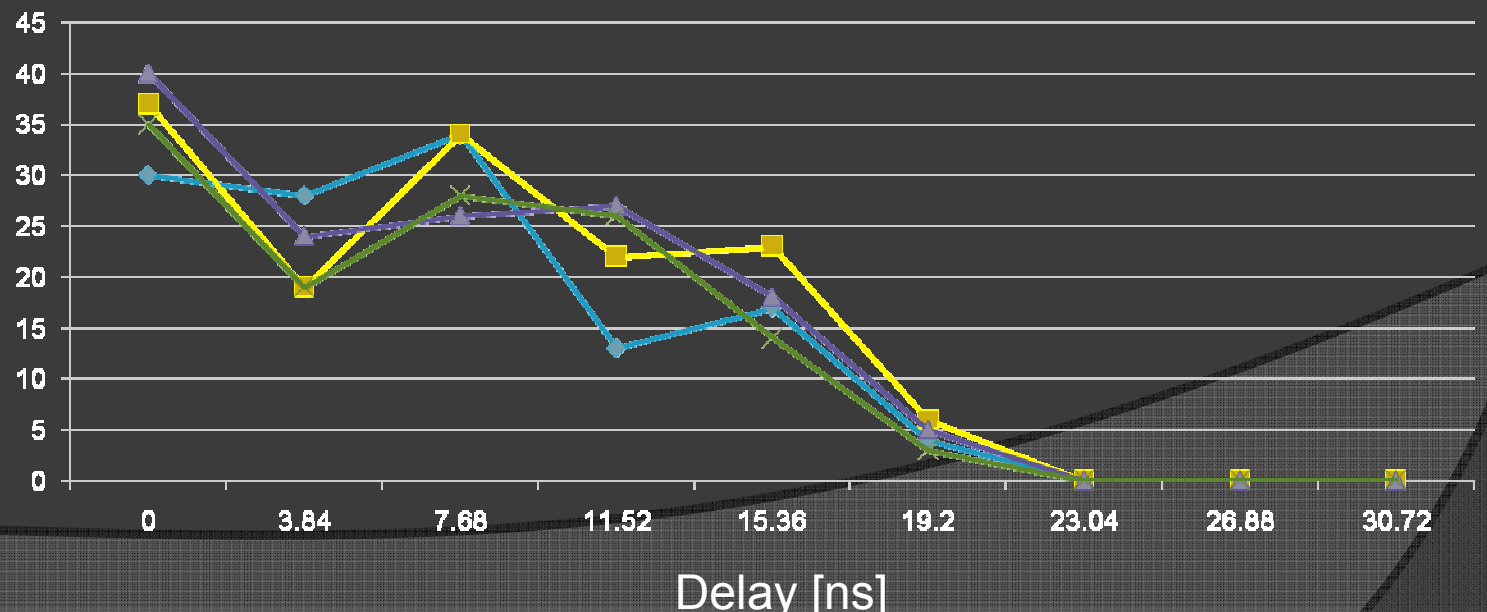
A case study

- DUT: Actel ProASIC3 250
  - 6,144 VersaTiles
  - A single chain composed of 5,652 inverters
  - 8 channels, ΔT = 3.84 ns
  - 8 channels, ΔT = 0.96 ns
- MD: Xilinx Virtex-II Pro 4
  - 100 MHz clock → blind time ≈ 20 ns
  - Partial readback capability
  - Full support for 11.49 IEEE standard (Boundary Scan)
- Ion beams: Cyclotron – Louvain-la-Neuve
  - Xe ions, LET = 5.59E+01 MeV·cm^2/mg, fluency = 1.00·10^6 particles/cm^2
  - Ar ions, LET = 1.41E+01 MeV·cm^2/mg, fluency = 3.00·10^6 particles/cm^2

Experimental results

- Measurement of SET pulses
  - Broadening effects among the DUT circuit
  - Widening effects dependent on the number of gates

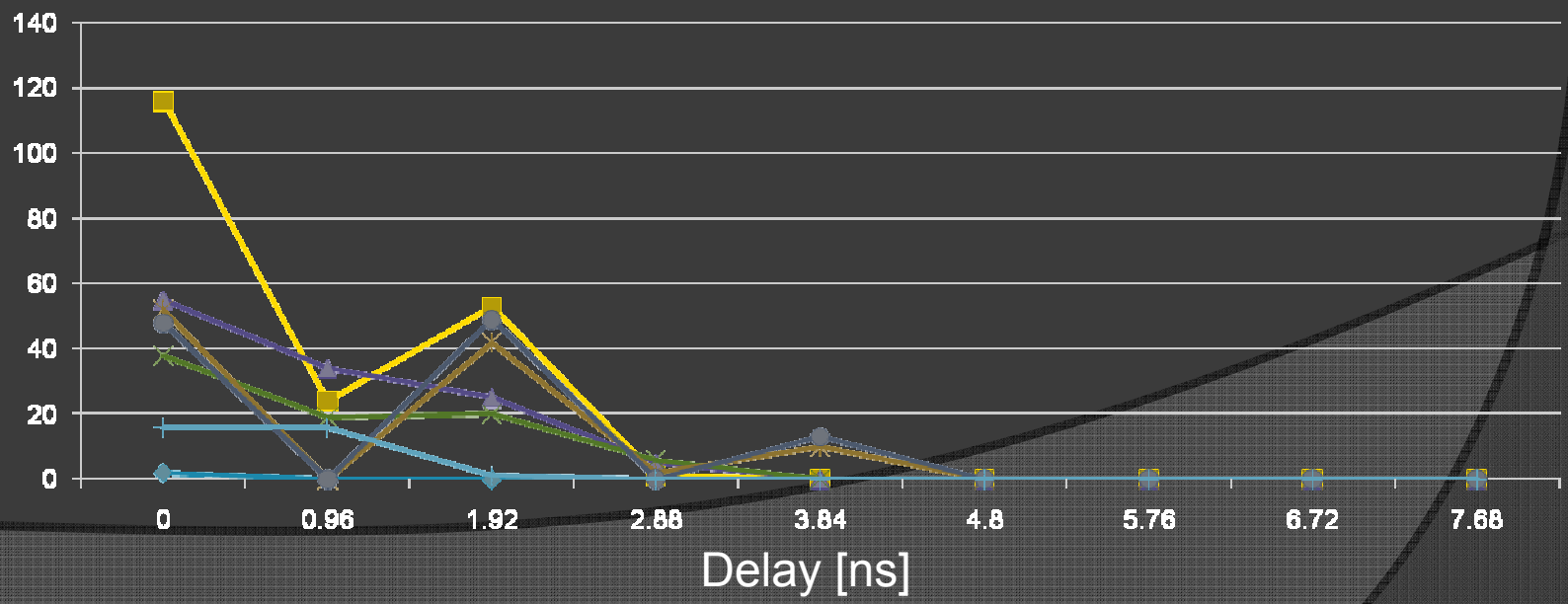
Event [#] – DUT with 4,500 inverters



Experimental results

- Measurement of SET pulses
  - Broadening effects among the DUT circuit
  - Widening effects dependent on the number of gates

Event [#] – DUT with 1,000 inverters



Experimental results

- Analysis of the configuration memory
  - Logic resources have been individuated
  - Interconnections rules are under development
- Logic sensitive locations computed and measured accordingly
  - LET [Xenon] of 5.59E+01 MeV·cm²/mg
  - LET [Argon] of 1.41E+01 MeV·cm²/mg

Experimental results

Circuit	Ion	Sensitive location [#]	Used Tiles [#]	Measured SET [#]
450	Xe	6,664	903	20
1000	Xe	12,538	1,632	42

The proportional coefficient between sensitive locations and the measured SET is approximately 333 for Xe ion and about 1,332 in the case of the Ar ion.

The ratio between the two proportional coefficients (1,332 / 333 = 4) is almost equivalent to the ratio between the energy transferred to the device (LET[Xe] / LET[Ar]) = 3.96.

Experimental results

- Dynamic test
  - Pipelined multiplier 16-bits and 35-stages
  - Running frequency: 40 MHz
  - 20 runs

- Two mapping with different routing
  - 136,555 configured bits: 105 average observed SET/SEU
  - 228,263 configured bits: 114 average observed SET/SEU

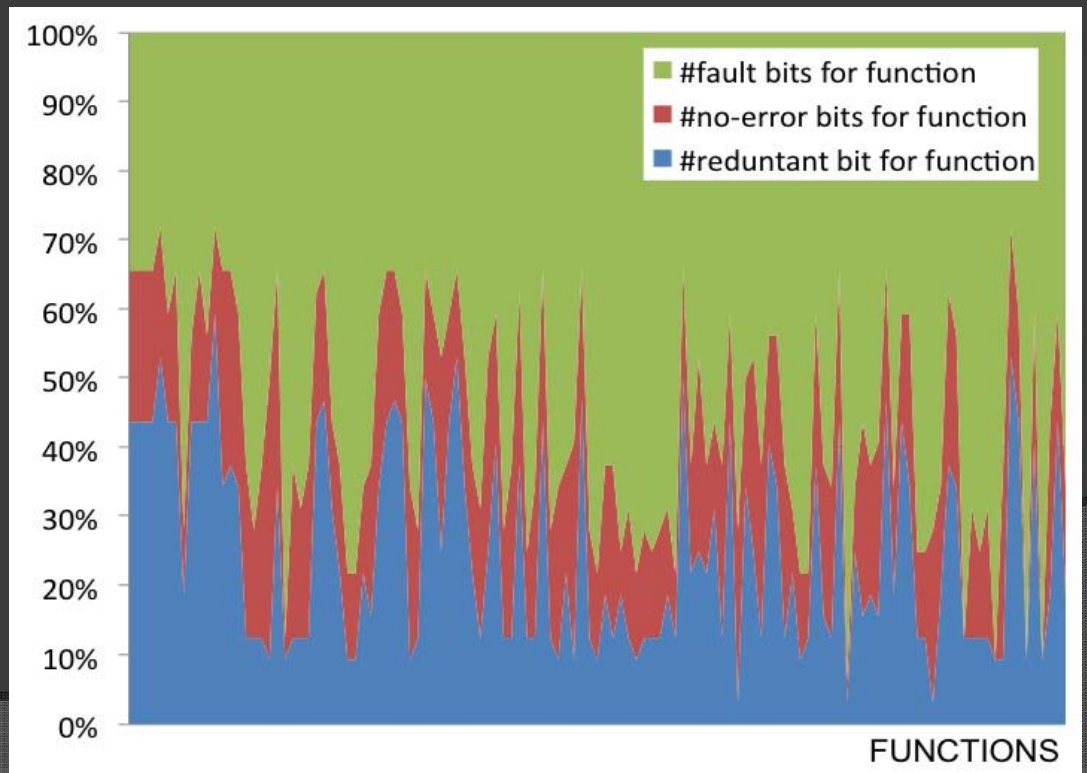
Experimental results

- Static test
  - Shift registers16-bits and 35-stages
  - 14 runs for each circuit

- Two circuits with different initial condition
  - 1 -> 0 - 36 observed SEU
  - 0 -> 1 - 52 observed SEU

Experimental results

- Modeling the VersaTile
- Different mapping lead to a decrease of about 56% of fault bits on the average



Status of the work

- SET measurement
  - Static and Dynamic test with different running frequency
  - Different gates sensitivity
- Configuration memory
  - Logic elements : stable
  - Interconnections hierarchy : on going
- VersaTile model
  - Integrating redundant function into an automatic mapper tool : on going

Thank you...

For questions and comments,

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