SET Generation & Definition - Overview

Andrew Chugg

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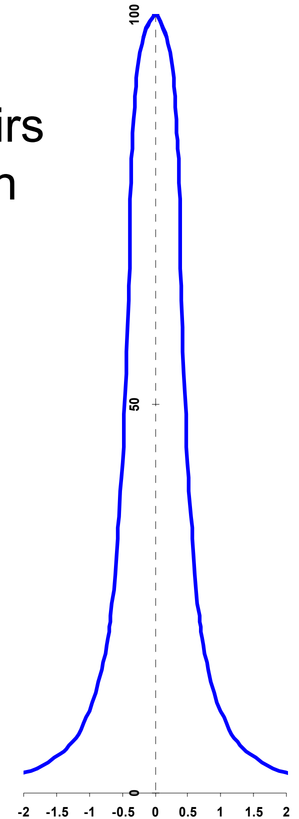
Single Event Interaction

- Single event phenomena occur as the result of a single particle interacting with a target material.
- The transit interaction of energetic single event particles are dependent on the particle and its energy as well as the material properties and dimensions through which it is travelling.
  - Transits generally occur in: ~ 1E-12 seconds [~1ps]
- The transit interaction results in the generation of electron-hole pairs [i.e. ions] along the track of the transiting particle through ionisation processes {~1ps}.
- The resultant 'instantaneous' plasma cylinder or charge column has an instantaneous nominal diameter of less than 1µm within which the ion (i.e. charge) density reduces from the centre as a function of r^{-2}.
- Any movement of the created charges equate to a current.
- In the presence of an electric field the charges will move in proportion to the strength of the electric field.



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Terminology: Single Event Transient (SET)

- In integrated circuits (IC's) reverse biased junctions collect charge due to the influence of the electric potential gradient.
- The movement of charge (current) causes changes to the device voltage potentials in the circuit and a voltage transient results.
- The movements of the charges with respect to the various circuit elements in which the charges are generated define the types of phenomena that will be created.
- Where the movement of charges cause a short term transient (glitch) which recovers in time without other actions to clear error condition it is termed a Single Event Transient (SET).
- SET's in analogue IC's (ASET's) commence from very low threshold levels because the operation of the circuit elements are working in their linear region (non-saturated conditions) and therefore any additional currents in the circuit will disturb the 'normal condition'.
- SET's in digital IC's generally require a specific minimum quantity of charge to be injected at a sensitive node before a transient will be observed because the parts are working in their saturated condition.
  - SEU's occur at the site where an error is latched in
  - SET's propagate to sites where they cause errors to be latched in

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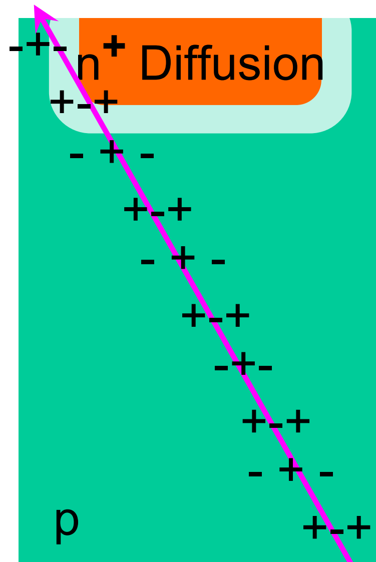
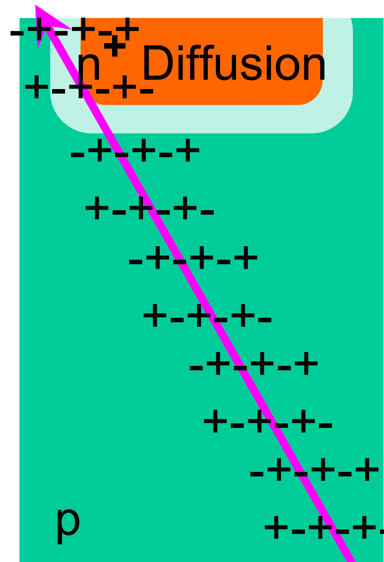
Terminology: Linear Energy Transfer - LET

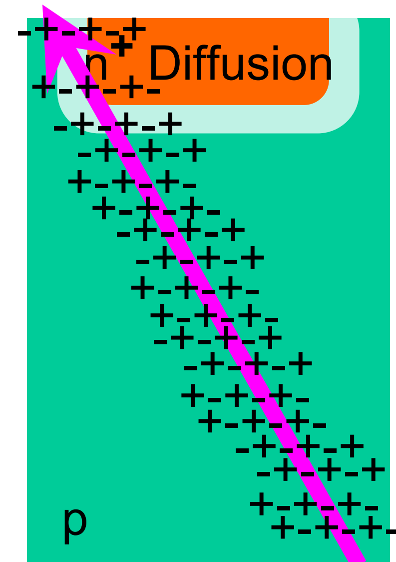
- Defines the quantity of energy that a particle will deposit per unit mass thickness by the ionisation process as the result of the interaction in the material. [i.e. The generation rate of electron-hole pairs along a track or column in a material.]
  - LET is a function of the particle's energy, type, mass, and electrostatic charge
    - AND of the material type, but we are usually concerned with LET in Si
  - LET is defined: Energy deposition per mass thickness, units: MeV.cm^2.mg^{-1}.



Low LET Ionisation Track



Moderate LET Ionisation Track



High LET Ionisation Track

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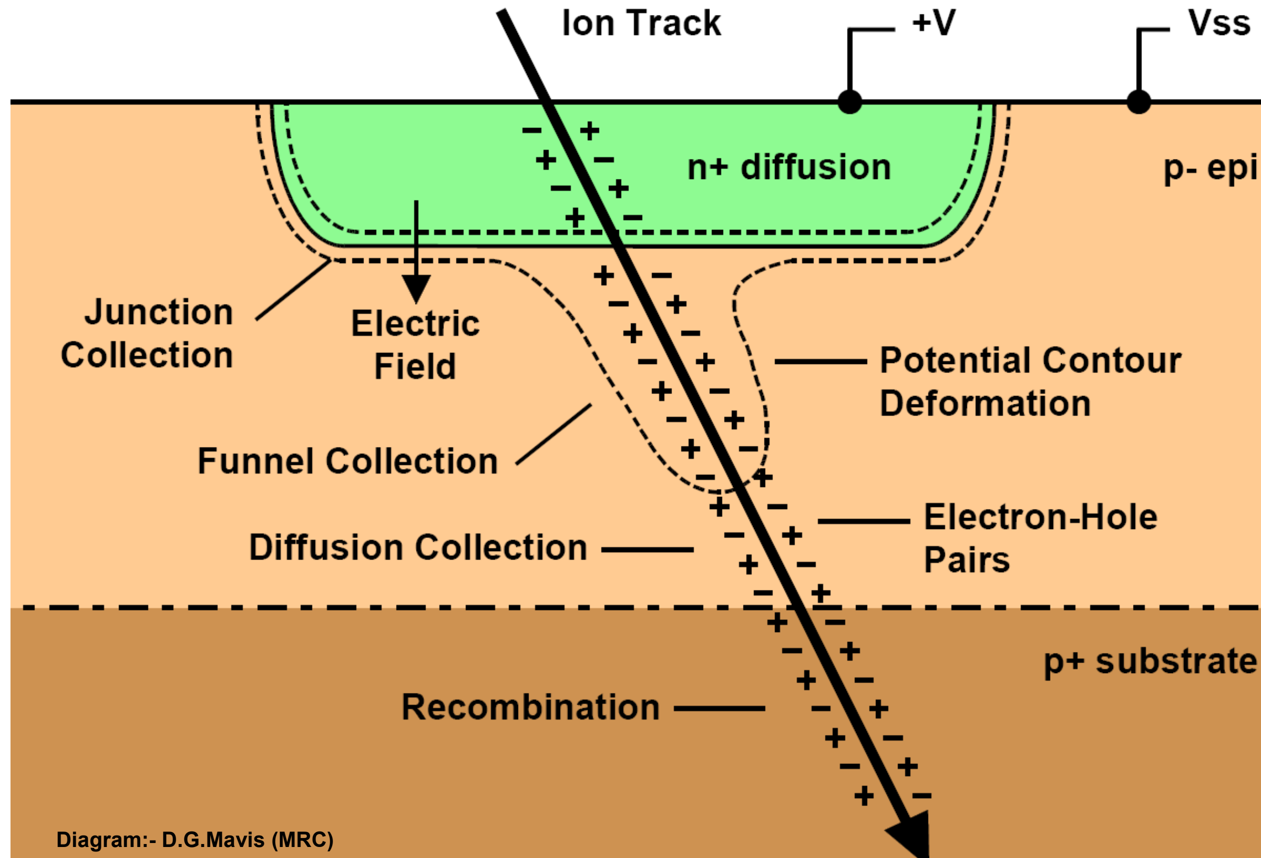
Charge Collection in a Device



- Junction collection potential well is distorted as the result of the ion strike in the semiconductor.
- Charges move in the semiconductor under the influence of the electric field through the semiconductor drift and diffusion processes.

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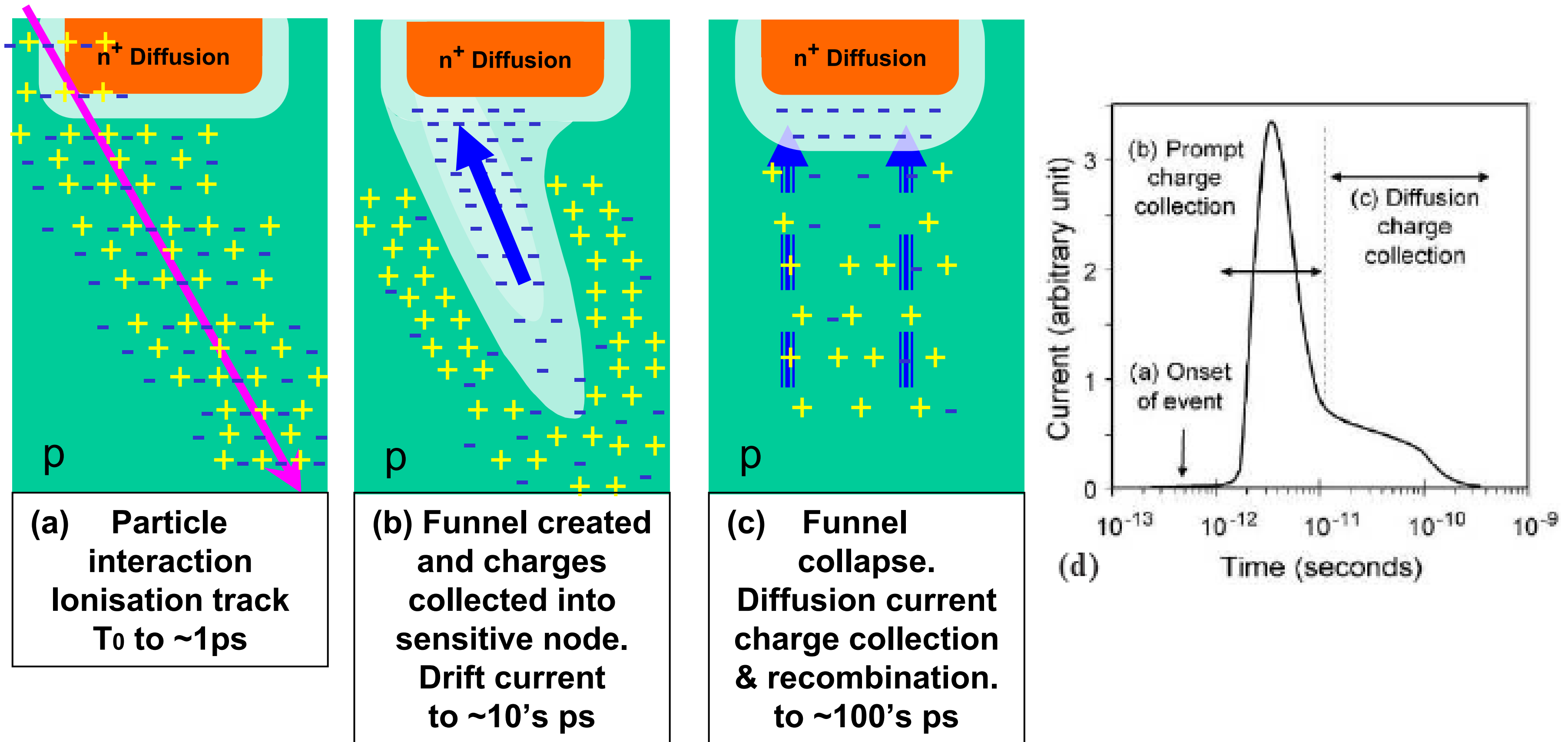
Charge Collection in a Device



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Terminology: Cross-Section (σ)

- Effective target area of a device that is susceptible to the generation of a single event phenomenon
  - Not all areas of the device when hit will result in a single event phenomenon or behaviour.
- The #-section is defined in units of area per device, [or per memory cell or per driver or per amplifier in multi function devices] e.g. in cm^2/device (or mm^2/device).
- Any #-section will need to be defined for a specific SET characteristic behaviour for a given LET value and possibly for the temperature and frequency or other conditions. e.g. LM137 - Negative Voltage Regulator
  - σ(SET(ΔV_{OUT} : -0.2V, I_{Load} : 300mA @ 20°C)) = 3.5E-3 cm^2 @ 10MeV.cm^2.mg^{-1}
  - σ(SET(ΔV_{OUT} : -0.2V, I_{Load} : 300mA @ 20°C)) = 5.0E-3 cm^2 @ 20MeV.cm^2.mg^{-1}
  - σ(SET(ΔV_{OUT} : -0.5V, I_{Load} : 300mA @ 20°C)) = 7E-4 cm^2 @ 10MeV.cm^2.mg^{-1}
  - σ(SET(ΔV_{OUT} : -0.5V, I_{Load} : 300mA @ 85°C)) = 2E-3 cm^2 @ 10MeV.cm^2.mg^{-1}

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Terminology: Analogue device Single Event Transient (ASET)

- ASET's vary widely in their characteristics
  - depending on the exact location in the circuit
  - the additional charges created by the ionisation may add to or detract from
    - the intended signal currents
    - or the relative charge levels [Q]
  - differences in
    - waveform shape
    - amplitudes
    - durations.
- As the quantity of charge captured [Q_c = (charge injected [Q_I] x capture efficiency)] at a specific node increases the severity of the upset behaviour increases with respect to the voltage transient and its duration. i.e.:
  - An incident particle generates a charge density Φ in the volume of a sensitive node [80% capture efficiency] and causes a specific behaviour then, all other things being equivalent another particle that strikes a volume very close to the sensitive volume but has a capture efficiency of only 20% for the node will require to generate a charge density of 4Φ to achieve the same response.

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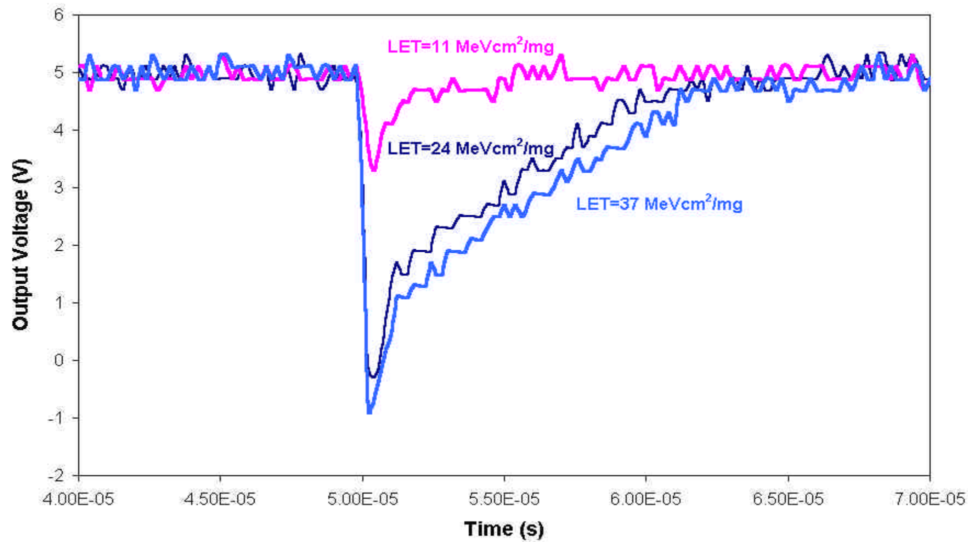
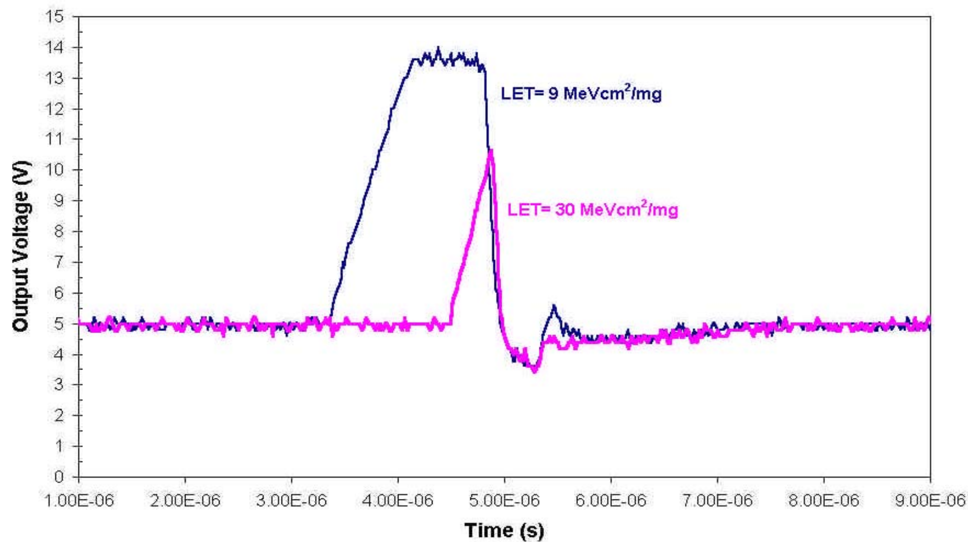
Terminology: Analogue device Single Event Transient (ASET)





- LM124 OpAmp - Voltage Follower Output responses due to interaction of different ion types.

  [Vcc = ±15V, Δ+V$_{IN}$ = 5.0 V]

At node A

At node B

Source NASA Test Guidelines

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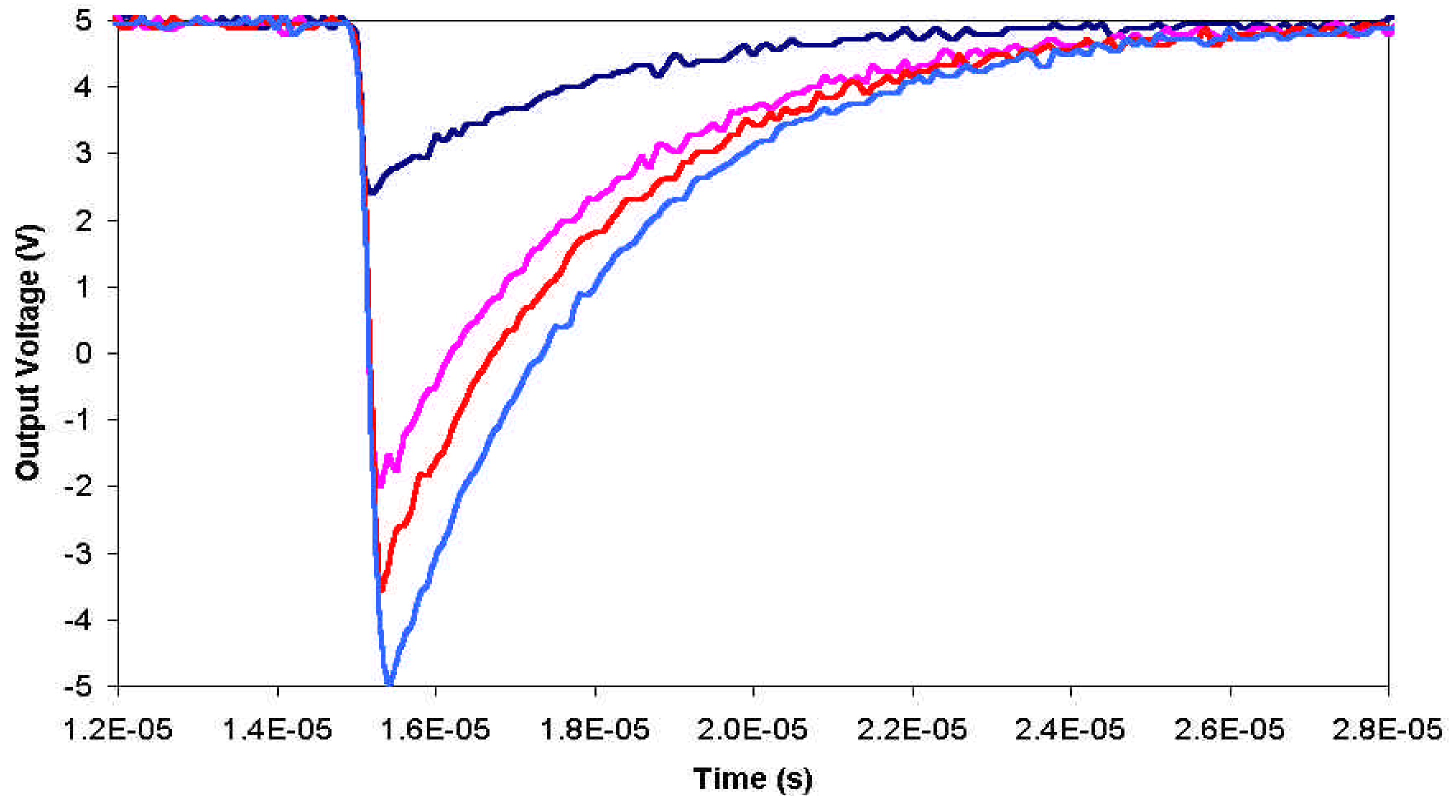
Terminology: Analogue device Single Event Transient (ASET)



- LM139 Voltage Comparator Output responses due to interaction of a single ion type [18.7 MeV.cm^2.mg^{-1} ions] in and adjacent to a specific sensitive node. [Vcc = ±5V, ΔV_{IN} = 800 mV]

Source NASA Test Guidelines

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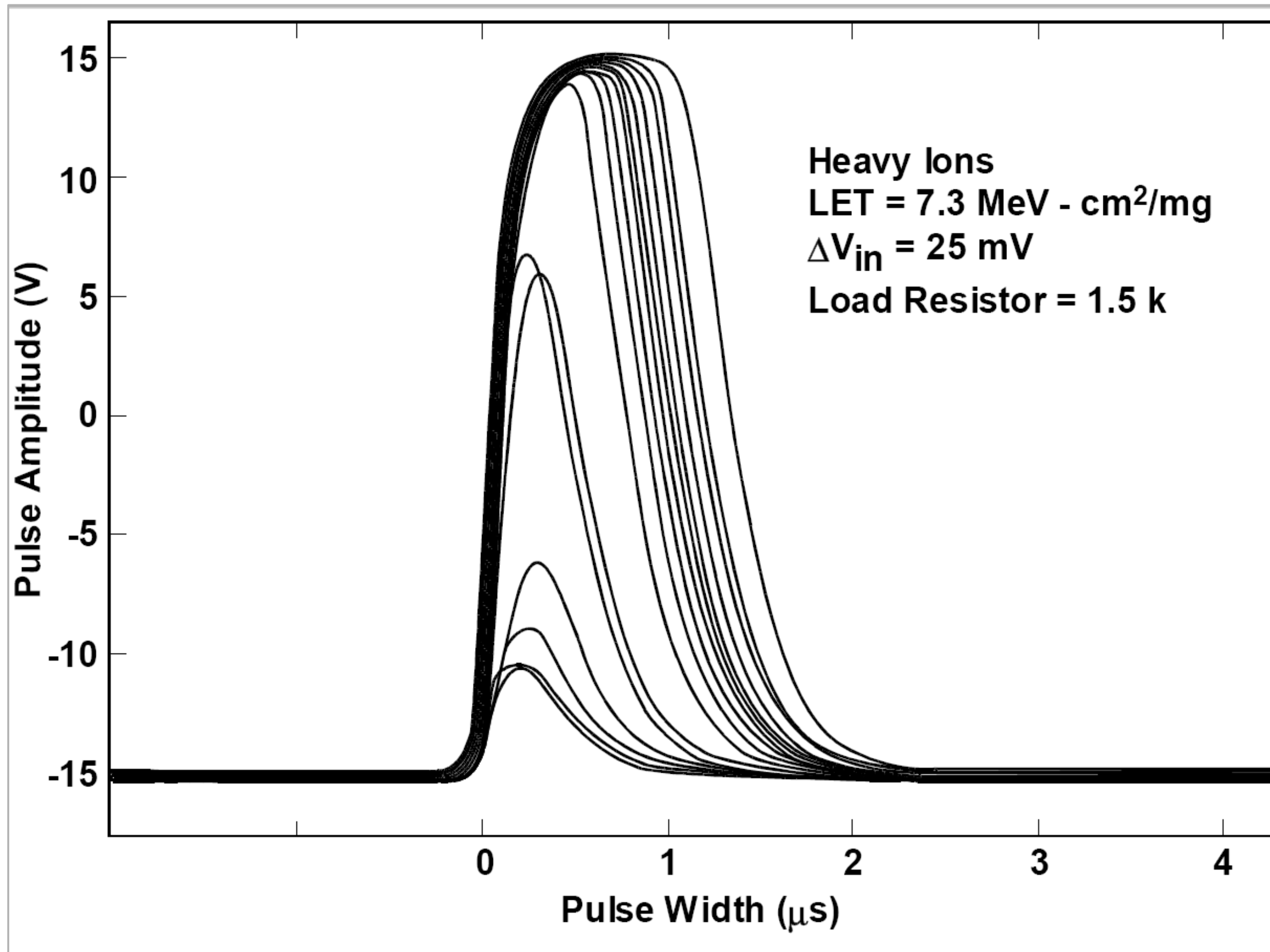
Terminology: Analogue device Single Event Transient (ASET)



- LM139 Voltage Comparator Output responses due to interaction of a single ion type [7.3 MeV.cm^2.mg^{-1} ions]. [Vcc = ±5V, ΔV_{IN} = 25 mV]

Source A. H. Johnson JPL

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Terminology: Analogue device Single Event Transient (ASET)

- ASET’s observed in analogue devices additionally have different characteristics as the result of different input conditioning:
  - Supply voltages.
  - Supply current drive - impedances & capacitance.
  - Input current drive - impedances & capacitance.
  - Input voltages - absolute & differential.
  - Signal frequency - first & second order.
  - Temperature
- ASET’s observed in analogue devices also have different characteristics as the result of different output conditioning:
  - Output load - impedance & capacitance.
  - Feedback characteristics - gain & time domain.

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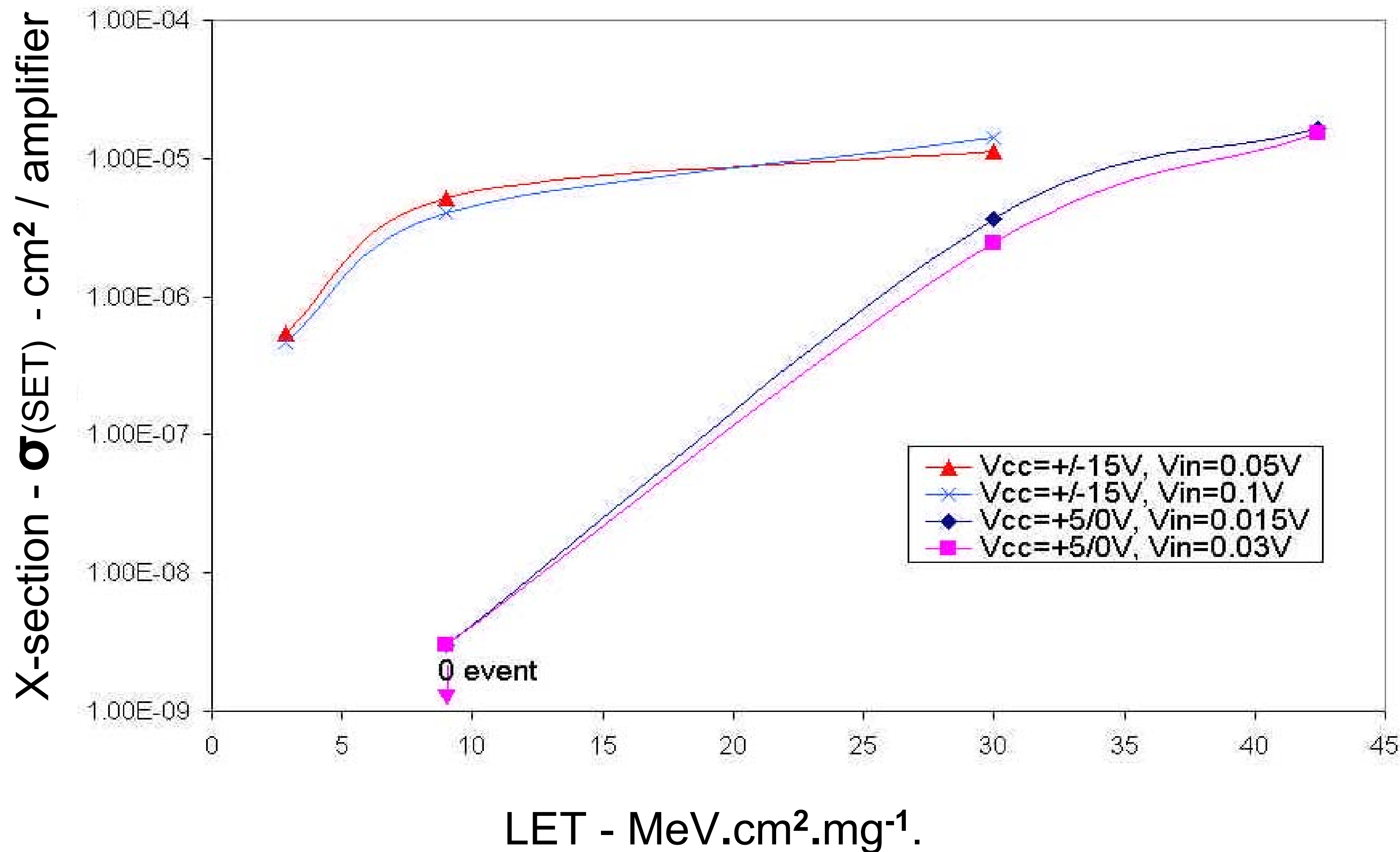
Inputs: Supply Voltage Effect on a LM124 Amplifier SET



Source NASA Test Guidelines

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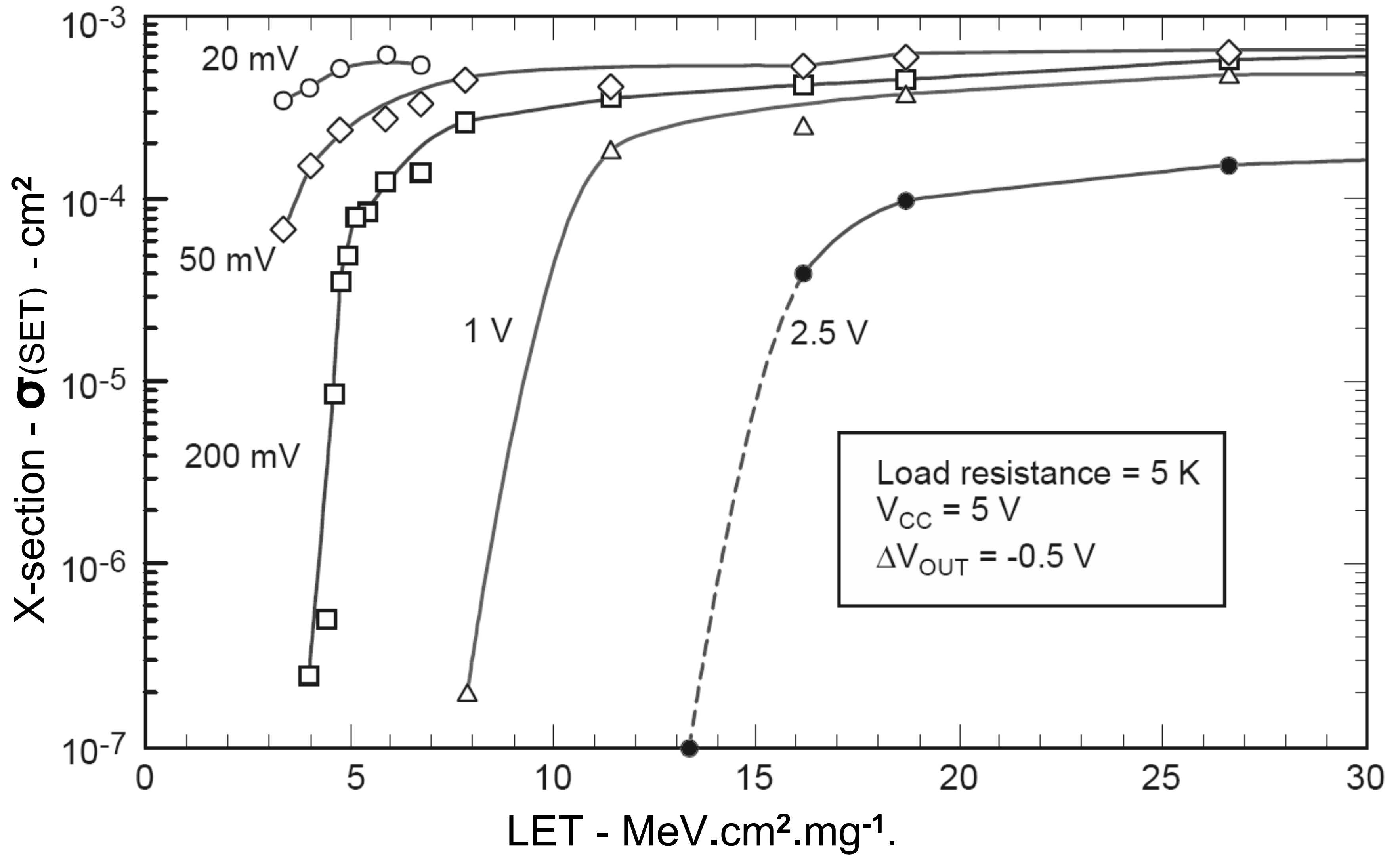
Inputs: Differential Input Voltage Effect on a LM139 Comparator SET



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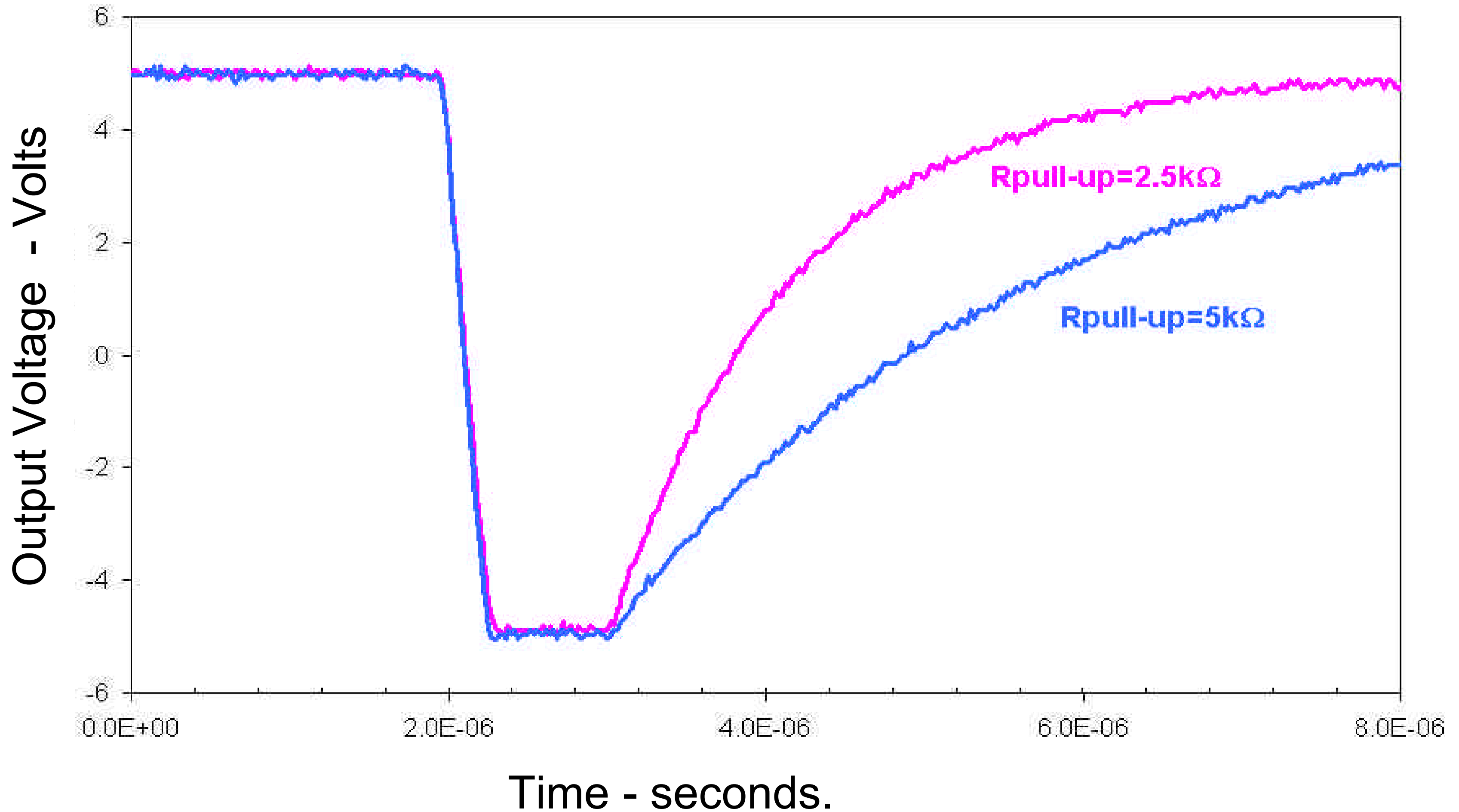
Outputs: Output Pull-up Effect on a LM139 Comparator SET Characteristic



Vcc = ±5V; Input V+ = 3 V; Input V- = 2.9V

LET = 11.4 MeV.cm^2.mg^{-1}.

Source NASA Test Guidelines

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Terminology: Digital device Single Event Transient (DSET)

- DSET's occur as the result of the same drivers as those of the ASET.
- The difference for digital devices is that the input and output conditioning is relatively well fixed and the elements within the device are operating in their saturated current condition:
  - Elements in the ON condition - SET charges added to an already saturated condition has negligible effect.
  - Elements in the OFF condition - SET charges created in elements passing only their leakage currents inject a primary level of current into the circuit. When the transient current is of sufficient magnitude to temporarily upset the stable condition a transient will occur; i.e. the charge collected at the OFF node must be greater than a value $Q_{CRITICAL}$.

- In CMOS devices the sensitive volumes are:
  - The channel region for the OFF NMOS FET.
  - The drain region for the OFF PMOS FET.

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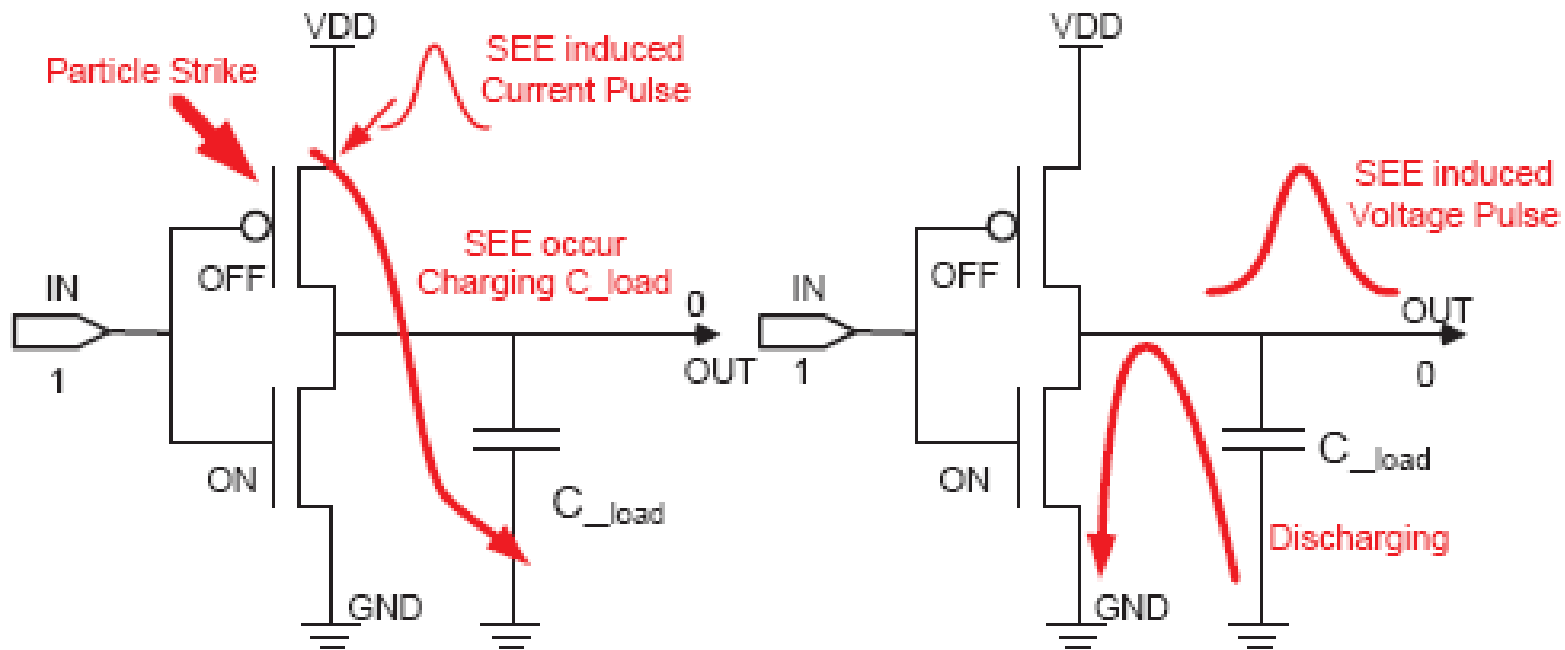
SET generation in a CMOS Inverter Element

- The voltage transient requires a quick injection of charge into the load capacitance in order to create a voltage transient at the output.
  - The voltage transient is a function of the value of the circuit capacitance (C) and the rate of charge injection into the capacitance (dQ/dt). Defined by the Drift and Diffusion currents set up in the struck node.
  - If the current injected into the capacitor is to slow then the discharge rate causes the maximum voltage transient to be small.



Ref.. . . . . . Diagram Source: Wang & Agrawal (Auburn University)

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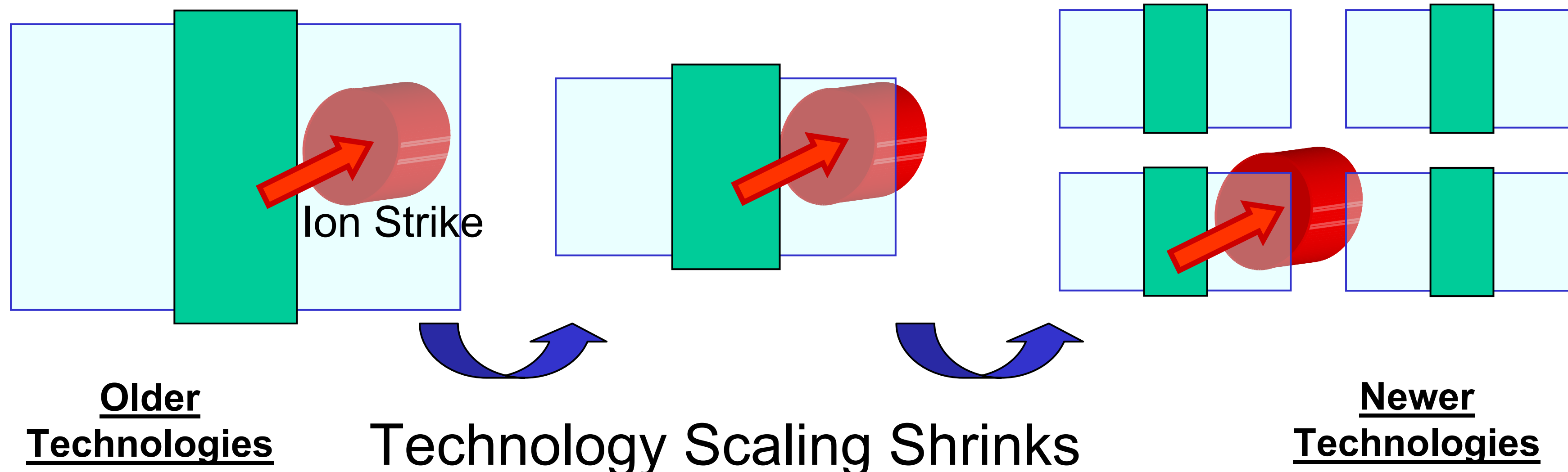

- In older technologies the ion track charge column was smaller than the transistor volume and the device critical charges larger.
- In new technology devices the ion track charge column can be larger than the transistor volume and may influence multiple transistors and the device critical charge is smaller.
  - The resultant effects are dependent on the spacing and interconnections.

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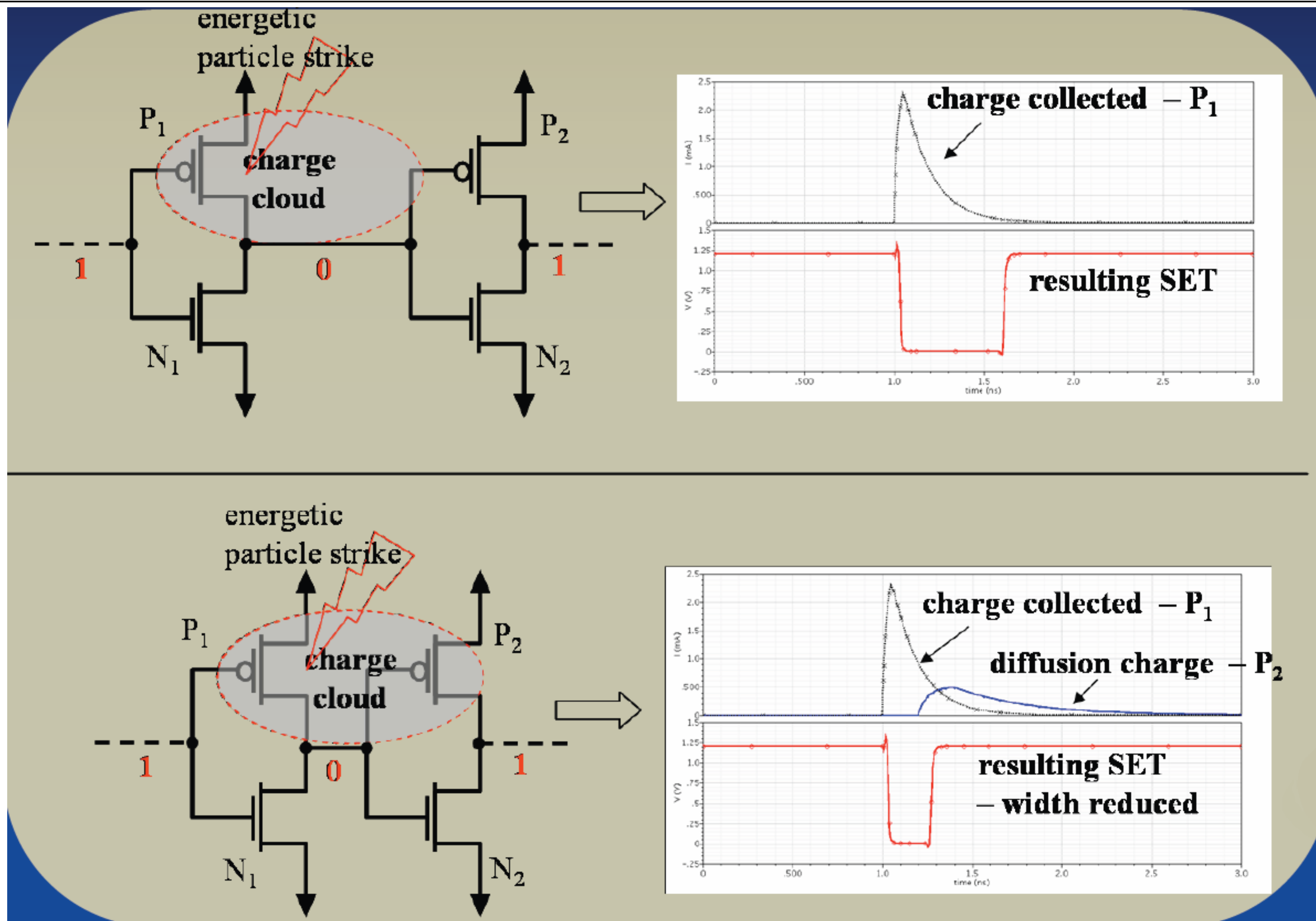
Results of Charge Collection at Adjacent Nodes



Source: B. Narasimham (Vanderbilt University) May 2008

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DSET Propagation & Conversion

- Once a transient is created and has enough voltage to cause the following circuit elements to respond to the transient as a signal then the DSET can propagate in the device through significant numbers of device nodes.
  - The transient becomes indistinguishable from true normal signals.
  - Can be incorrectly accepted as data to be stored if it arrives at a store element coincident with a clock signal edge.
  - The conversion of transients into erroneous data is dependent on the clock frequency:
    - -Static CMOS Logic – Error rate proportional to frequency.
    - -Dynamic CMOS Logic – Error rate decreases with frequency.
  - SET propagation is dependent on the duration of the SET. The minimum duration required for SET propagation [i.e. the critical duration (also referred to as the critical width)] has decreased in proportion to the square of the technology feature size.
- Types of DSET include:
  - Data input transients.
  - Clock line transients.
  - Synchronous and Asynchronous control line transients.

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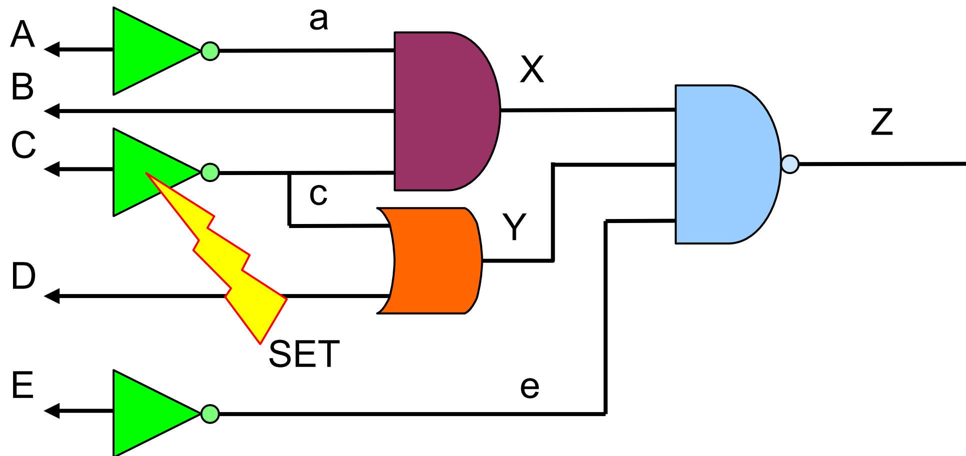
DSET Propagation & Conversion



Set	1	2	3	4	5	6	…
A	1	0	0	0	0	1	
B	1	1	1	1	1	1	
C	1	0	0	0	1	1	
D	1	1	0	0	0	0	
E	1	0	0	1	0	0	
a	0	1	1	1	1	0	
c	Λ	V	V	V	Λ	Λ	
e	0	1	1	0	1	1	
X	0	V	V	V	Λ	0	
Y	1	1	V	V	Λ	Λ	
Z	1	Λ	Λ	1	V	1	

- The SET exists within a logical configuration and signal propagations are dependent on the circuit condition at the time of the event.
- This example is very simplistic – real circuits need consideration of circuit time delays in addition to the logic and thus both the amplitude and durations of the transients are important.
  - These considerations define how many nodes a transient will pass through in the circuit.

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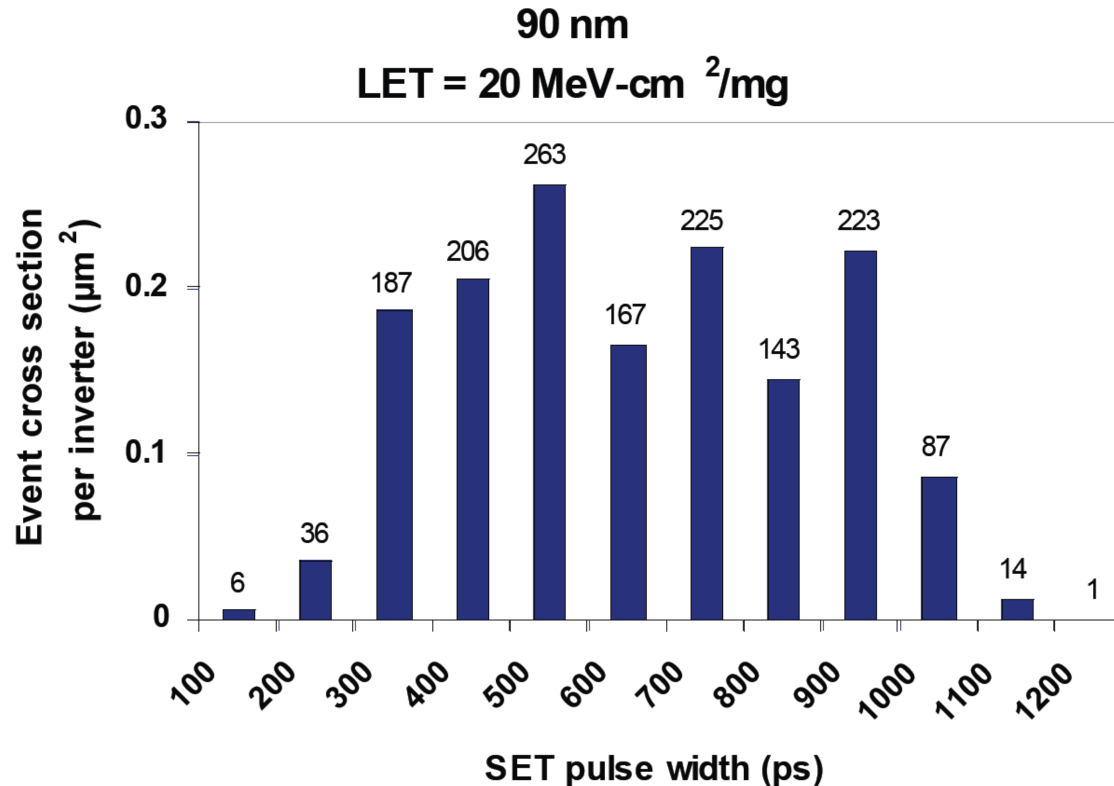
SET Pulse Durations (Widths)



- Results presented by B. Narasimham (Vanderbilt University) show the range of SET durations for a given particle LET in a 90 nm technology
- Variations are attributable to:
  - The effects of strike location.
  - The effects of charge collection characteristics.
  - The effects of circuit bias conditions.

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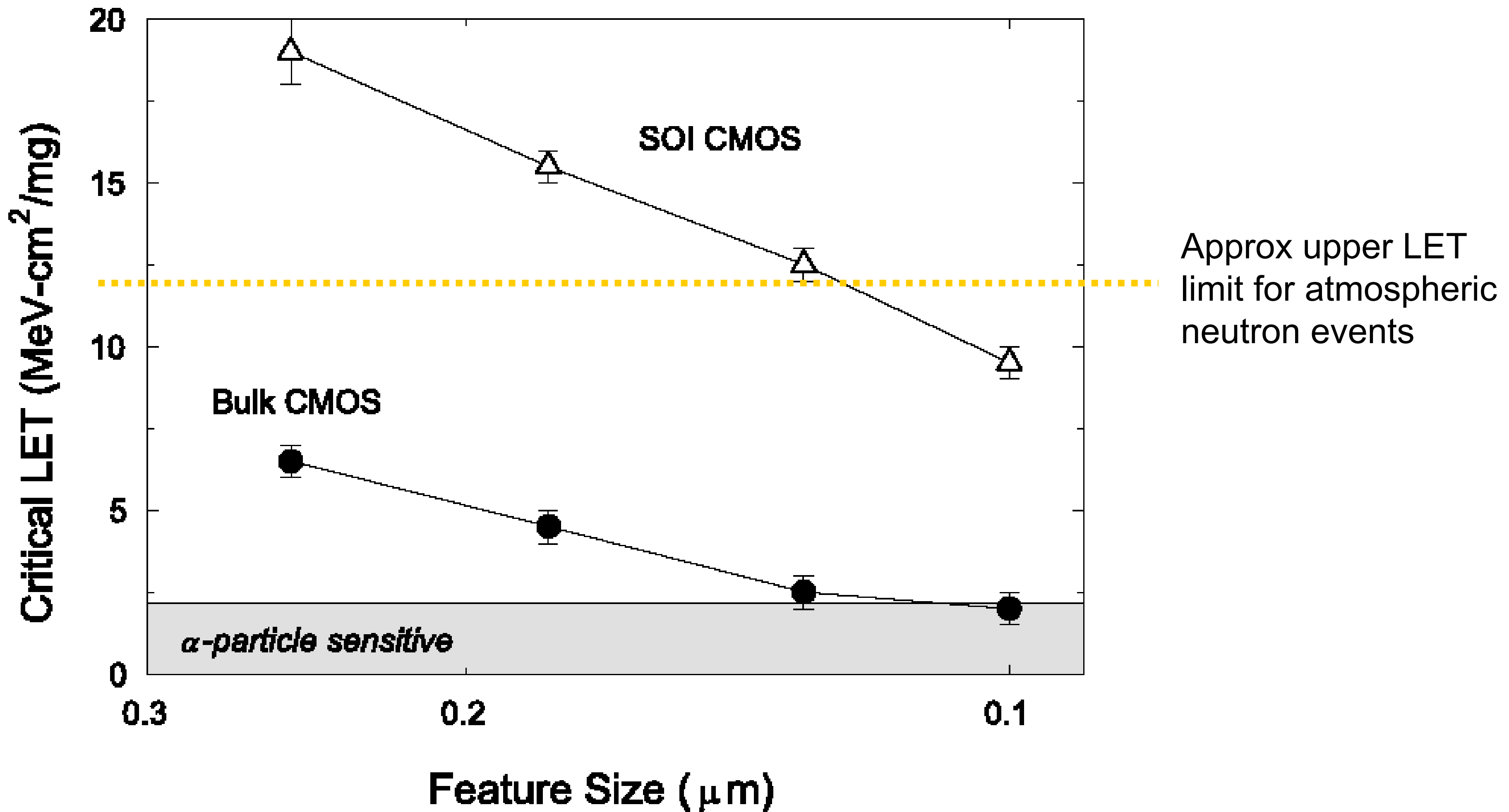
Increasing DSET sensitivity with decreasing feature size



Source: Paul Dodd et al, Production and propagation of single-event transients in high-speed digital logic IC's, IEEE Transactions on Nuclear Science, December 2004

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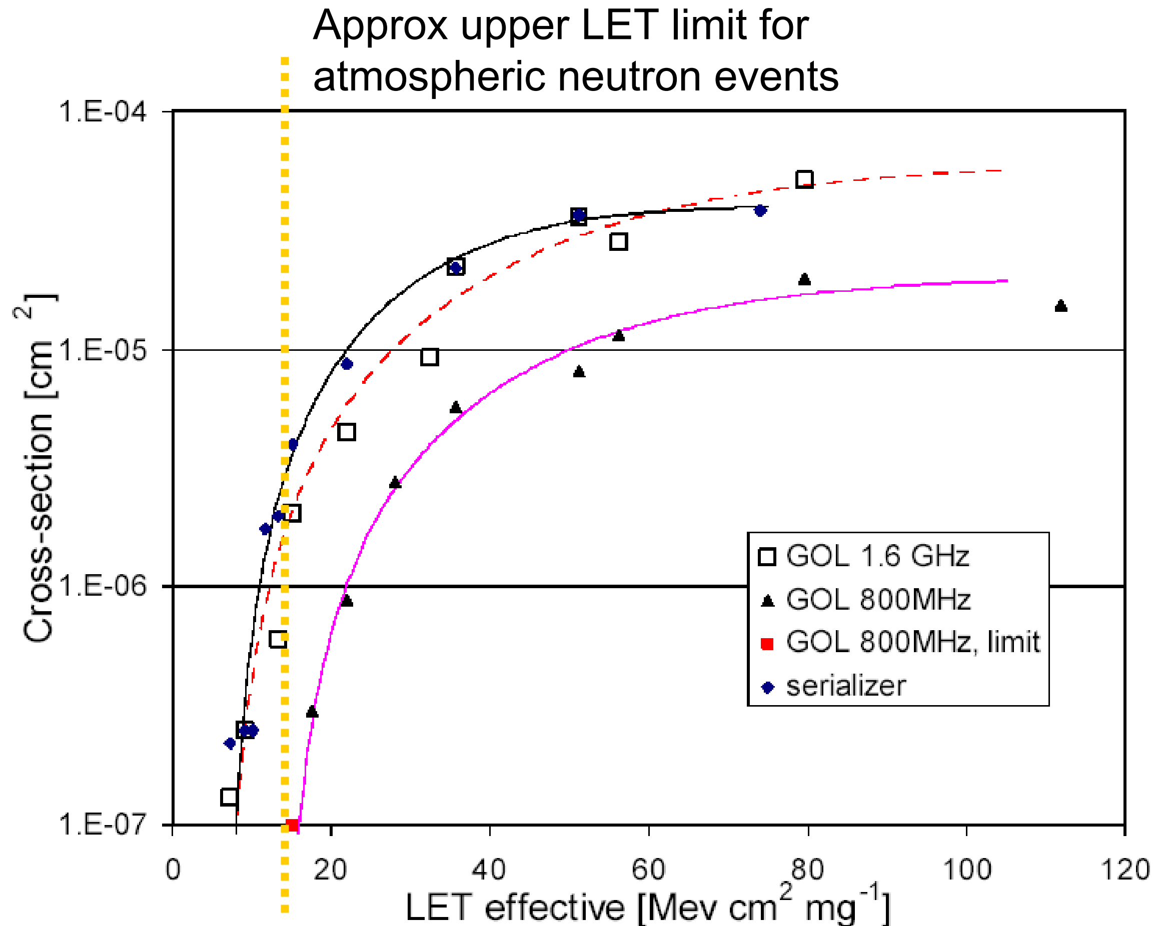
Databus chipsets are showing SEE sensitivity in the GHz range

SEE cross-sections for the Gigabit Ethernet GOL and serializer (CERN data)



Source: ***P. Moreira et al, G-Link and Gigabit Ethernet Compliant Serializer for LHC Data Transmission, IEEE Nuclear Science Symposium Conference Record, 2000***

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Future Key Issues

- As digital frequencies move across the 1GHz region
  - DSET's may predominate over SEU's and other SEE's
  - It will be crucial to test at operational frequencies
    - Due to frequency dependencies
  - & in operational configurations (to some extent)
- Will this require abandonment of component testing?
  - testing chips embedded within PCB's, MCM's or other sub-systems?
  - Testing individual chips or the whole sub-system?
- ASET's will continue to be a reliability barrier for sensitive instruments
  - We need design strategies to cope with ASET's
    - Redundancy, error checking etc?
  - This will be crucial to improving instrument sensitivities for space applications

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