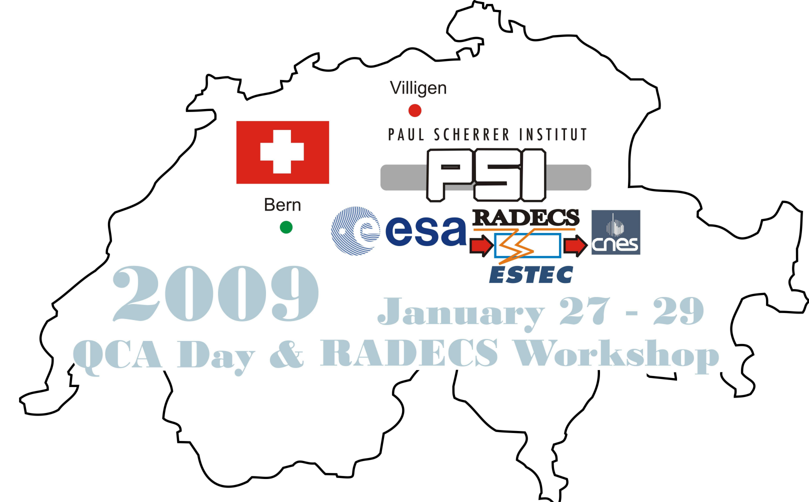

Single Event Transients in Digital Circuits

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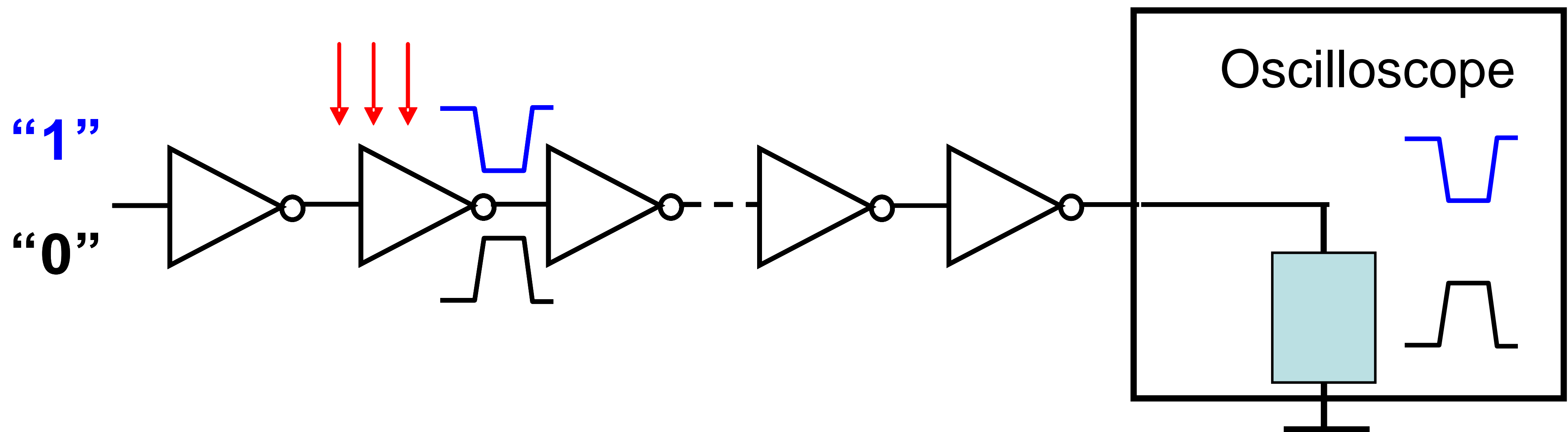
Chains of inverters were fabricated in bulk and SOI with different designs

- 180nm and 130nm bulk chains
- 130nm SOI chains, four designs, with body contacts

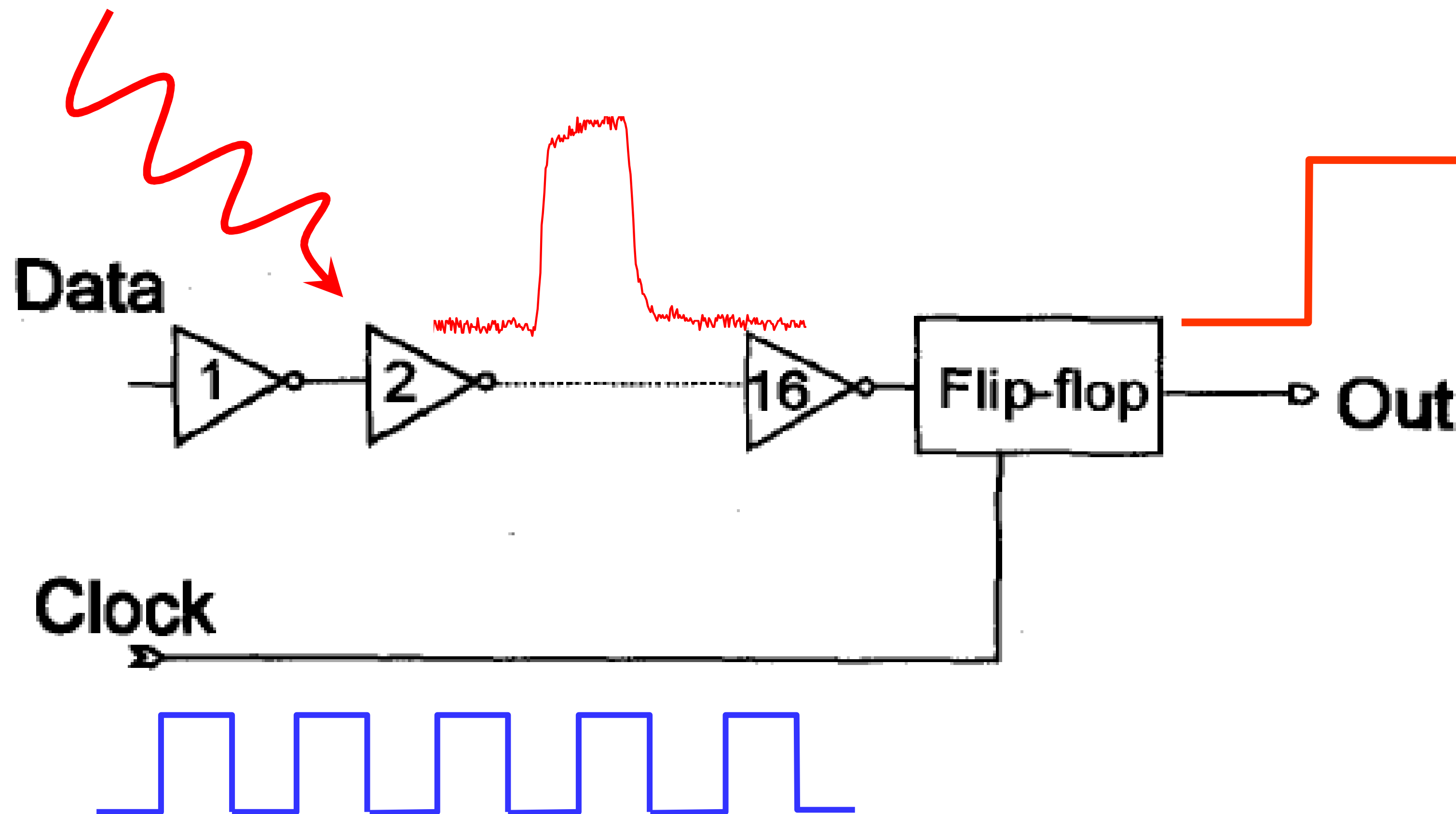
NMOS width W_N (µm)	0.3	0.9	1.8	2.7
PMOS width $W_P = 2 \times W_N$				

Broad beam ions — *IPN Orsay* — *RADEF Jyväskylä*

Focused pulsed laser — *IMS Bordeaux* — *NRL Washington*

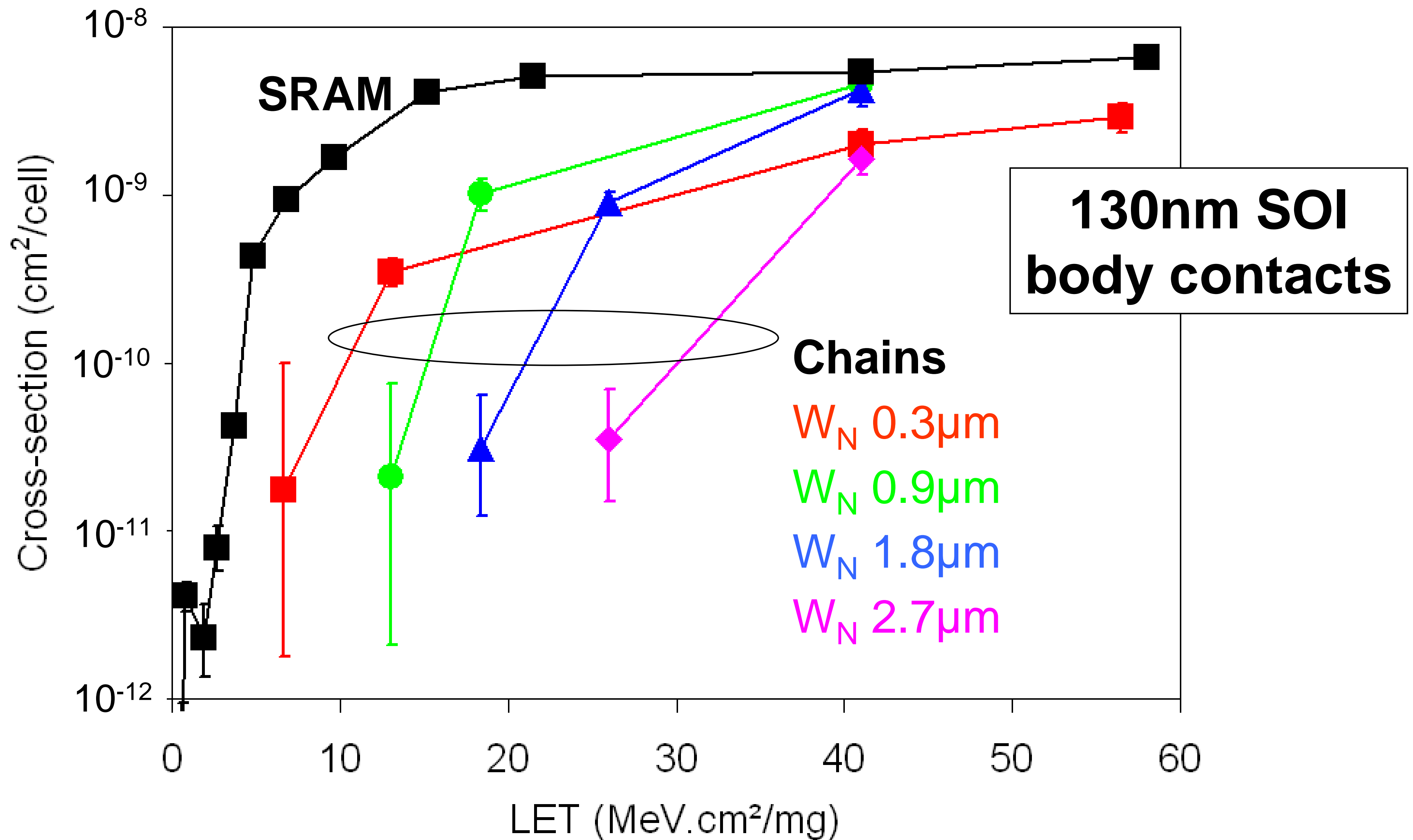


The unattenuated propagation of SETs is a growing concern in high-speed logic ICs with technology downscaling

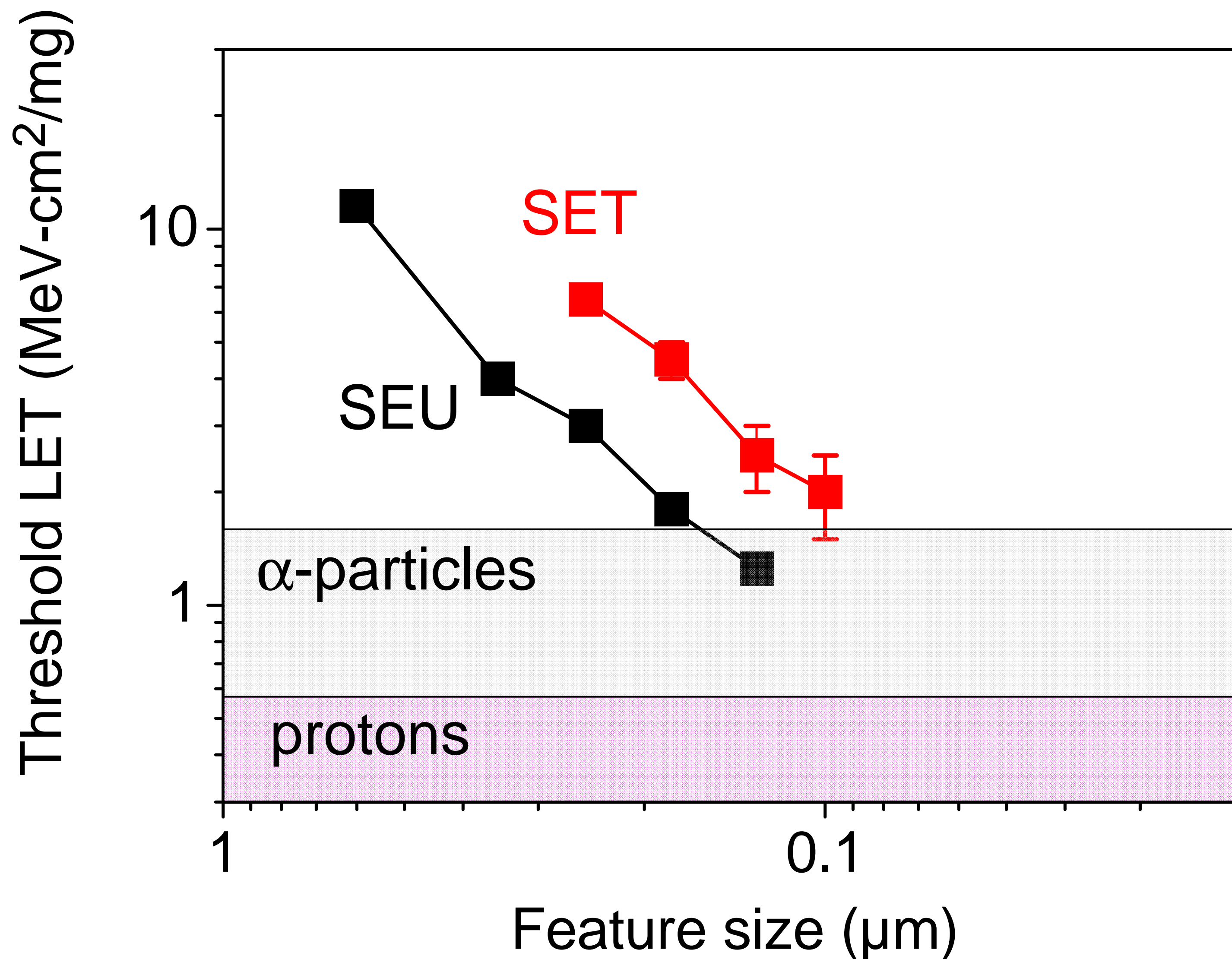


[S. Buchner, TNS 1997]

SEU versus SET sensitivity



Technologies below the 90-nm node will be sensitive to SETs induced by terrestrial α-particles



P. E. Dodd, , et al. TNS 2004

The minimum widths of unattenuated SETs are narrower with technology downscaling

Critical transient width (ps)

1000

100

10

1

0.1

Feature size (µm)

Mavis02

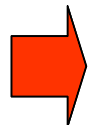
Dodd04 ● Bulk

△ SOI

Ferlet06

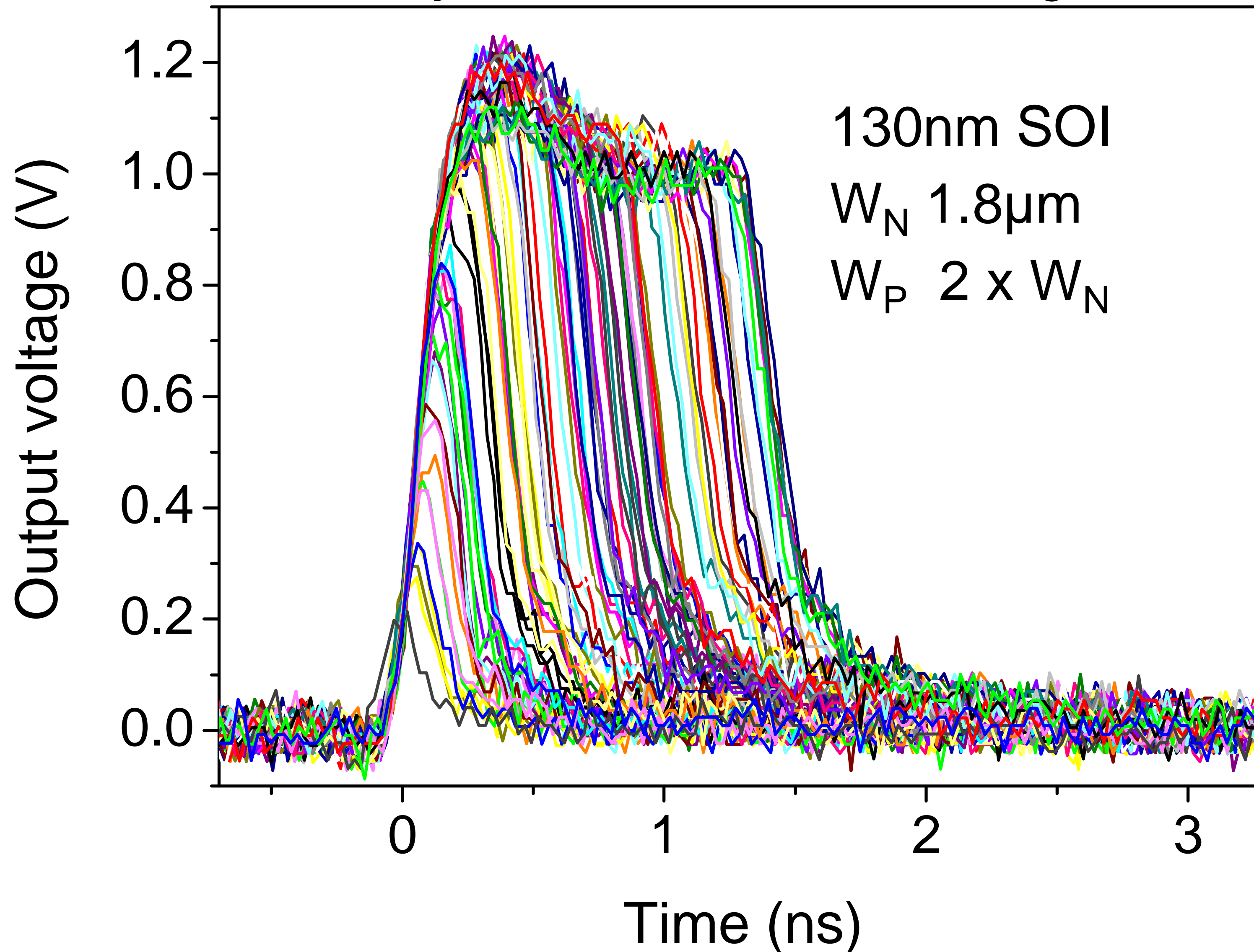
◆ Bulk

◇ SOI

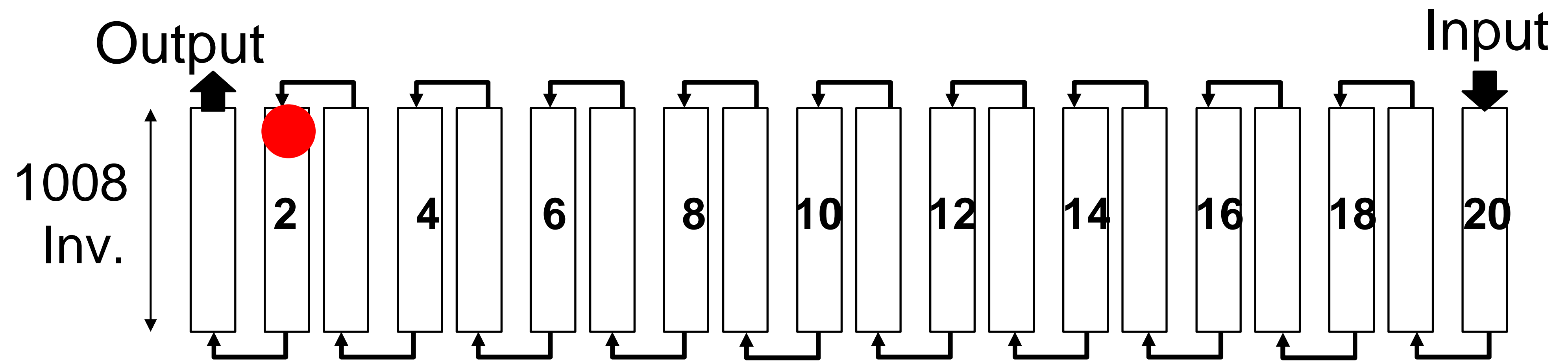


A large range of SET width is expected to propagate in logic circuits fabricated in highly scaled technologies

Large distributions of SET pulse widths are measured at the output of inverter chains

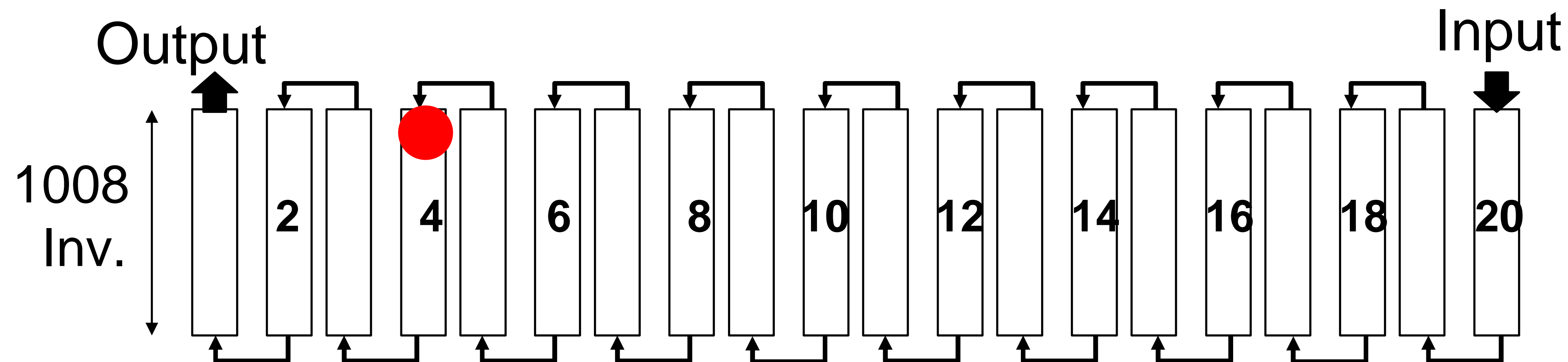


Typical runs count at least 200 transients to get enough statistics

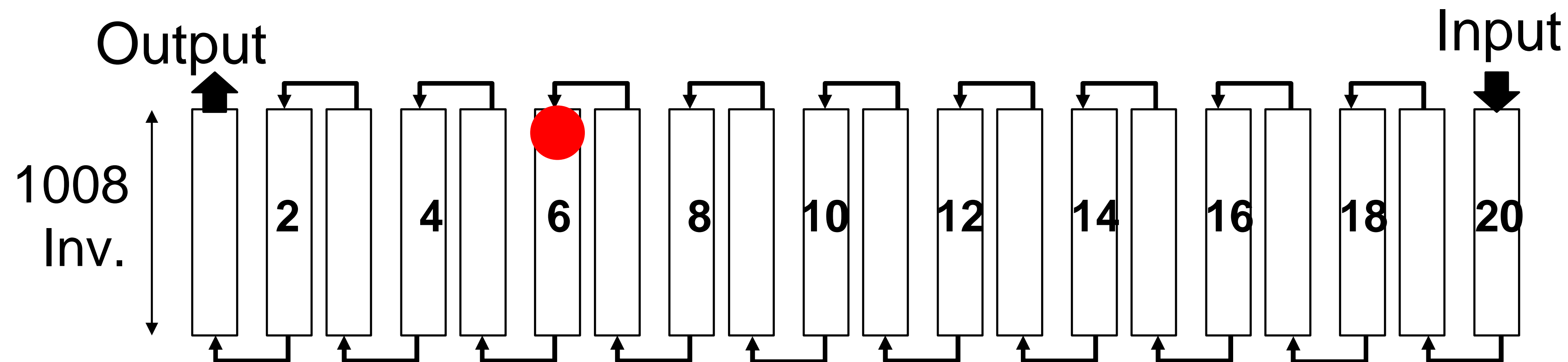


1.2
0.6
0.0
Output voltage (V)
0
200
400
600
Time (ns)

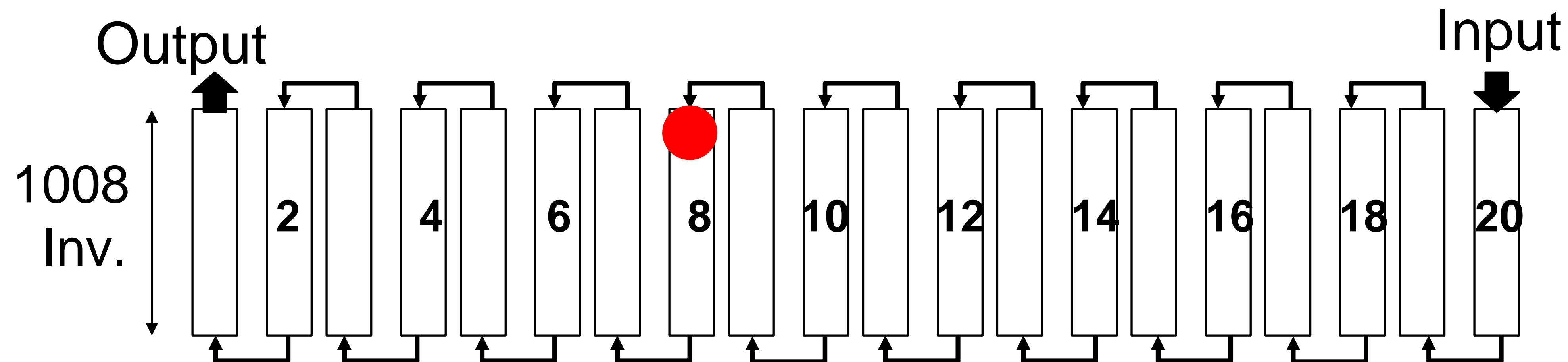
130nm bulk chain
Focused pulsed laser


Output
Input
1008
Inv.
2
4
6
8
10
12
14
16
18
20

Output voltage (V)
1.2
0.6
0.0
0
200
400
600
Time (ns)


Output
Input
1008
Inv.
2
4
6
8
10
12
14
16
18
20

Output voltage (V)
1.2
0.6
0.0
0
200
400
600
Time (ns)

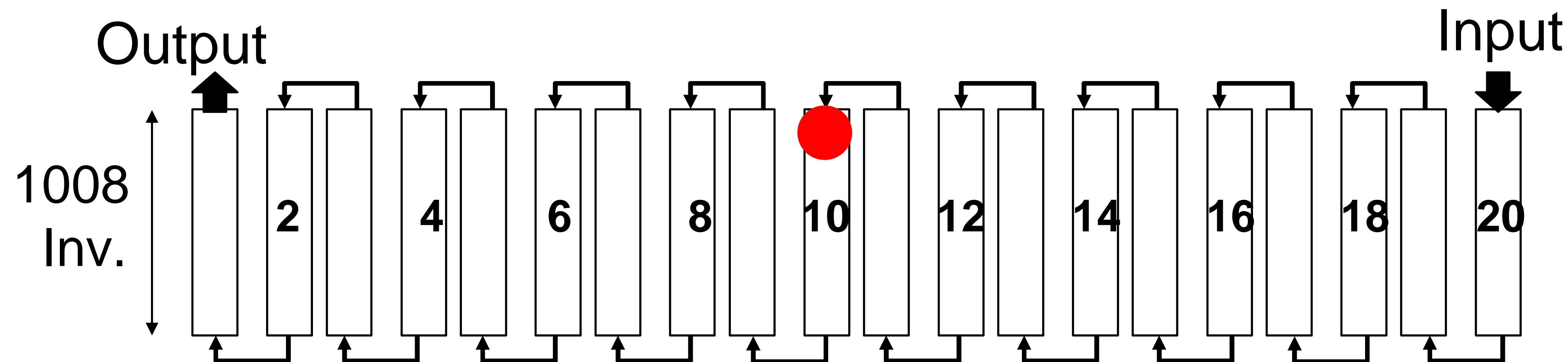


Output voltage (V)

1.2
0.6
0.0

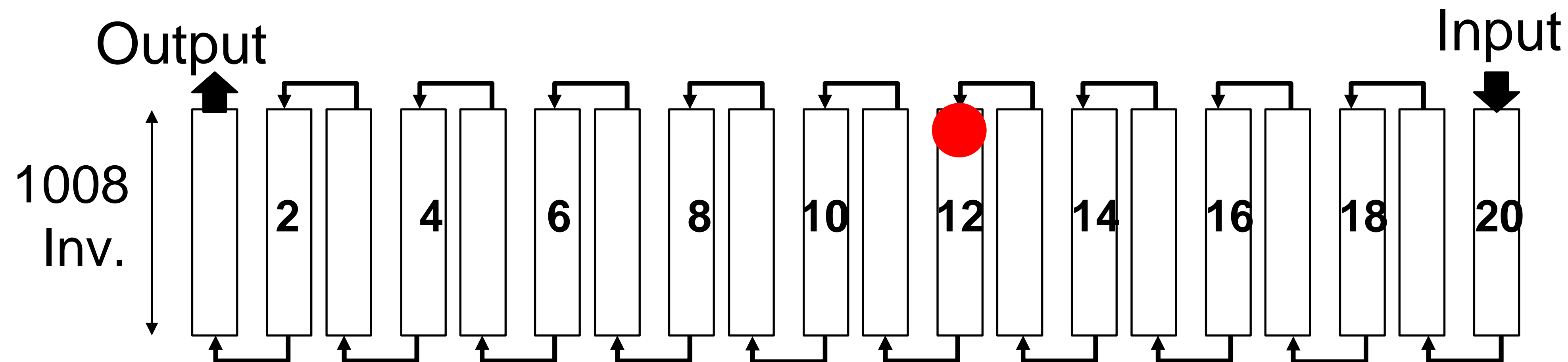
0
200
400
600

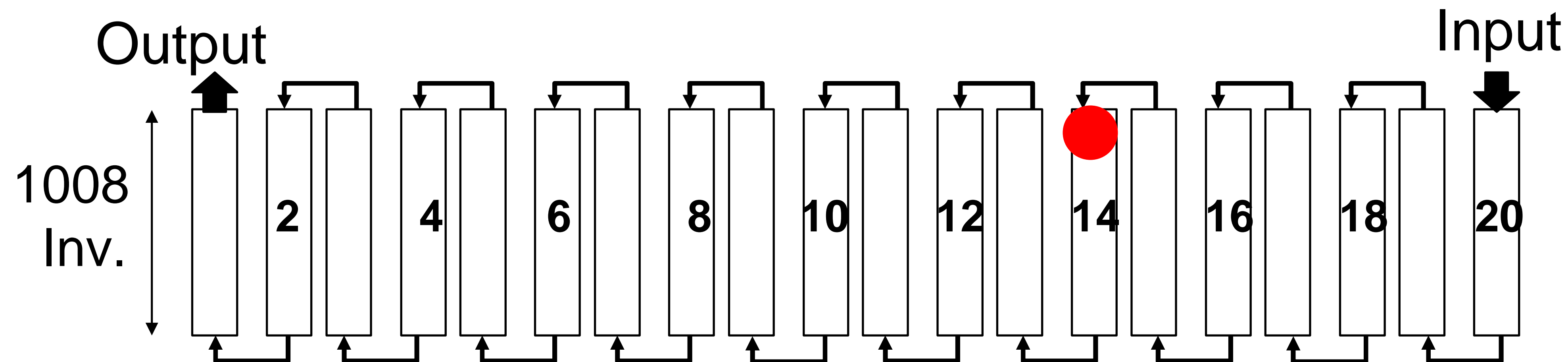
Time (ns)



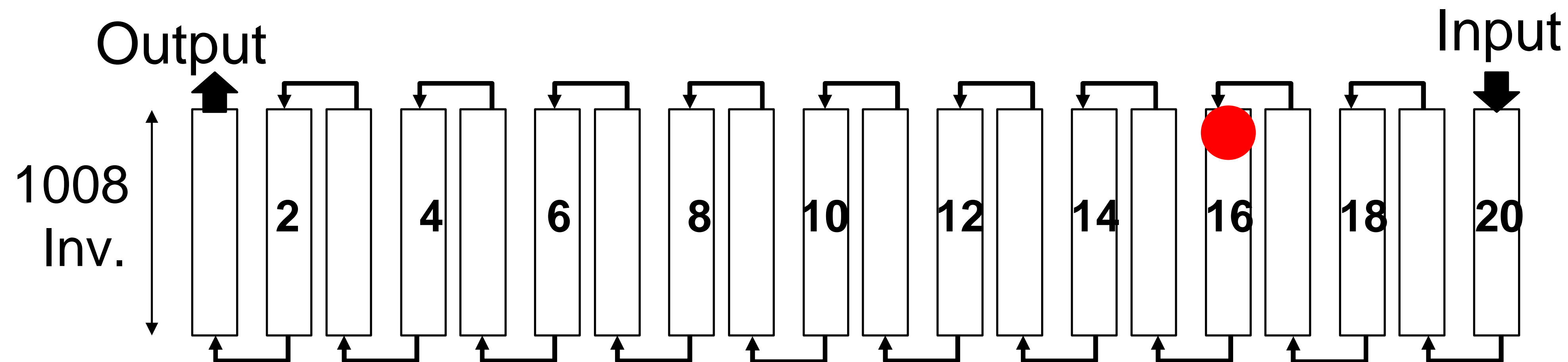
Output
Input
1008
Inv.
2
4
6
8
10
12
14
16
18
20

Output voltage (V)
1.2
0.6
0.0
0
200
400
600
Time (ns)

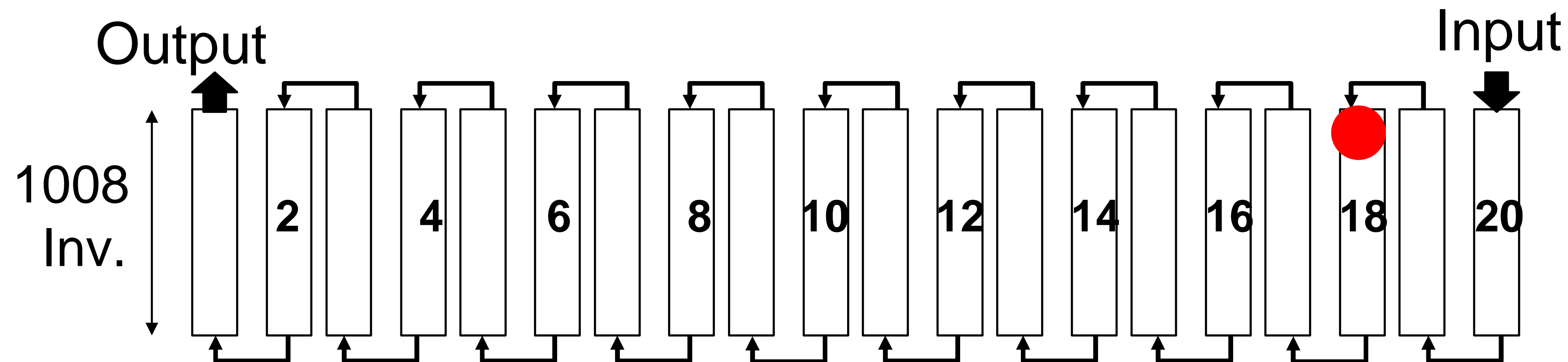

Output
Input
1008
Inv.
2
4
6
8
10
12
14
16
18
20
1.2
0.6
0.0
Output voltage (V)
0
200
400
600
Time (ns)


Output
Input
1008
Inv.
2
4
6
8
10
12
14
16
18
20

1.2
0.6
0.0
Output voltage (V)
0
200
400
600
Time (ns)



1.2
0.6
0.0
Output voltage (V)
0
200
400
600
Time (ns)



Output voltage (V)

1.2

0.6

0.0

0

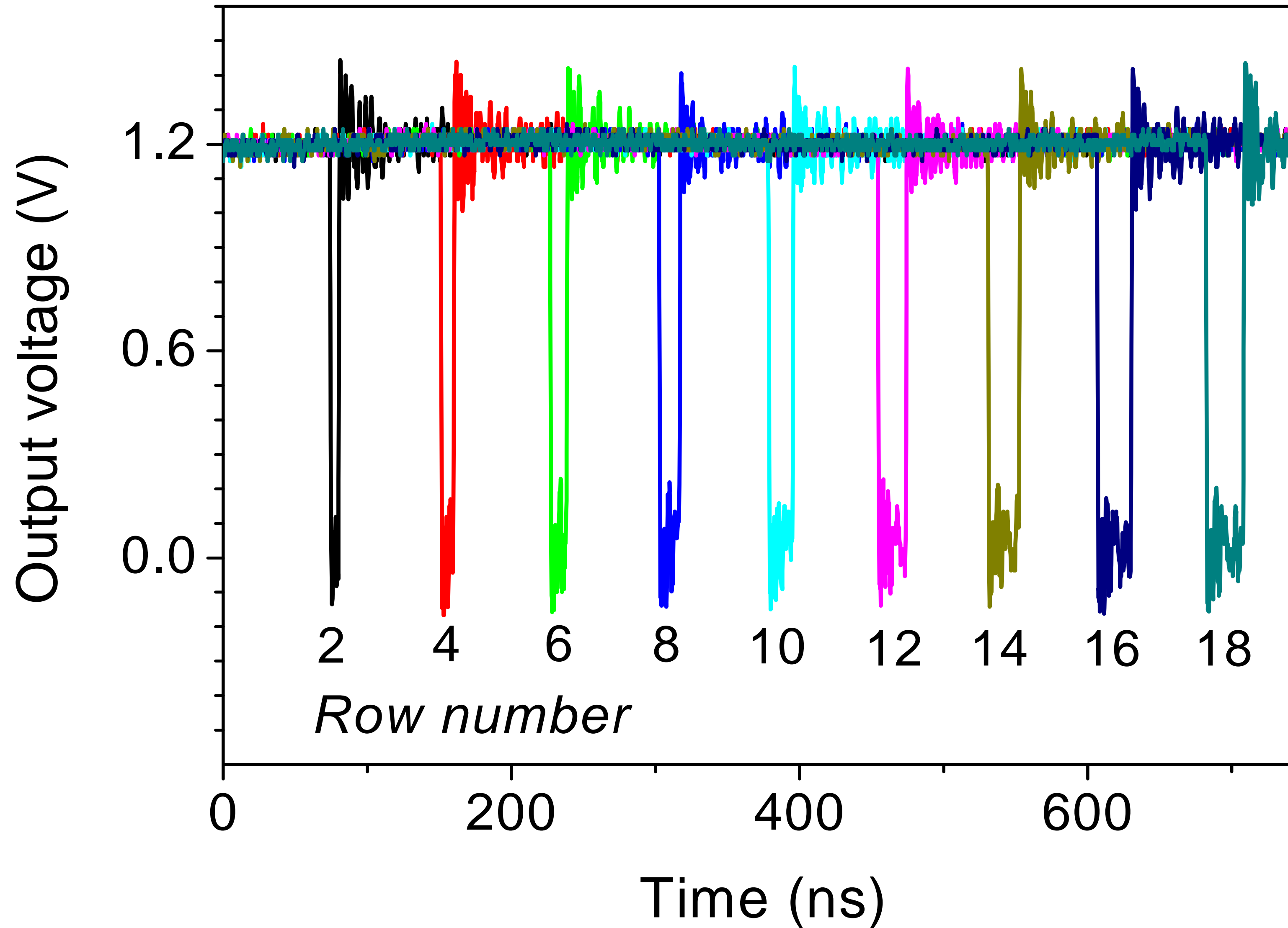
200

400

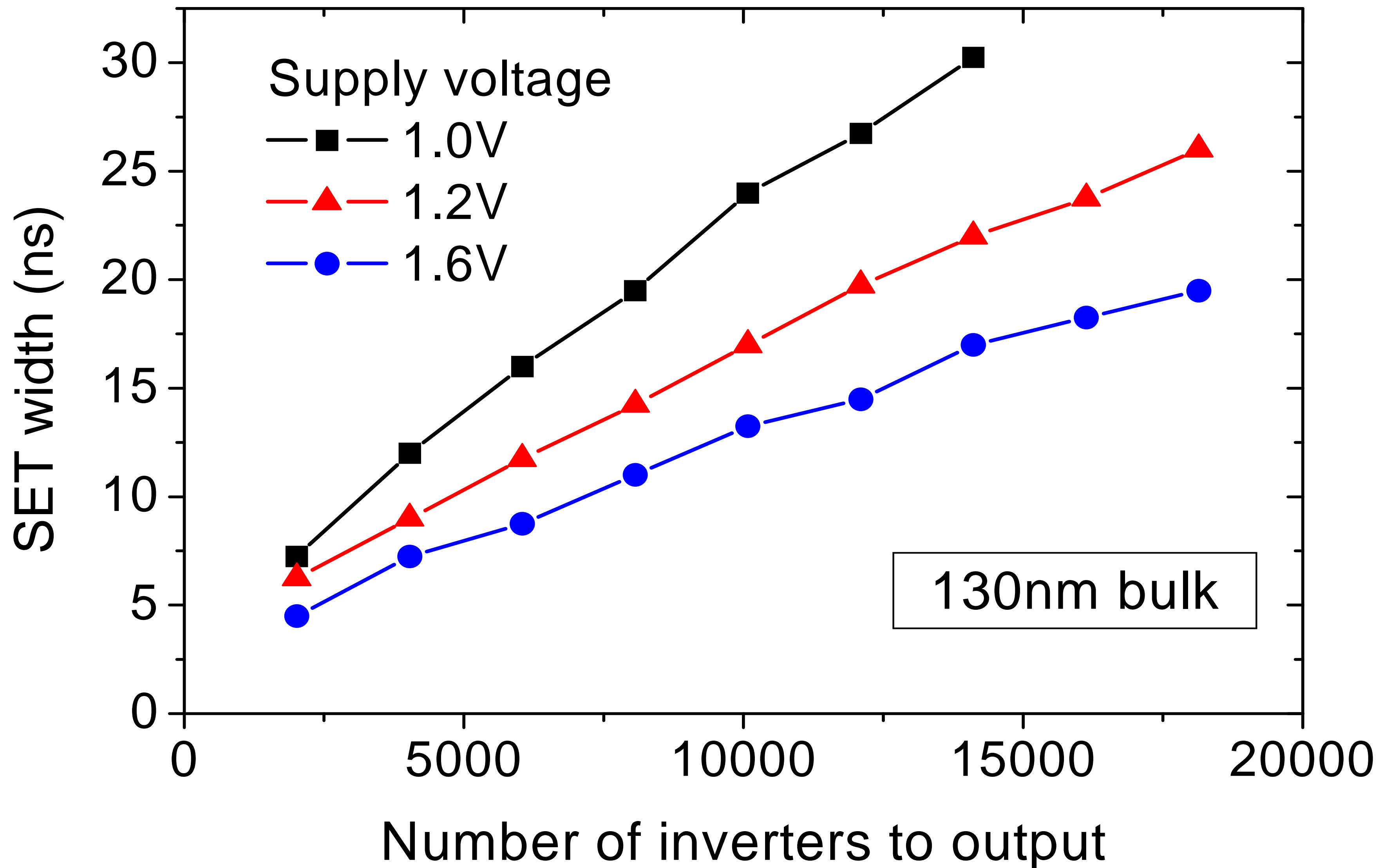
600

Time (ns)

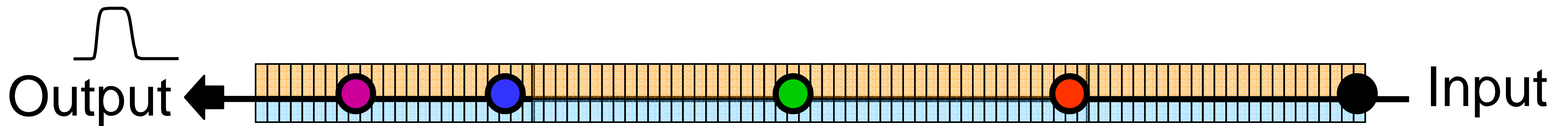
The bulk chain exhibits an obvious Propagation-Induced Pulse Broadening (PIPB) effect



Pulse broadening is enhanced at low supply voltage



130nm PD SOI with body contacts also exhibits pulse broadening



Inverter number

105

205

405

605

797

Output voltage (V)

1.2

0.6

0.0

0

5

10

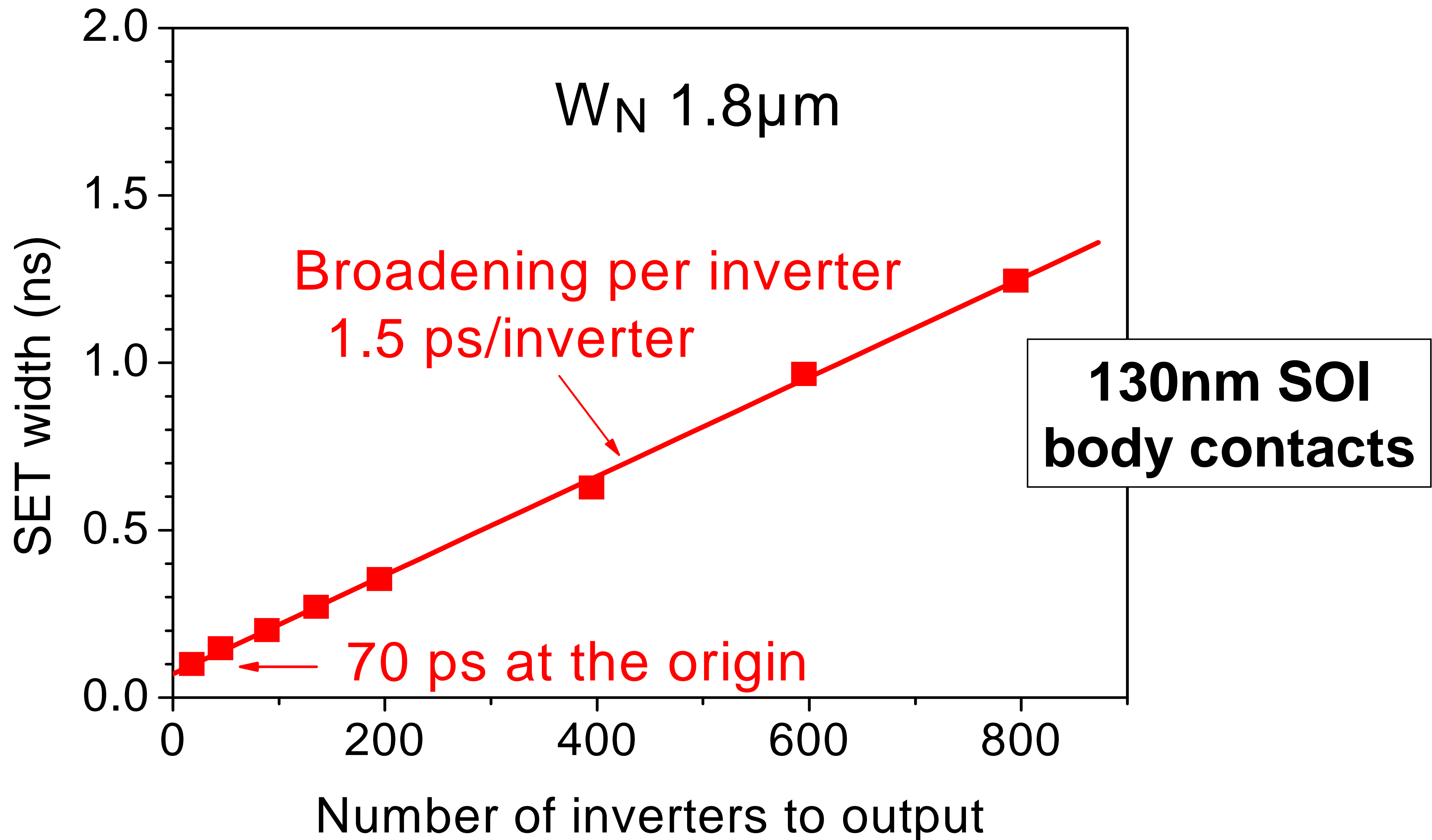
15

20

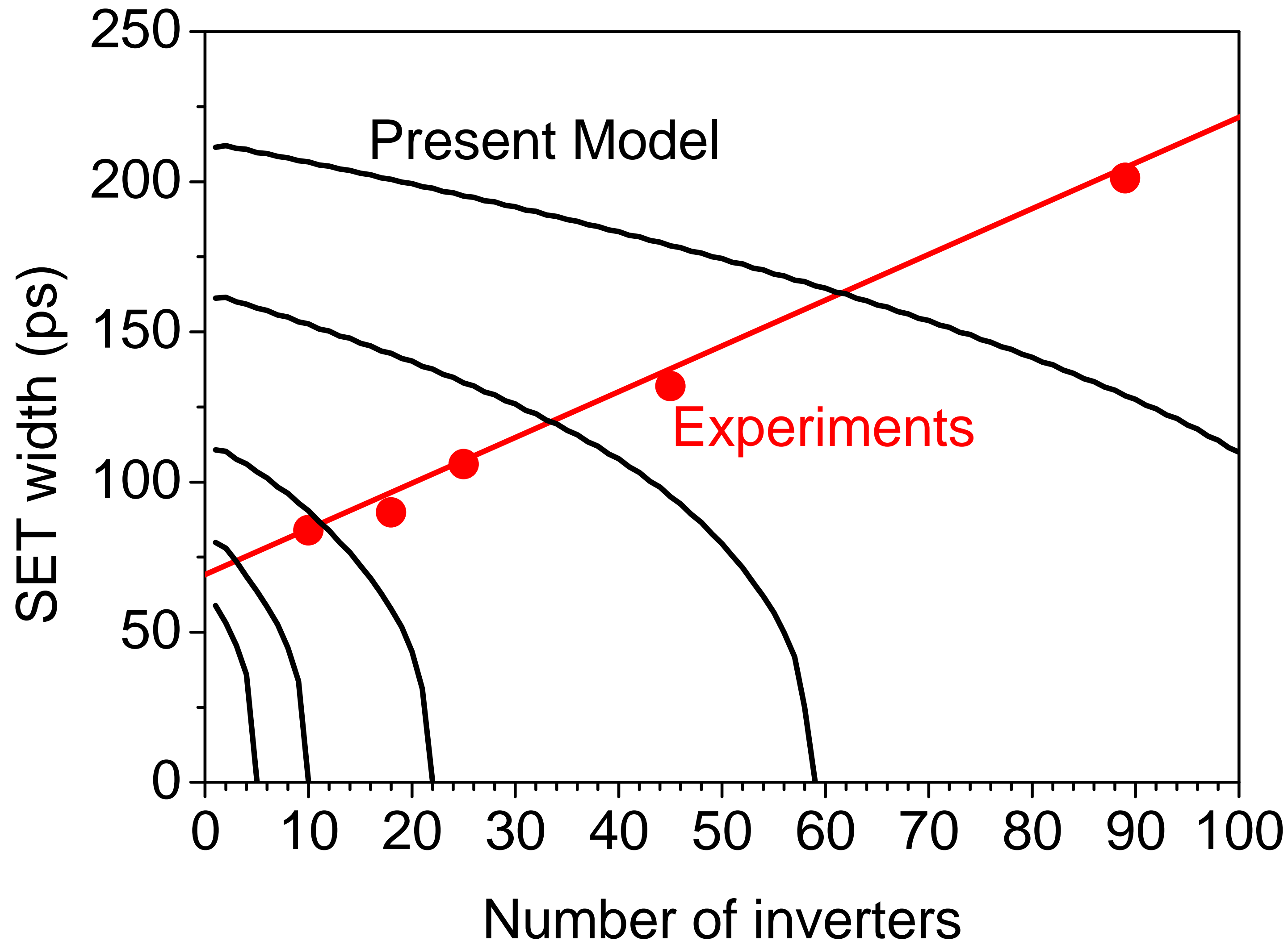
25

Time (ns)

The broadening per inverter and the "original" SET width are extracted from laser experiments

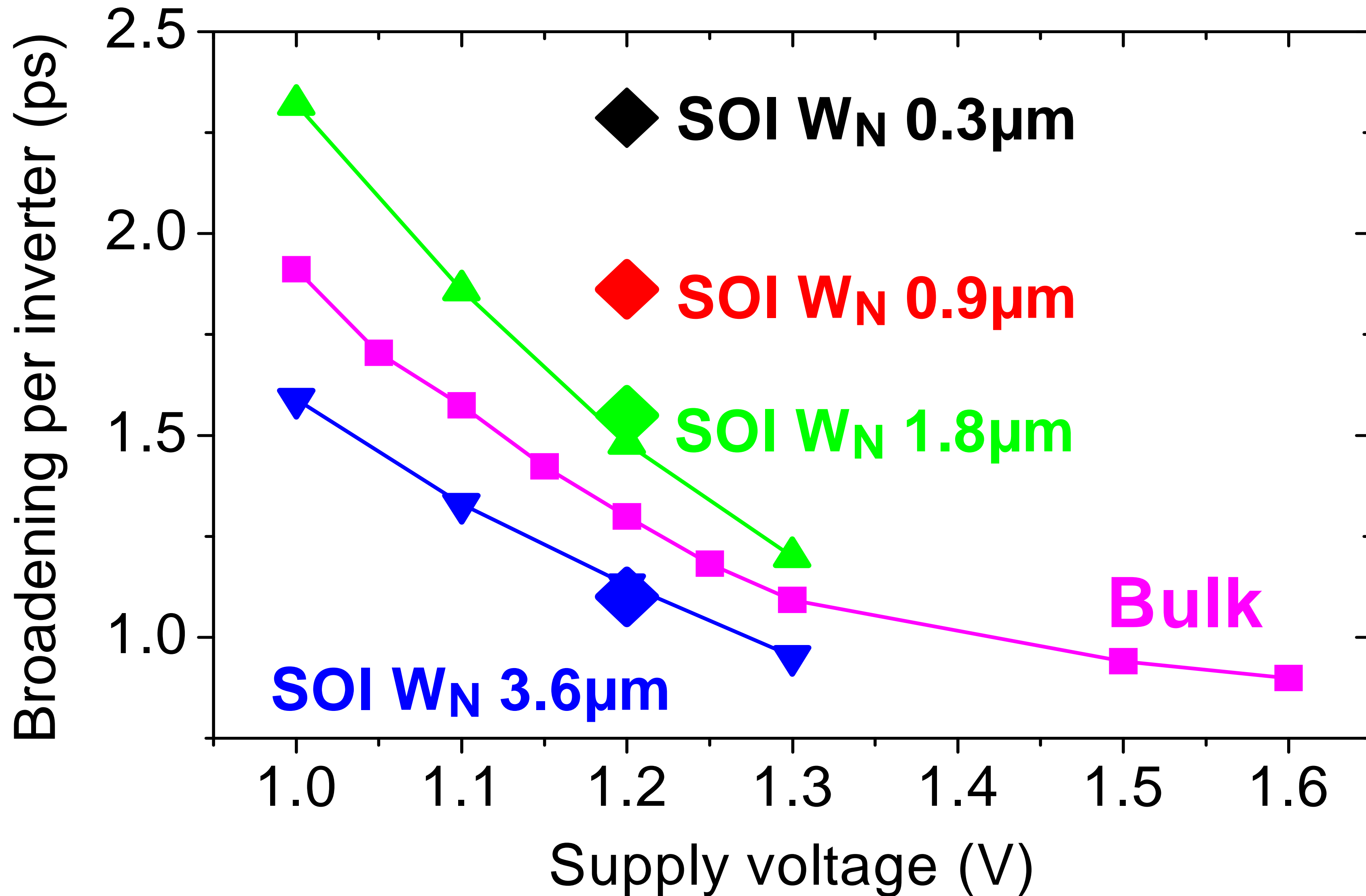


The SET sensitivity is largely underestimated by standard models

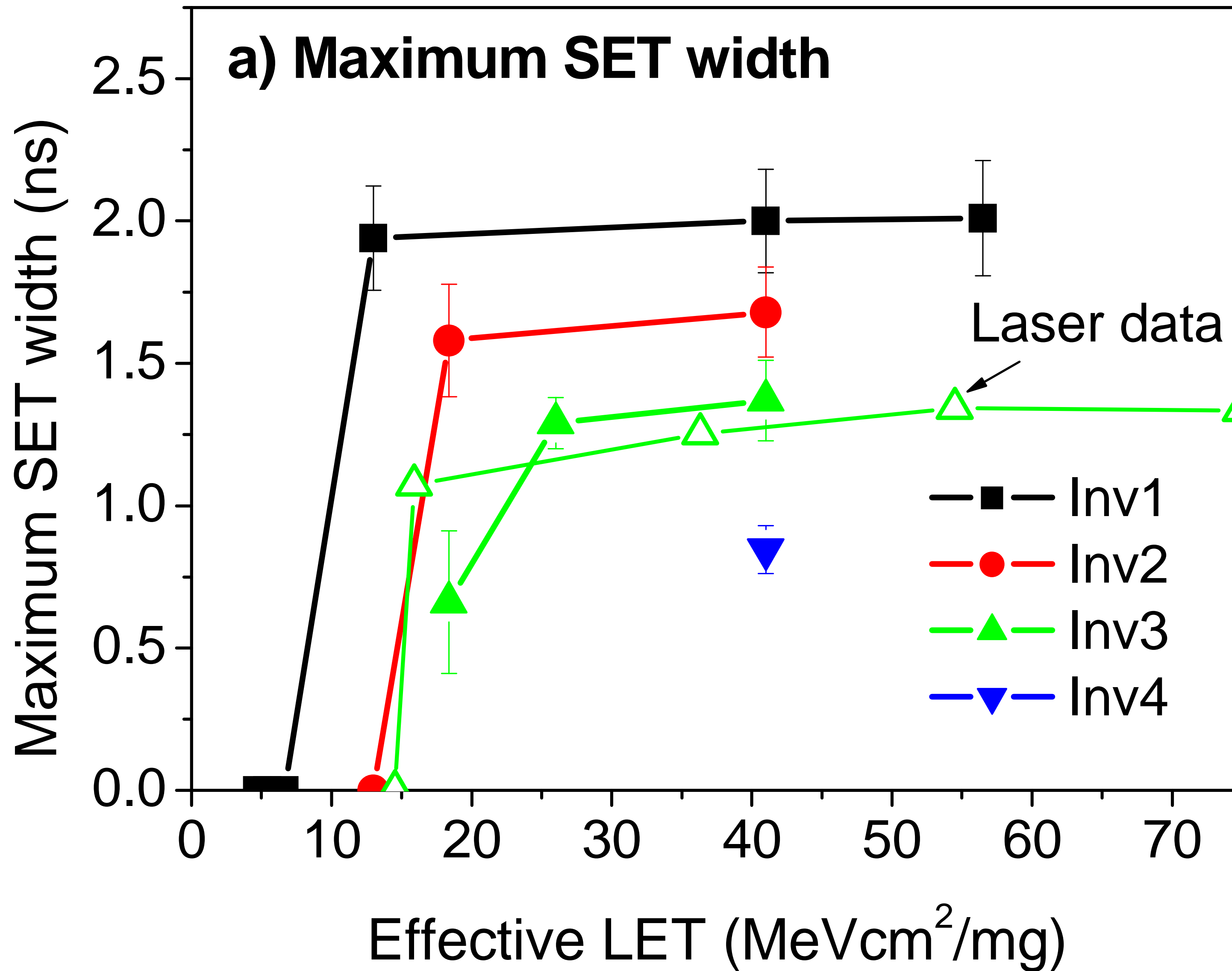


The broadening effect contributes to enhanced the SETs sensitivity

Heavy ion tests are consistent with laser data

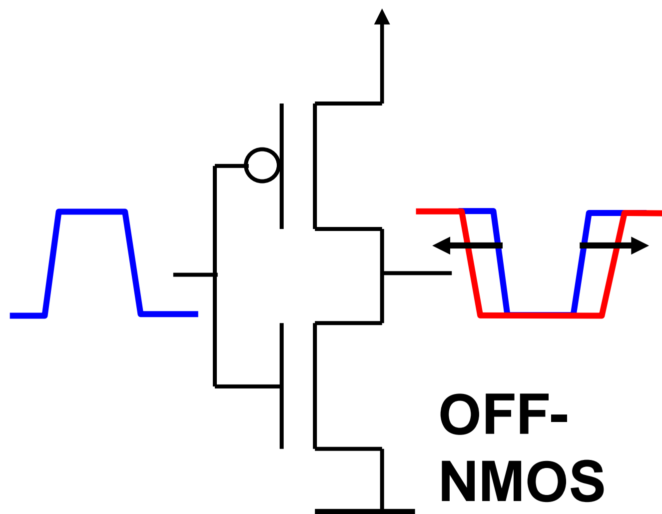


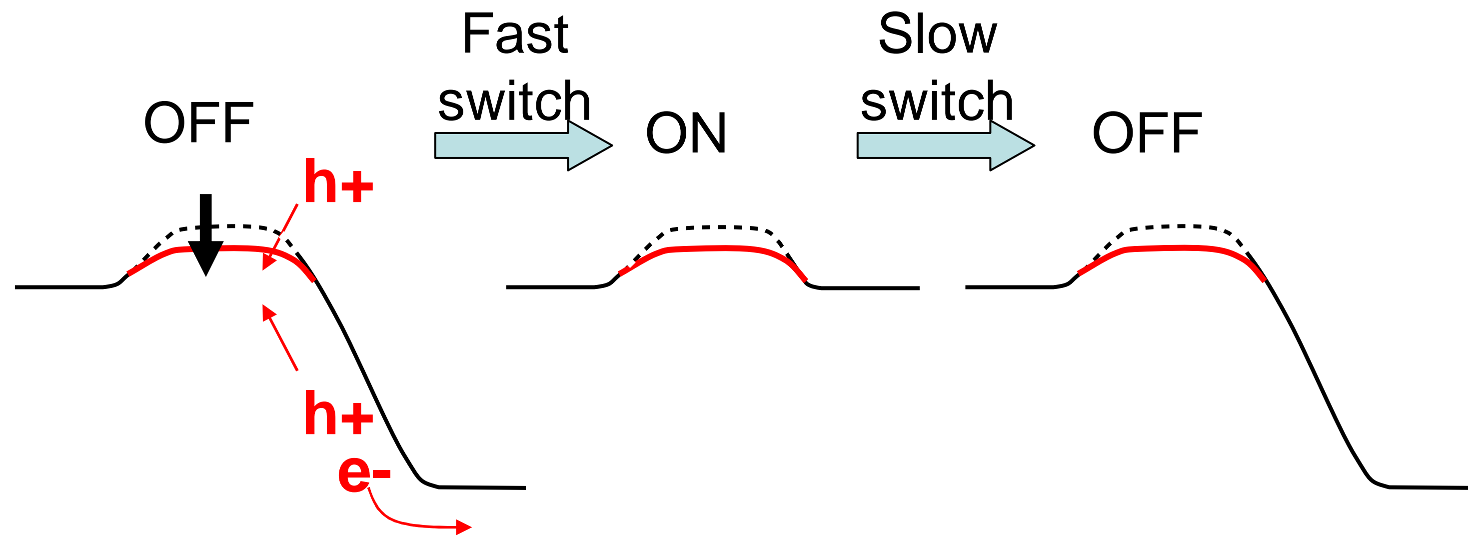
Empirical rule: 1pJ = 1MeVcm²/mg
Front side laser irradiation 590nm



Body charging in <u>bulk and SOI</u> OFF-state transistors is responsible for broadening

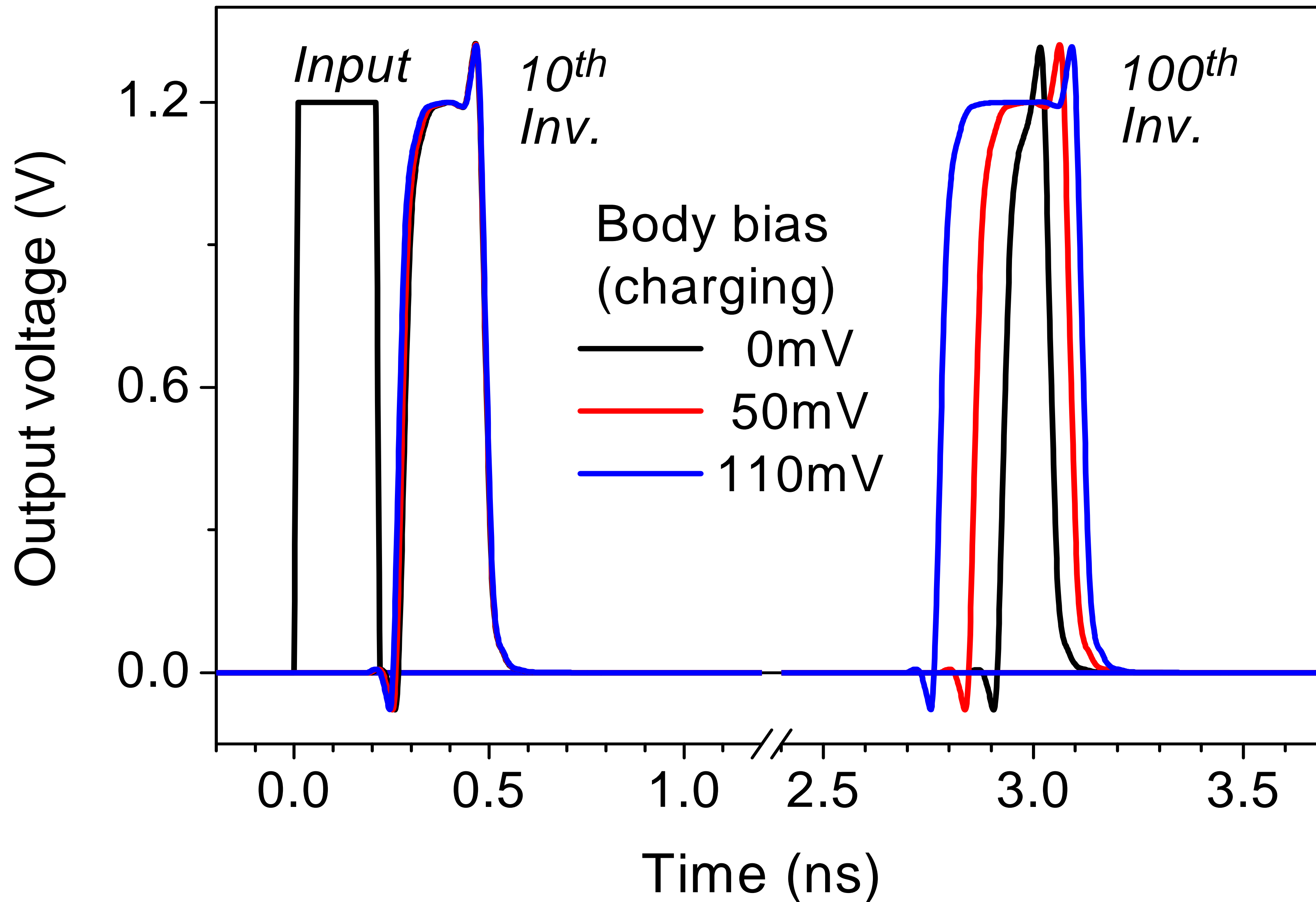
The body charging lowers the threshold voltage of the OFF-state transistors



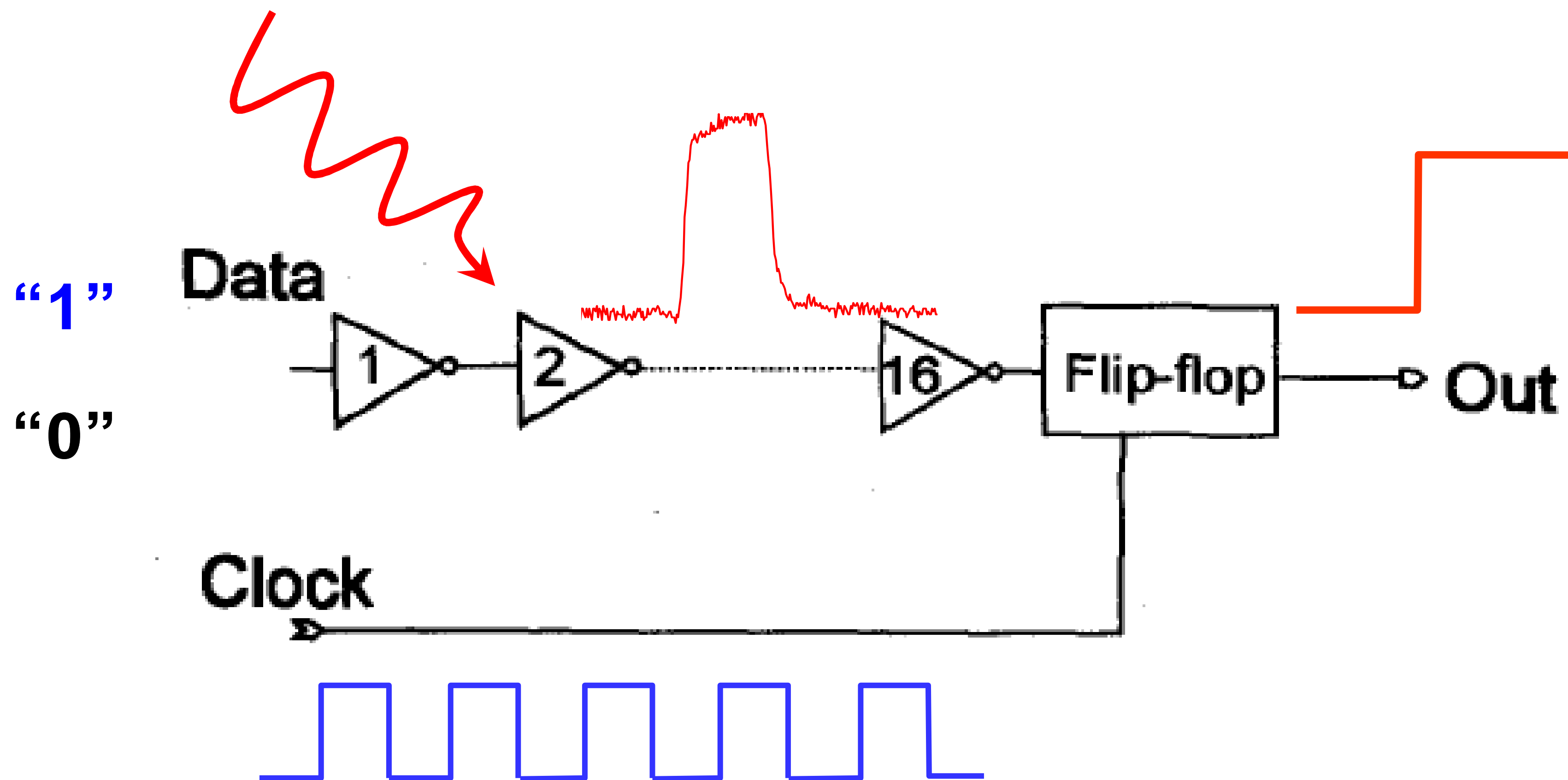


Impact ionization
Gate oxide leakage

When body charging is taken into account pulse broadening is reproduced by simulation

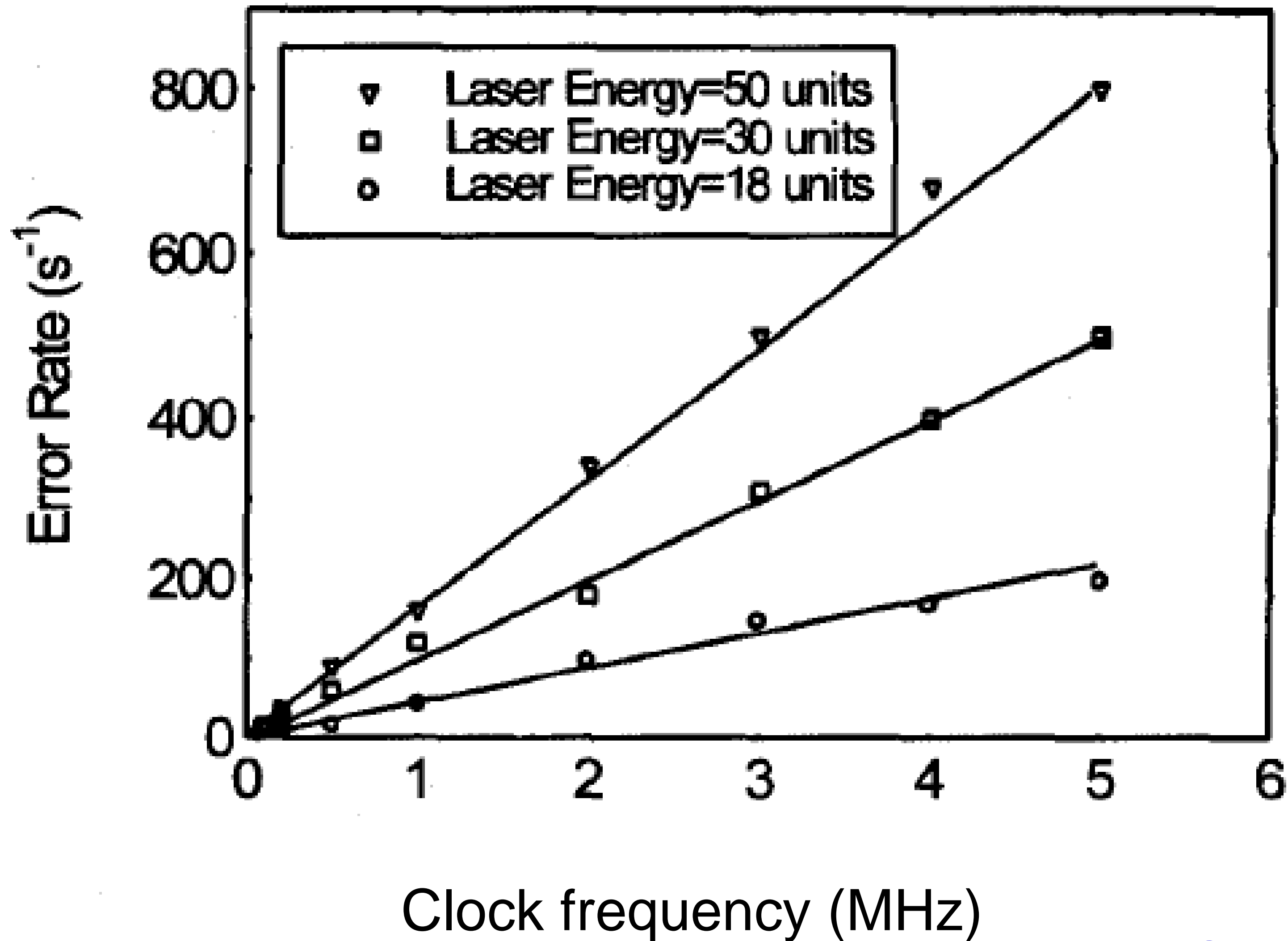


What are the effects of
- the clock frequency?



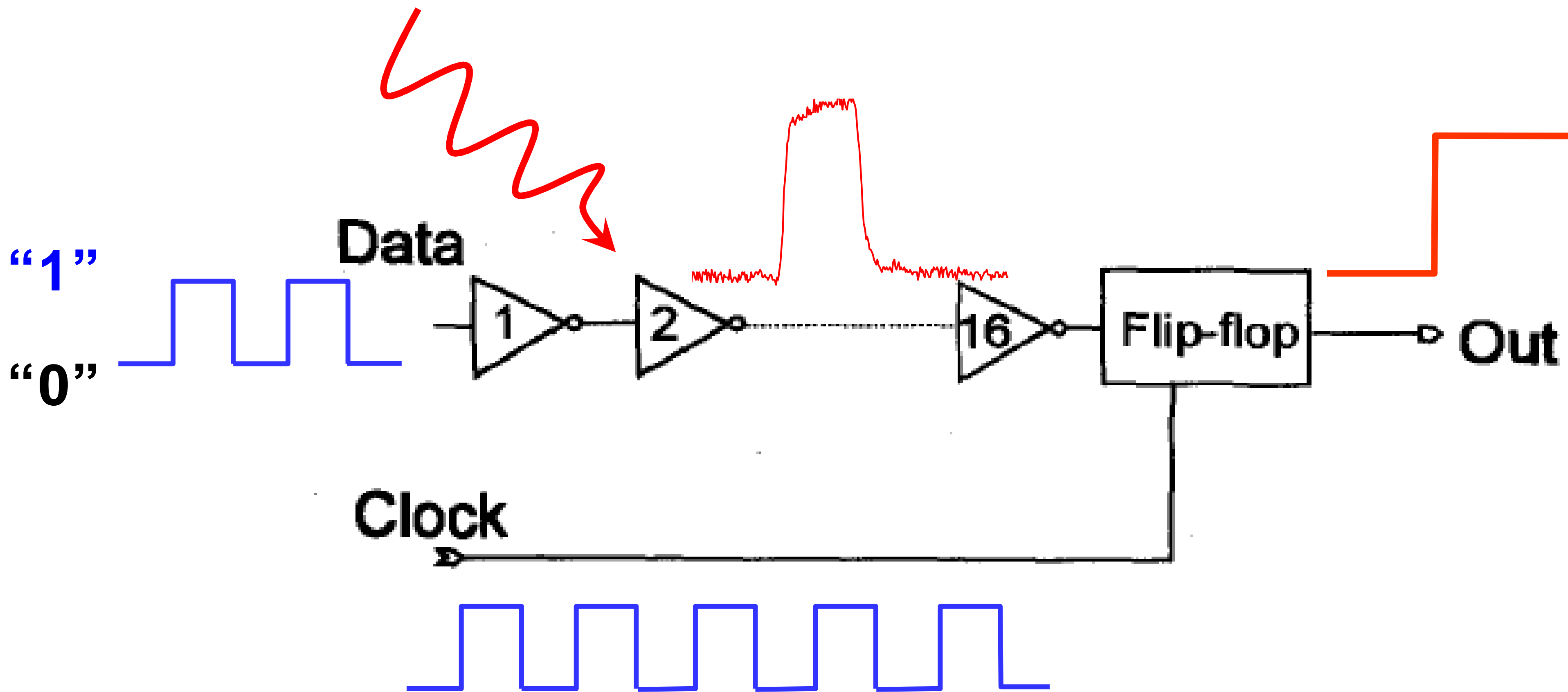
[S. Buchner, TNS 1997]

The probability of SET capture increases linearly with the circuit clock frequency



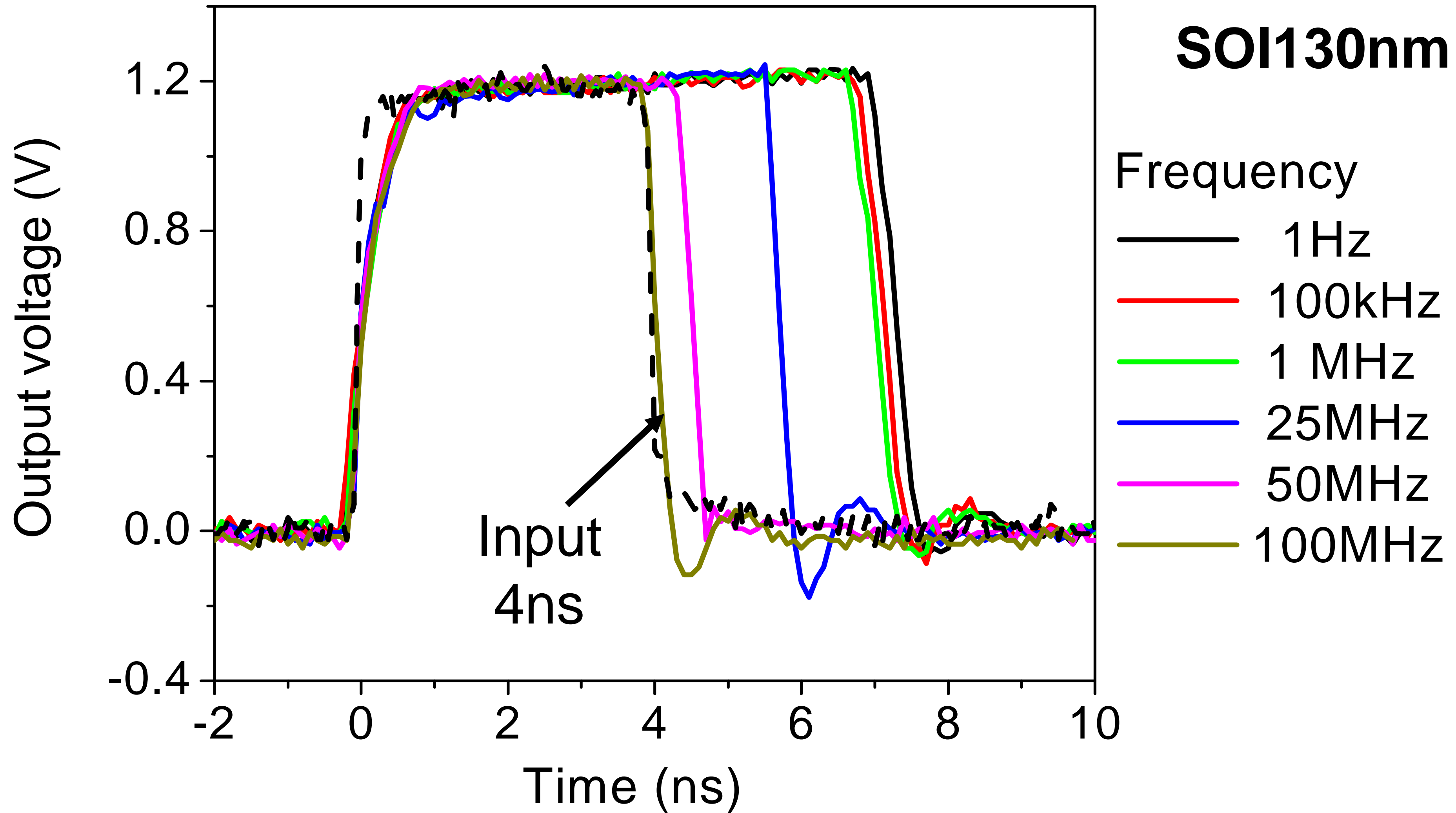
[S. Buchner, TNS 1997]

What are the effects of
- the clock frequency?
- the data frequency?



[S. Buchner, TNS 1997]

The pulse broadening (i.e. the SET sensitivity) decreases at high data frequency (≥ 100MHz)



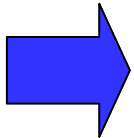
Pulse broadening is a dynamic effect related to the inverter history

Summary

- **SET broadening occurs in both bulk and SOI**
  - SET broadening is responsible for the propagation of narrow SETs
  - It contributes to increase the sensitivity to SETs

- **SET broadening is induced by body charging in OFF-state transistors**
  - It is a dynamic effects which depends on the transistor history
  - SET broadening occurs at low frequency (< 100MHz)

- **SET broadening is enhanced**
  - at low supply voltages
  - for designs using small transistors
  - in some "worst-case" branched designs



SET broadening is an issue in highly-scaled complex circuits

Implications for hardness assurance test methodologies and hardened circuit designs

- **SET broadening must be accounted for in SET width measurements**
  - **Presently utilized SET test methodologies must be adapted to characterized the broadening effect**

- **SET broadening must be taken into account in circuit models for hardened circuit design**
  - **Otherwise, techniques such as fault injection are not predictive**
  - Still a lot of work to be done