Flip Chip for microwave applications

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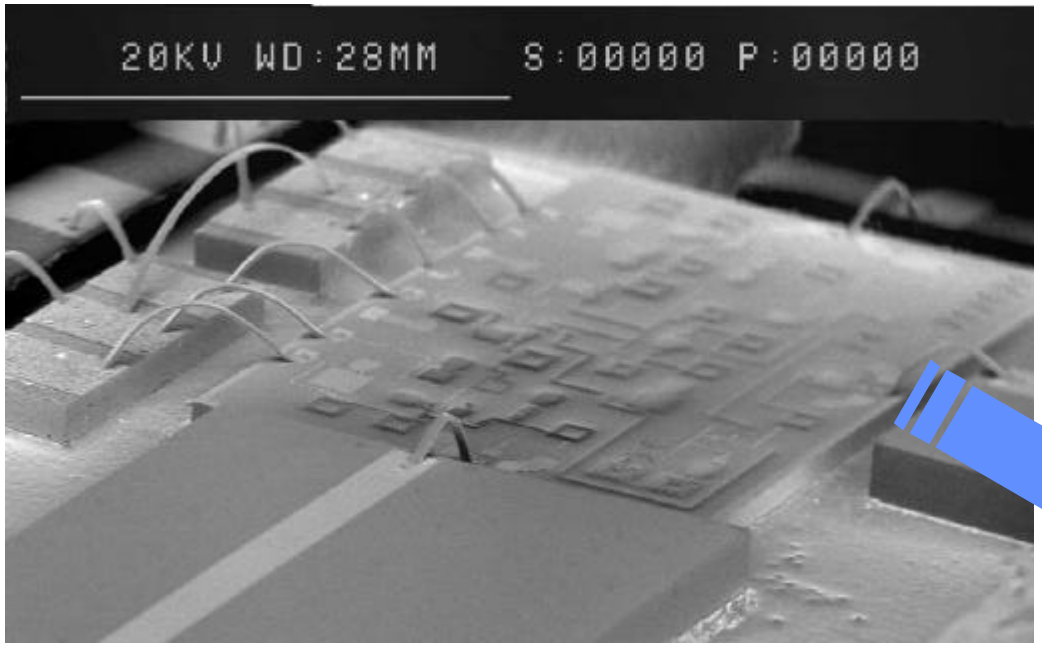
Flip Chip for microwave applications

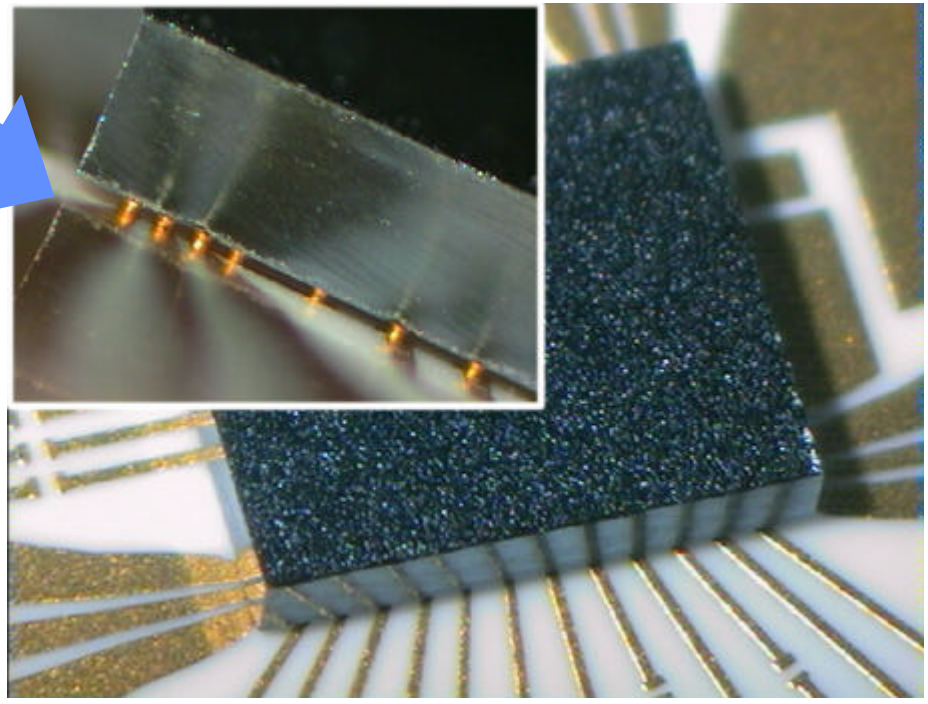
- Flip chip Vs wire bonding
- Which flip chip in microwave modules ?
- Main results and characteristics
  - thermo mechanical
    - daisy chains
    - underfill
  - microwave (HFSS simulations and measurements)
    - flip chip module
    - parasitic mode
- Non Destructive Test

Wire bonding towards flip chip



mechanical interface : glue
electrical interface : glue and wires

Only one mechanical and electrical interface : bumps



Flip Chip or Gluing&Wire bonding ?

- Cons Flip Chip
  - **Electrical**
    - the back of the die must be well connected to ground
  - **Fabrication**
    - "new" process (gluing and wire bonding still present)
    - Control is more difficult and visual inspection is impossible after assembly
- Pros Flip Chip
  - **Electrical**
    - better RF performances
    - perfect for reaching higher frequencies
      - better performances
      - wider frequency bandwidth (less selective)
    - more repetitive results

Alcatel Flip Chip Needs

- When wire bonding assembly is limited
  - for power applications,
    - when heat dissipation through GaAs is not enough,
      - thermal bumps near transistor hot parts
  - For millimetre wave applications
    - when bonding 2 or 3 wires in parallel is not sufficient for good S11,
    - when parasitic effect of wires can not be cancelled any more,
      - need for thin and high bumps
- Quality Insurance
  - Thermal Expansion Coefficient difference between die and substrate can quickly create failure
    - Need for underfill ? Which underfill ?
    - Verification with thermal cycles
  - Non destructive Control ?

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RF application particularities

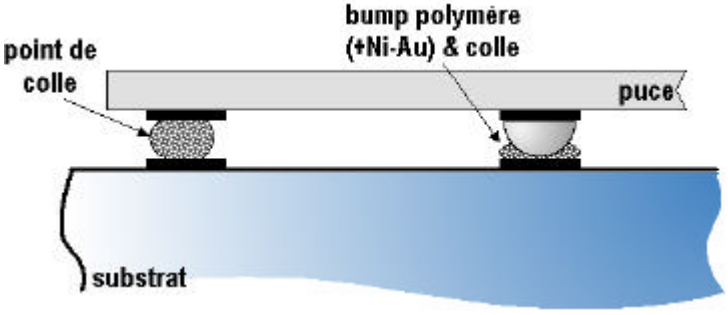
- GaAs components (usually 100 µm thick)
- a few bumps : 10 to 20 per die
- pad dimensions and pitch : 50 to 100 µm - Au top metallization

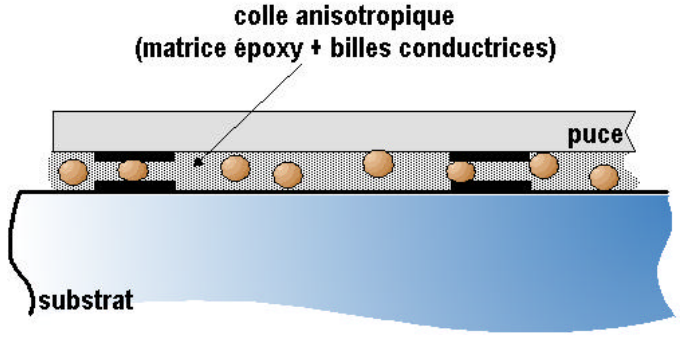
in a flip chip configuration

- Die active face down facing the substrate
  - ➲ package influence on RF performances
    - material electrical characteristics (dielectric constant, losses…)
    - ground plane position, connection, quality and proximity,
    - gap height between die and substrate…
- most of the time : microstrip access on substrate and ground plane just beneath

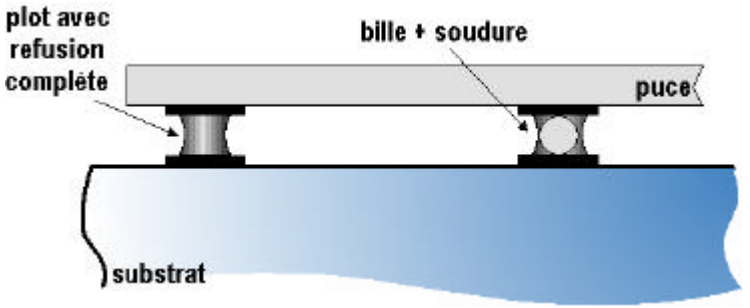
Which Flip Chip for microwave applications ?

Gluing

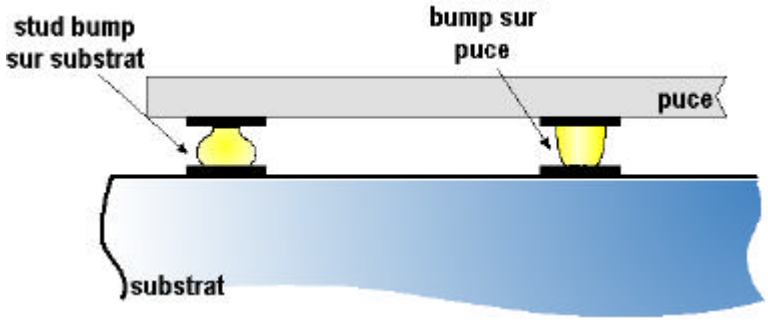




Soldering



Thermo-compression

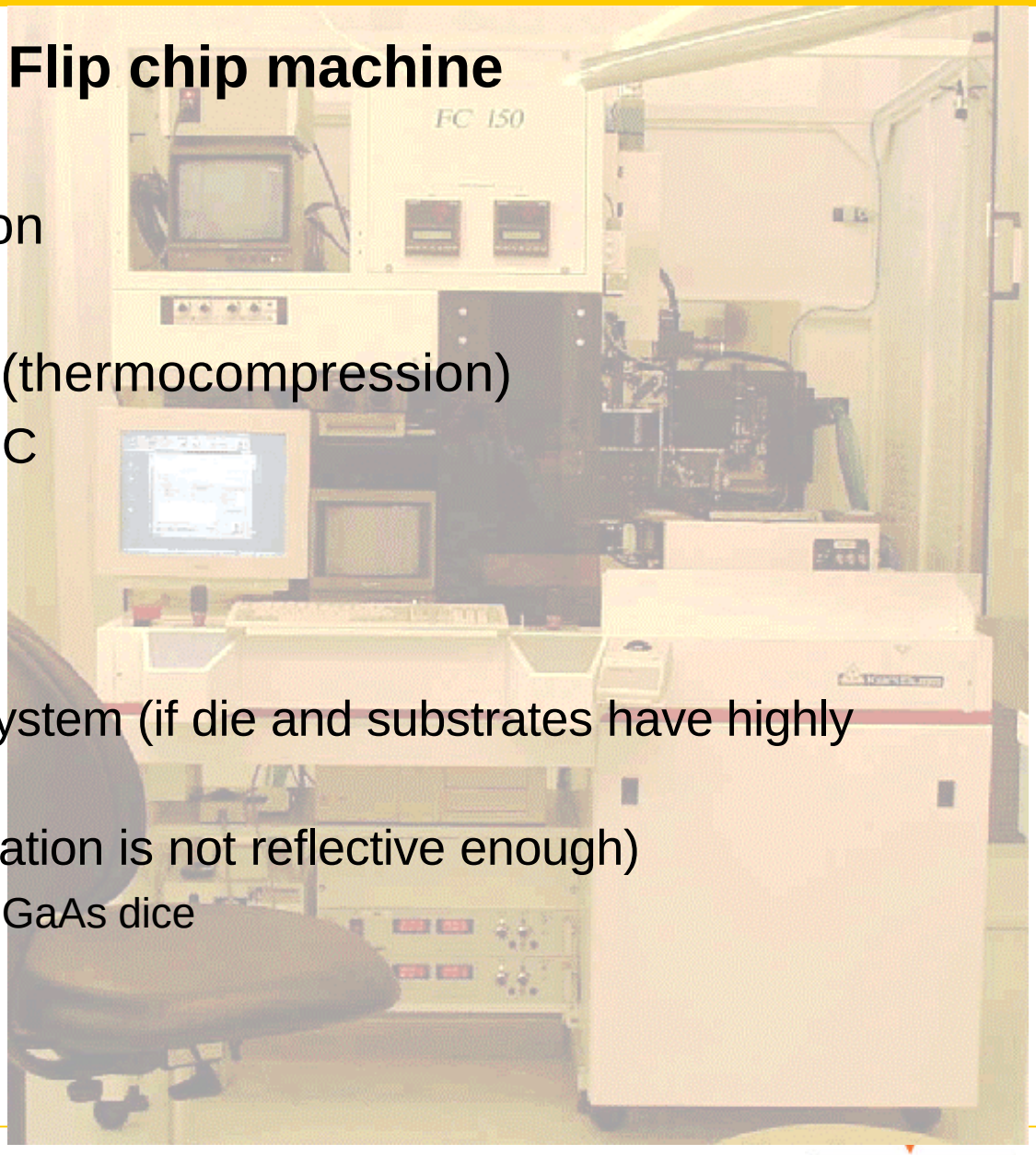


Flip Chip for microwave applications

Which flip chip

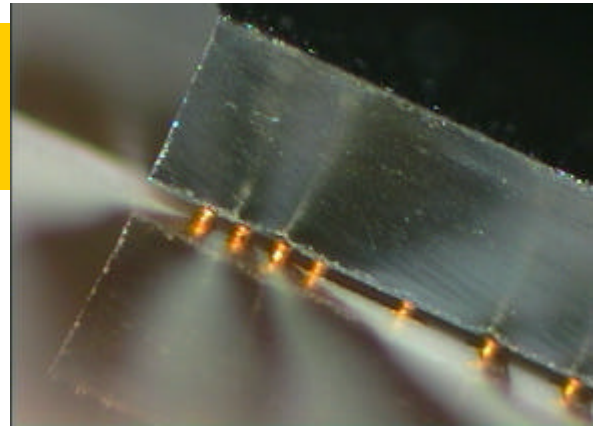
- Alcatel Space hyper frequency dice are GaAs dice with gold pads
  - Soldering ?
    - no SnPb solder directly on die
    - AuSn would be more appropriate
      - quite high temperature process
  - Gluing ?
    - Is one solution when low temperature process is needed (ex : organic parts)
    - still need small pitches and thin and high bumps
      - gold bumps too
      - not compatible with usual gluing techniques
    - Compatible with Silicon and GaAs pads
  - Thermocompression ?
    - Alcatel Space main experience
    - compatible with gold pads and their small dimensions and pitches
    - but high temperature process
      - gold bumps

Suss Microtec Flip chip machine



- Thermocompression or refusion
  - depends on used arm
- 3 µm XY precision at 3 sigma (thermocompression)
  - maximum temperature : 450°C
  - Maximum Load : 50 Kgf
- Parallelism correction :
  - with optical autocollimation system (if die and substrates have highly reflective metallization)
  - with Laser system (if metallization is not reflective enough)
    - most of the time the case with GaAs dice

Flip Chip for microwave applications



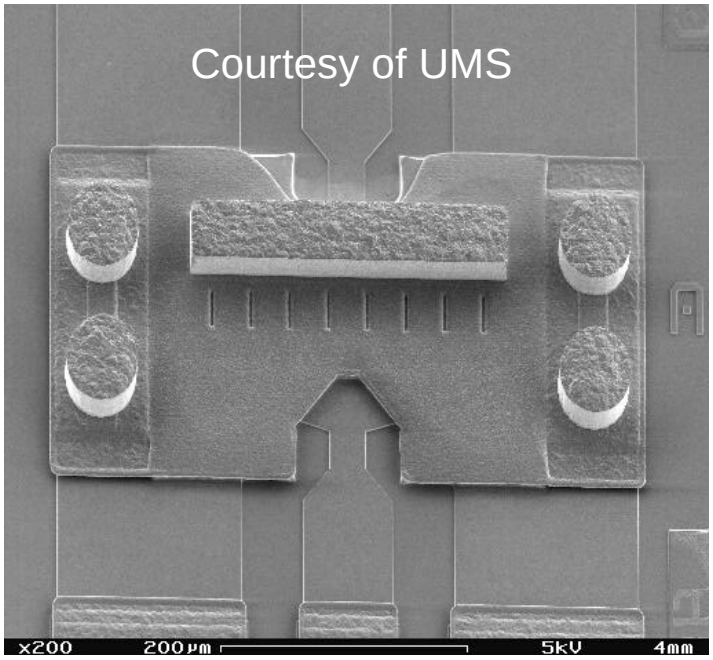
Flip Chip under study at Alcatel Space

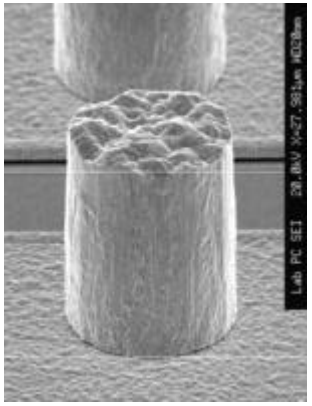
- **Power Flip Chip**
  - Gold thermal bumps made on wafer (by the foundry)
  - High Thermal dissipation substrate (AlN, Diamond…) with thin film and via
- **Low Power Flip Chip**
  - Gold stud bumps (3 possible heights) made by HCM La Rochelle
  - Al_2O_3 substrate with thin film and via
- **Possible "dice"** : MMIC, transistors, MEMS
- **Mostly used technique** : thermocompression

"Power Applications"

Electrolytic Bumps

- Made on the wafer (by the MMIC foundry)
  - perfect for mass production
  - gold electrolytic growth
    - Height ≤ Diameter
  - Excellent for thermal dissipation
    - Thermal bumps on the hottest points of the transistors
  - Critical Points
    - How to perform electrical tests ?
    - No proper evaluation due to bump fabrication default
- Some foundries can make those bumps on GaAs, GaN, SiC wafers



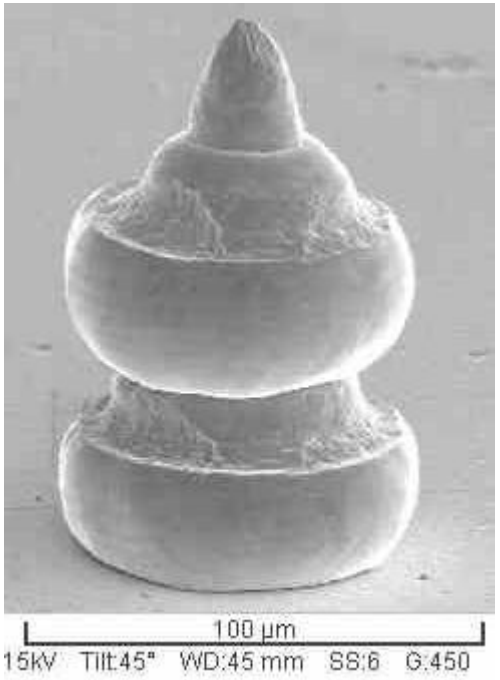


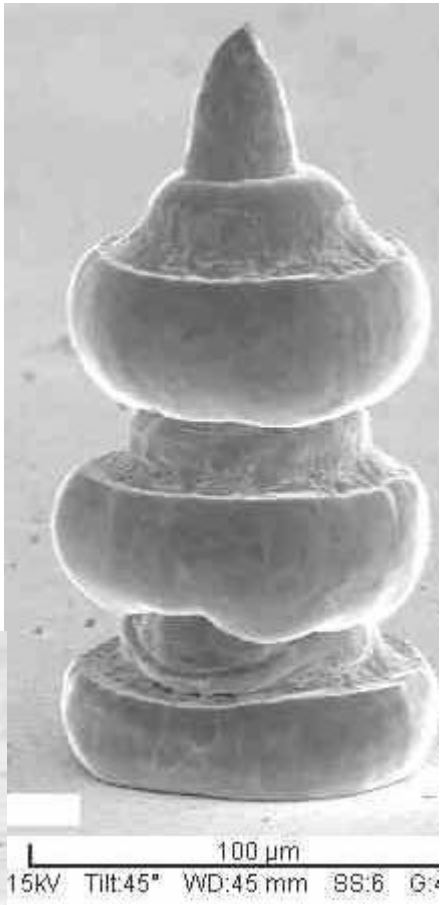
Courtesy of UMS

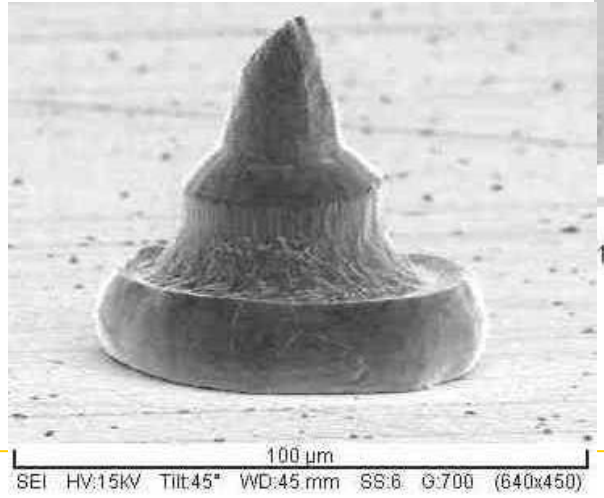
"Standard Applications"

Stud Bumps

- Made on substrate
  - can use MMICs of the shelves
- Adapted to both RF and LF part dimensions
  - 60µm diameter
- Several possible heights
  - 20 to 90µm
- Very good adhesion on AlN and Alumina substrates
  - around 20gf per bump
- Evaluation performed on HCM bumps
  - ESTEC Study (2004)

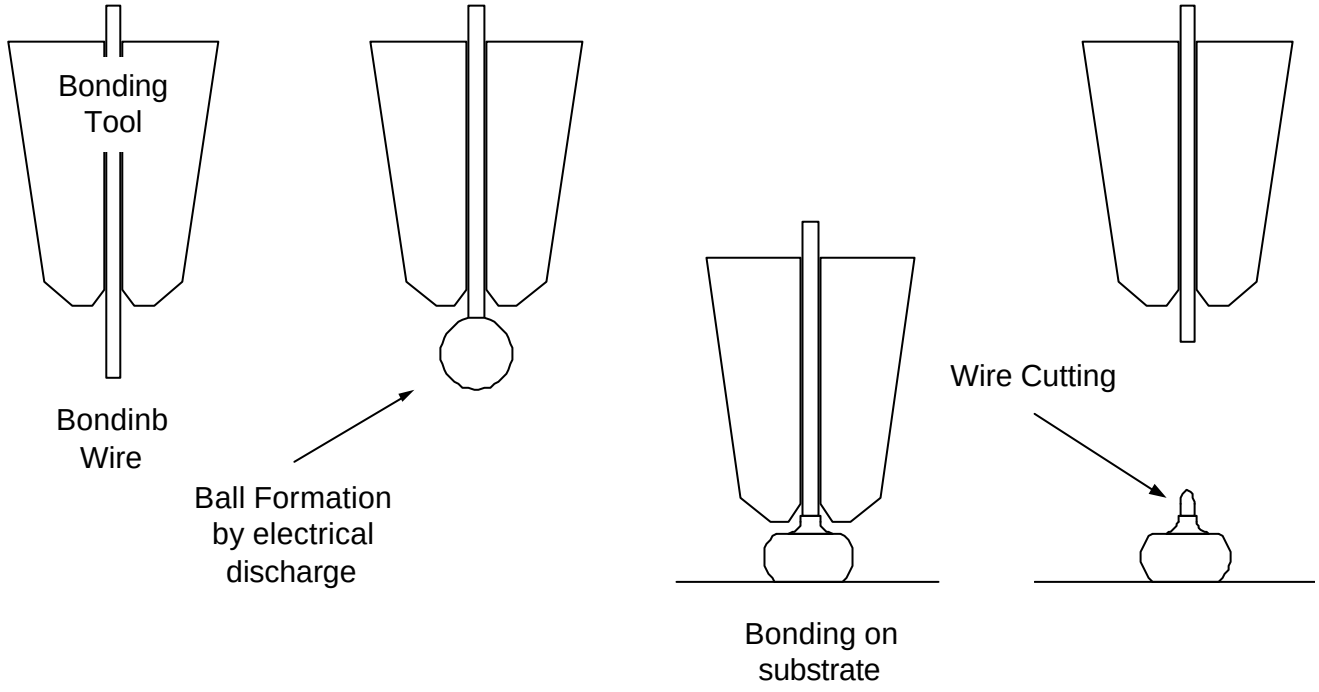






Stud Bump Theory

- Two ways of performing stud bumps
  - 1 - PANASONIC patent
    - gold wire used for wire bonding (same gold)
    - wire cutting by a quick movement of bonding tool - wire torsion
    - stitch against the ball
  - 2 - HCM bumps
    - wire pulling until break
    - dedicated gold wire (1 or 2% palladium for wire breaking)
    - usually 20 µm diameter wires, could be 17.5 µm



HCM Stud Bumps possibilities

- HCM La Rochelle France - Micro electronic Packaging
- Design rules
  - **+/- 3,5 µm** accuracy with K&S8028 machine
  - Minimum pitch between bumps : **55 µm**
  - Minimum pad dimension : **50 µm**
- Gold wire
  - AW6 type gold wire with Pd - **20 µm** diameter
  - can have **18 µm** diameter
- Machine and tools
  - K&S1484 usual machine
  - K&S 8028PPS new machine
  - Many tools can be used but difficult to test them all.

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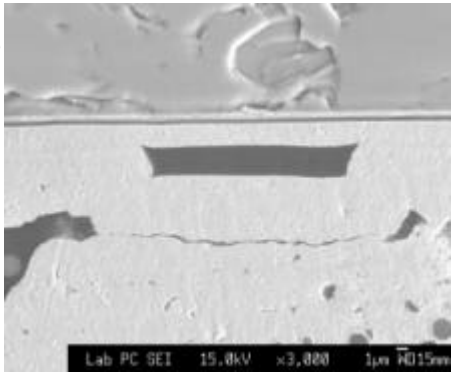
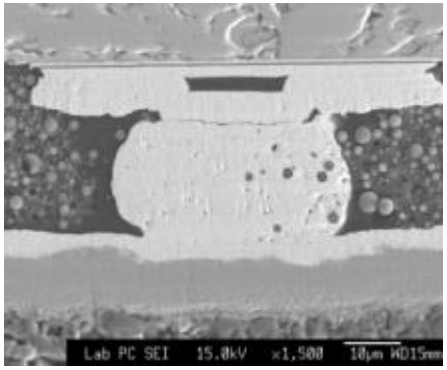
  - thermo mechanical
    - daisy chains
    - underfill
  - microwave (HFSS simulations and measurements)
    - flip chip module
    - parasitic mode
- Non Destructive Test

Process quality and reliability

- When optimising a process, one must check its quality and strength
  - just after assembly : see if all bumps are correctly connecte
  - after ageing tests : see if bumps stay correctly connected…
- Possible defaults
  - Too much strain between die and substrate (due to Coefficient of Thermal Expansion mismatch and big dice)
    - délamination between bump and pad
  - Pollution
    - no bump adhesion on pad
  - Air trapped inside underfill (if there is some)
    - if those bubbles are against bumps, it might concentrate stress on those bumps
- Checking techniques
  - Cut / SEM / EDAX -> long and expensive
  - Daisy Chain and 4-point resistance measurement



Fabrication default o bumps made on the wafer by UMS



Daisy Chain Resistance Measurement

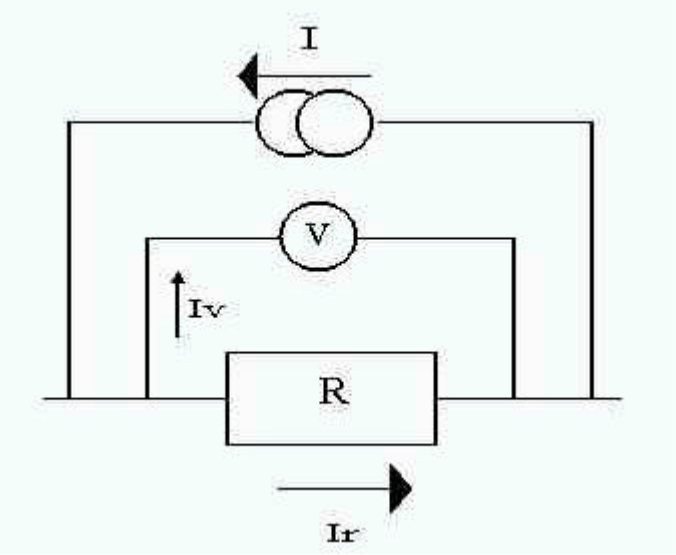
- The best way to control assembly quality and reliability
  - precise and complete information on contacts at initial time & during ageing
  - to see the impact of chosen materials, dimensions…on assembly sturdiness
  - to find the weakest parts of assemblies
- ASP has a dedicated test bench - 4 point resistance measurement
  - easy adaptation to different dice, assemblies...
  - 5% precision on a 1mΩ resistance
    - ➲ very precise measurement of bump evolution
  - automatic measurement of entire daisy chain and small parts of it
    - ➲ some defaults appear and progress very slowly
    - ➲ one bump default could stay a long time unnoticed as bump resistance variation would stay very small compared to the whole chain resistance

- 4 point resistance measurement
  - Theory

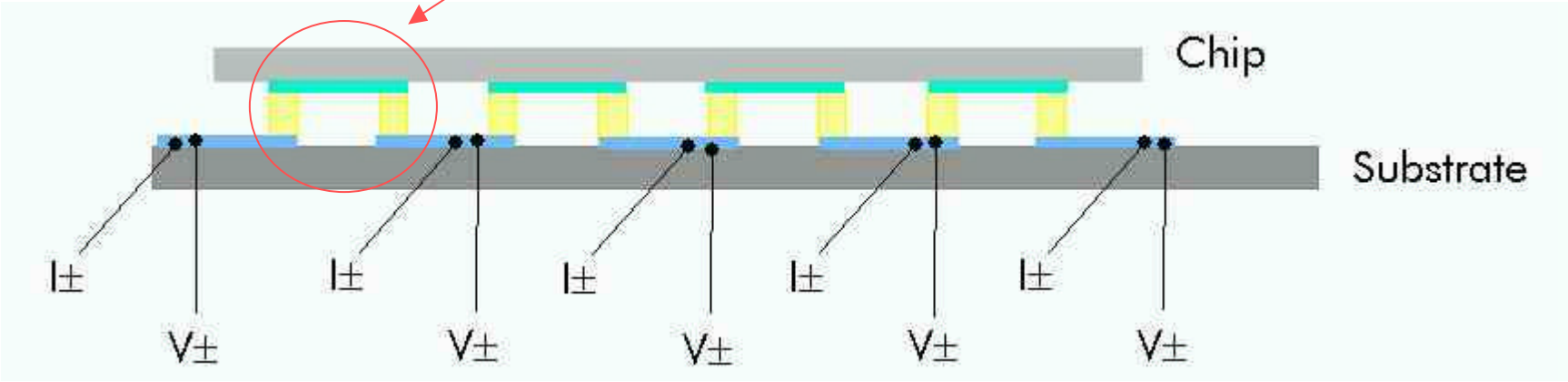
Ir » I

Iv<<Ir

- So measured resistance is nearly exact R
- Wires and lines that bring current or that measure voltage are not taken into account
- and moreover, any ΔR will be more easily noticed

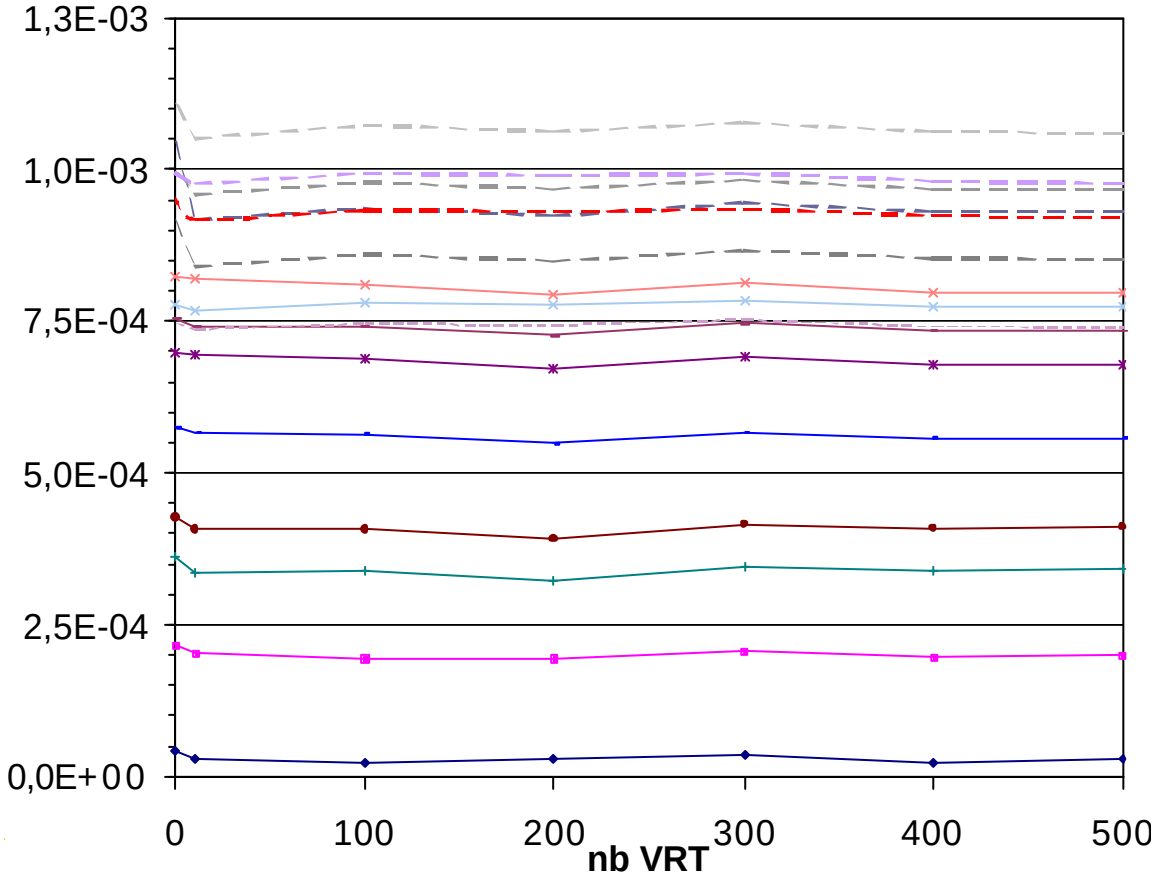


- Bump pairs - ordinary daisy chains
  - bumps are connected with lines alternately on die and substrate
    - the total length of the daisy chain can be measured
      - immediate indication of failure
      - but not always information on default apparition
    - or we can measure groups of "Two bumps and a line on die"
      - Measured resistance is smaller so one bump evolution should be visible
      - location of the default
  - very simple principle and measurement

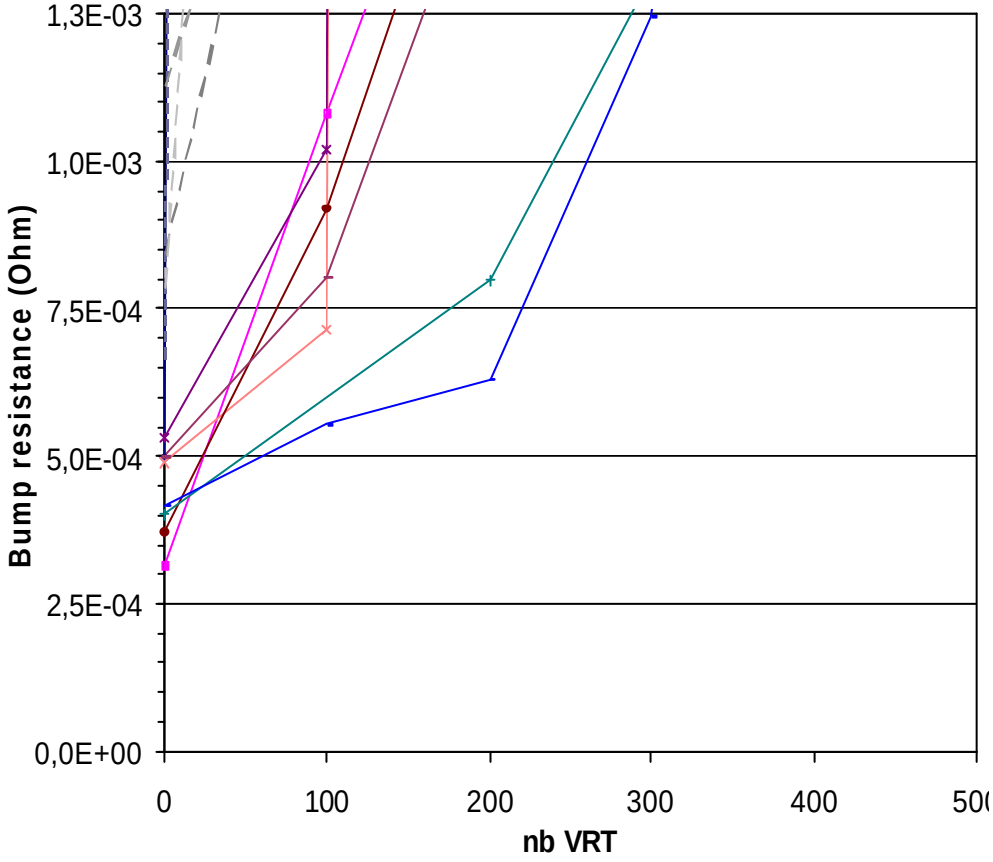


Flip Chip for microwave applications

- Some results with GaAs on alumina and AlN
  - Thermocompression process
  - Thermal cycling
    - On AlN
      - with underfill



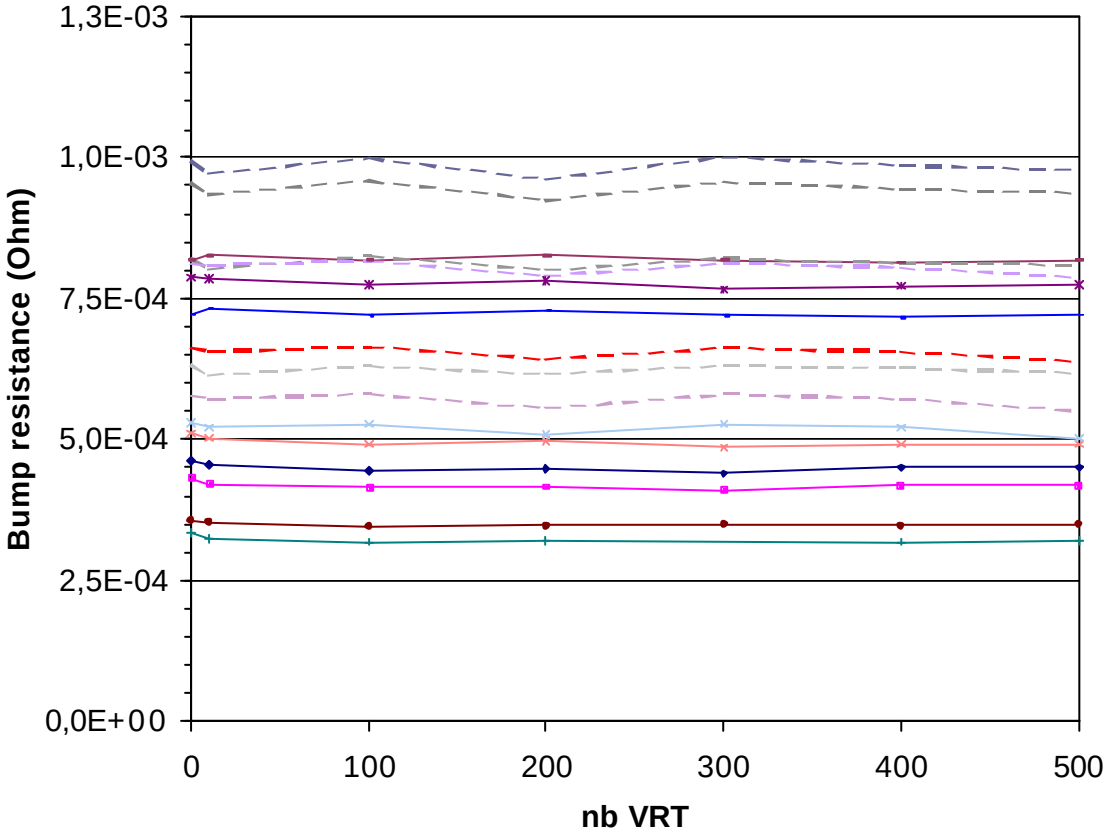
without underfill



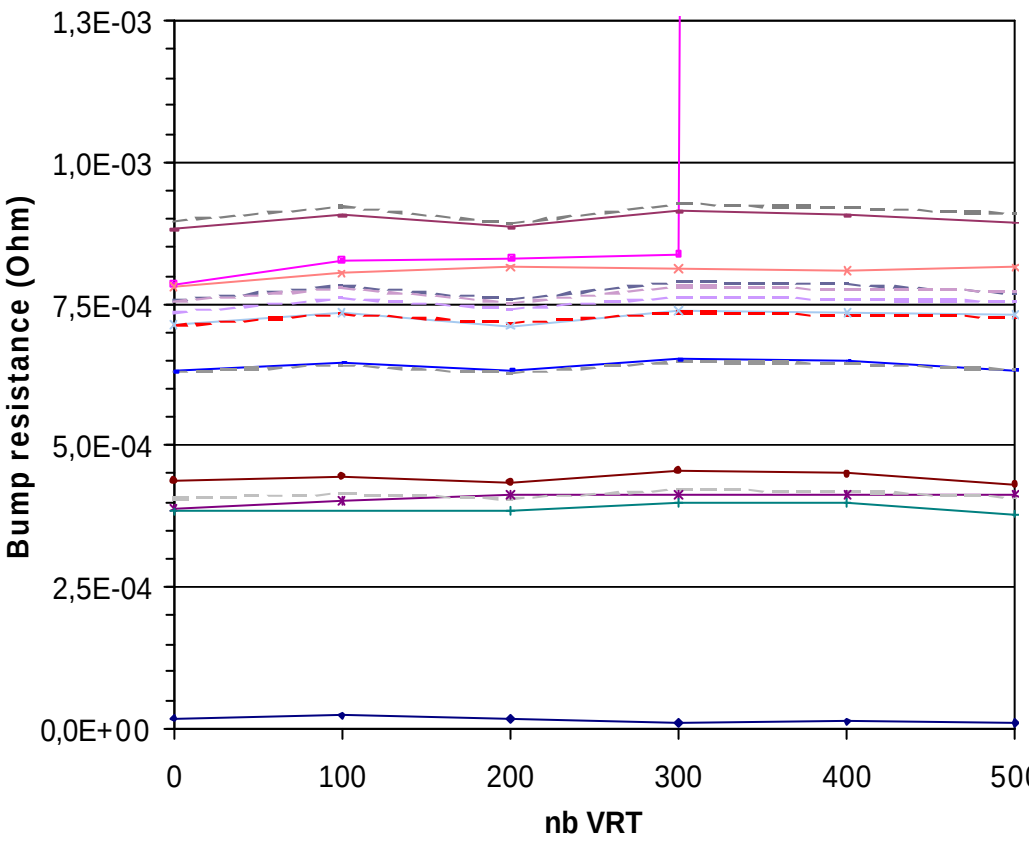
Flip Chip for microwave applications

- Thermal Cycling
  - On Alumina

- with underfill



without underfill



Why Underfill ?

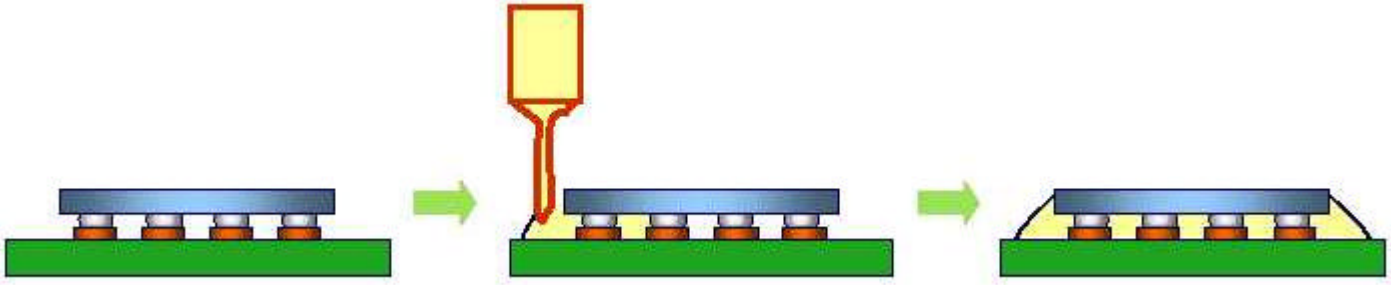
- Coefficient of Thermal Expansion Mismatch between die and substrate
  - high stress concentrated at the bump level

Chip	CTE @ 25°C (ppm/°C)	Substrate	CTE @ 25°C (ppm/°C)
GaAs	5.8	Alumina	5.25
Si	2.6	AlN	2.3

- Solution : Underfill
  - Inserting a curable liquid resin between the die and the substrate
    - Spread the thermally induced stress over the entire package
  - ASP configuration
    - Small bump height : 20 to 50 microns
    - Few bumps, mainly at the die periphery (i.e. high DNP)
    - Die size : from 1x1 to 5x5 mm²

Underfill Solutions

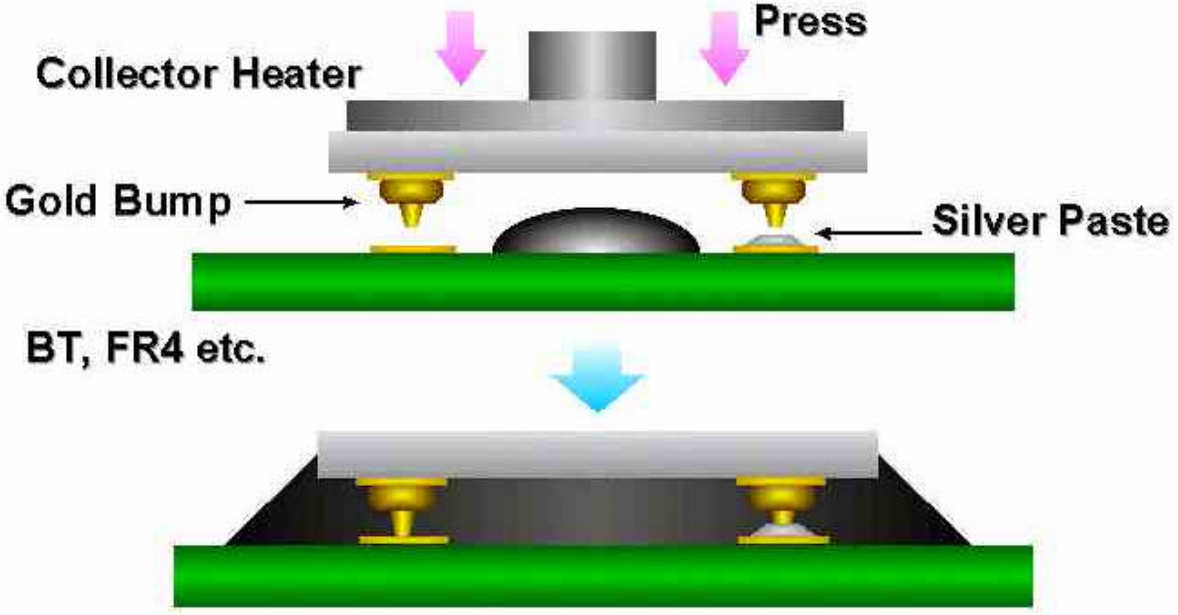
- Capillary underfill
  - underfill dispensed near the edge of the chip
  - flow under the die by capillary action
  - cured when flow completed



  - most common type of commercial underfill
    - limit for high volume : time consumming (flow time + curing time)
    - new solutions under development

Flip Chip for microwave applications

- "No Flow" underfill
  - underfill dispensed on substrate at the die location
  - chip is placed & pressed on the bump
  - flip chip assembly & underfill polymerisation at the same time
    - most of the time dedicated to solder bump
    - unfilled resin, so high CTE : source of fatigue
    - critical dispensing proccess ("floating chip")



- "No Flow" underfill
  - "Press Bump" Underfill
    - No flow for stub bumps
  - products with or without fillers

Underfill ?

Pros : Fabrication et reliability

- Proven effectiveness for die dimensions up to 5x5mm et 5.5x4mm on AlN circuits
  - Thermal cycles [-55;+125°C] : 500-1000 OK
  - Storage at 125°C : 2000h OK
  - Better and stabilise good but imperfect assemblies (// pb for ex).
- Assembly secured
- Less severe control

Cons : Fabrication and electrical

- New organic material (need evaluation and qualification)
- More fabrication steps
- More RF losses
- RF mismatch (frequency bandwidth gets lower)
  - MMIC design taken underfill into account (new library)
  - Or module design taken this frequency shift into account

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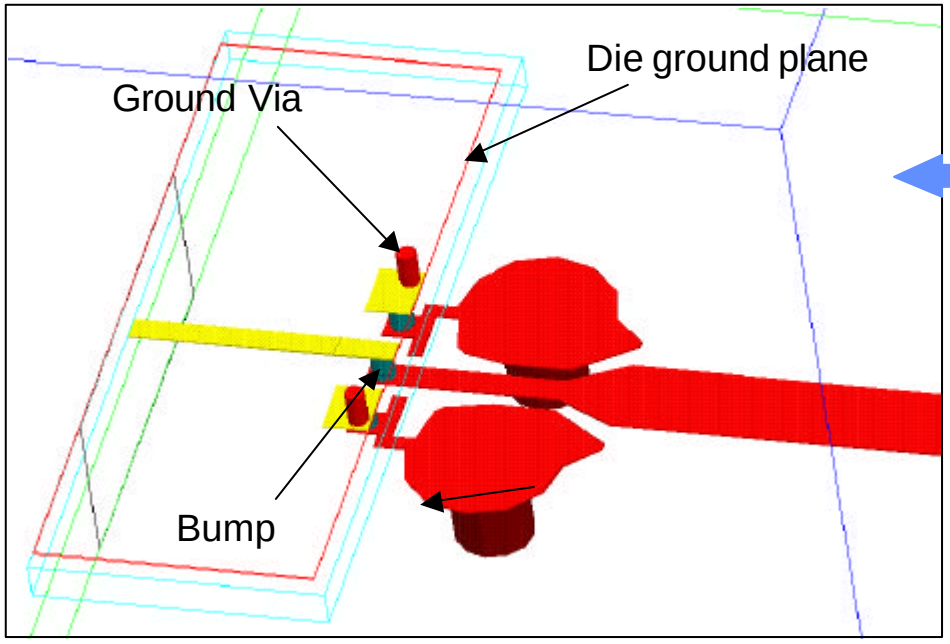
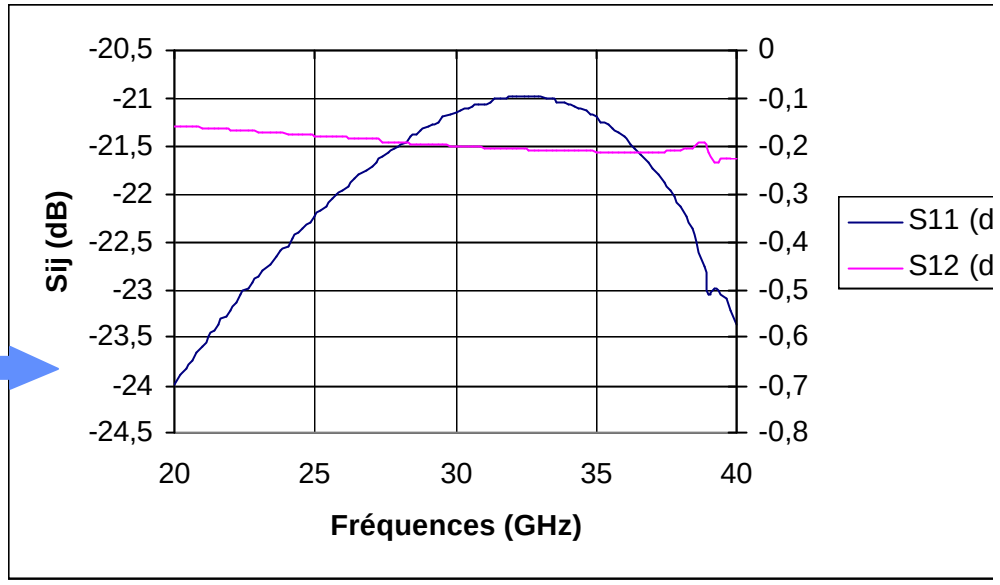
Flip Chip for microwave applications

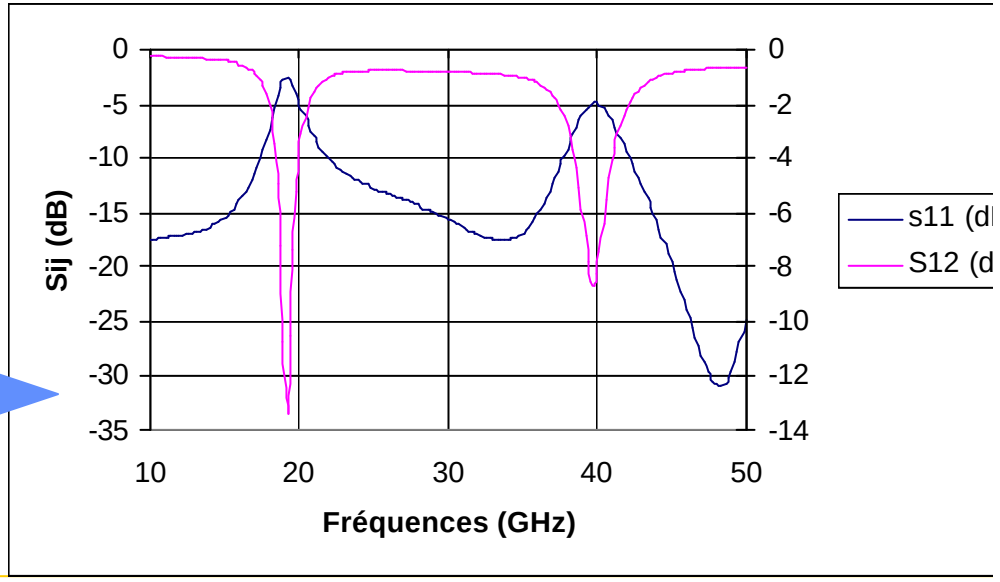
HFSS design

- optimisation of the flip chip transition





- Optimisation of the flip chip module (with 50Ω line instead of MMIC function)
  - ➲ parasitic mode resonance localisation and management

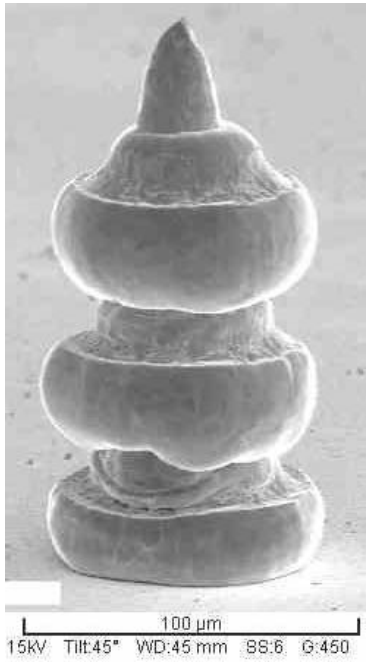


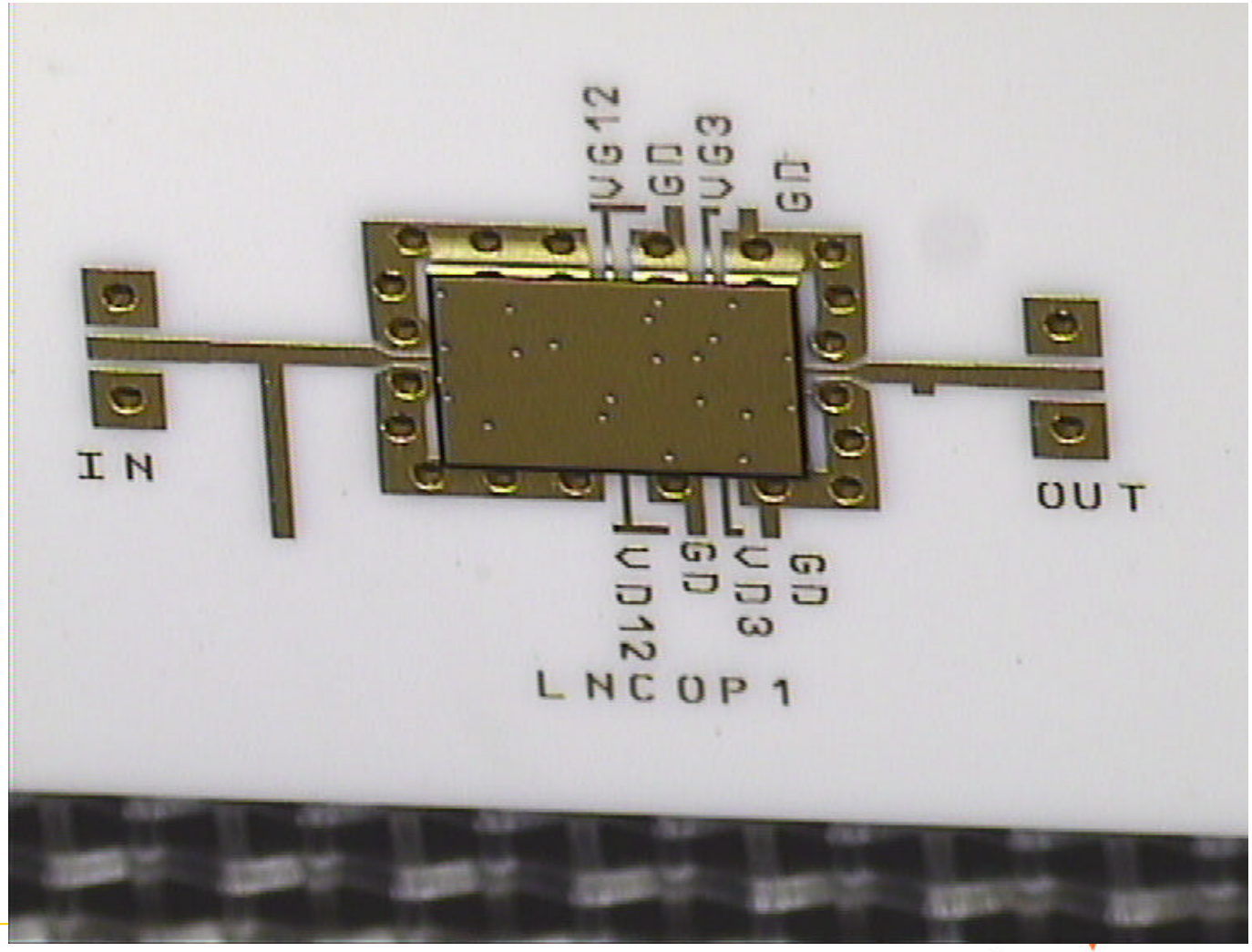
Parasitic mode : type of "Parallel Plate Mode"

- Coupling between MMIC and circuit ground planes
  - happens in main application with the chosen flip chip topology
- Resonance frequency ➢ if :
  - die size ➘
  - bump height ➢
  - ground bump position and number ➢
  - underfill between die and substrate (global εr below the die ➘)
  - circuit thickness ➢
- Solutions
  - HFSS simulations before circuit design -> possible to move this resonance frequency above active bandwidth
  - Take it into account in MMIC design
  - or other flip chip configuration ("Hot Via" or "Embedded transmission-lines (ETL)" topologies)

Flip Chip assembly of a 30GHz LNA

- LNAUM24A flip chip mounted on alumina circuit with HCM triple bumps





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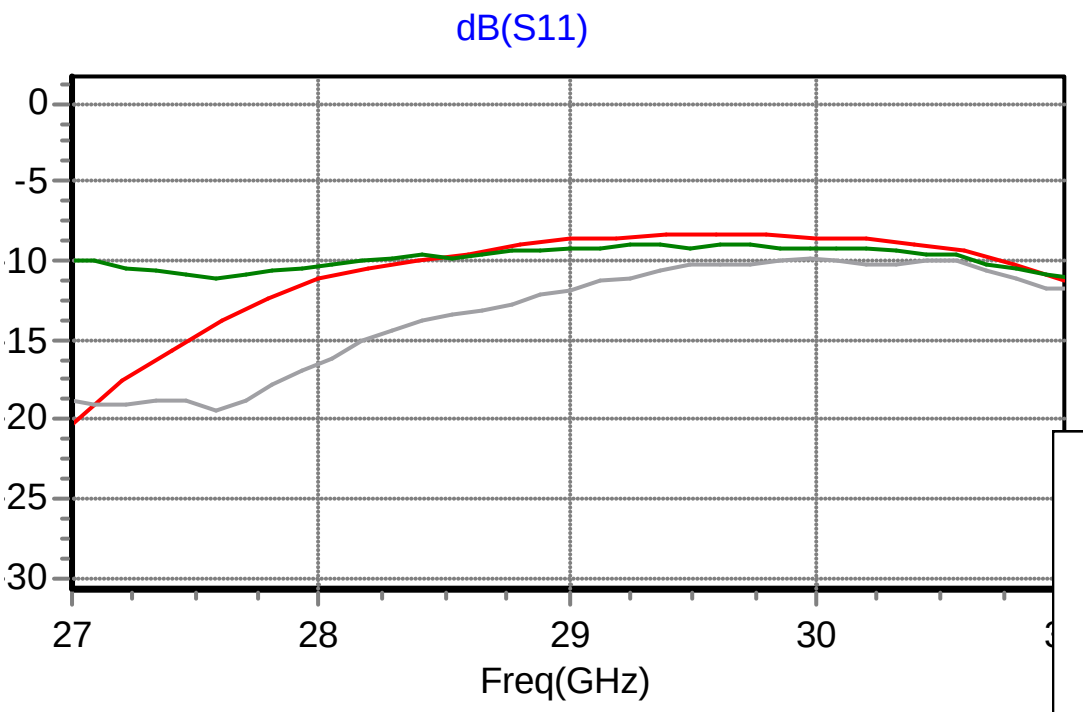
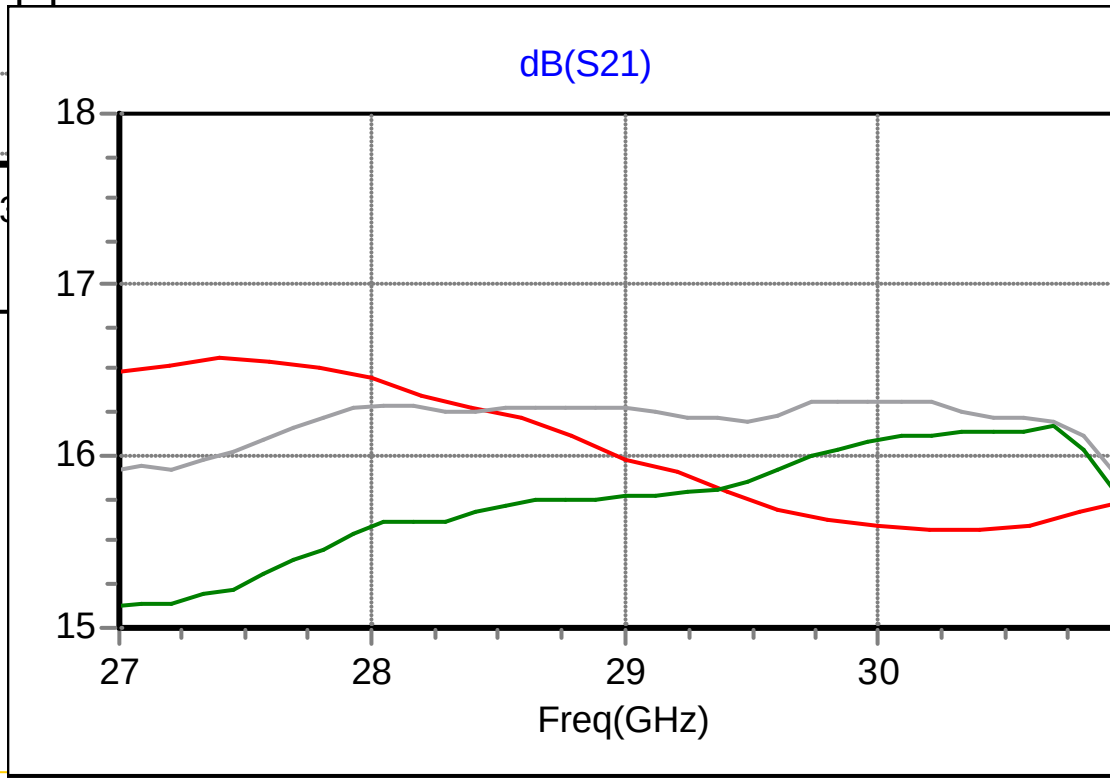


Measurement

Red - bare die
green - module with stub on alumina circuit
grey - module without stub on alumina circui



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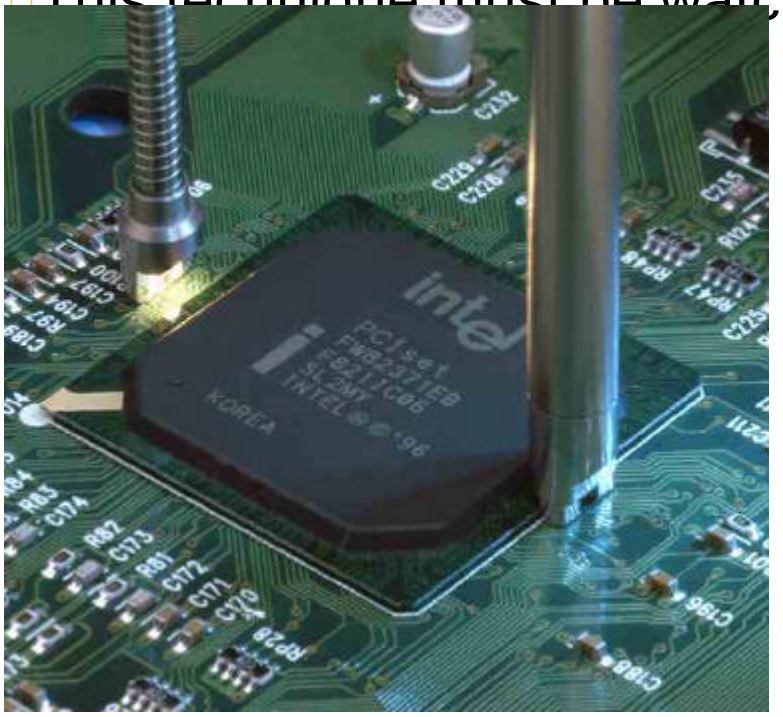
Non Destructive Control

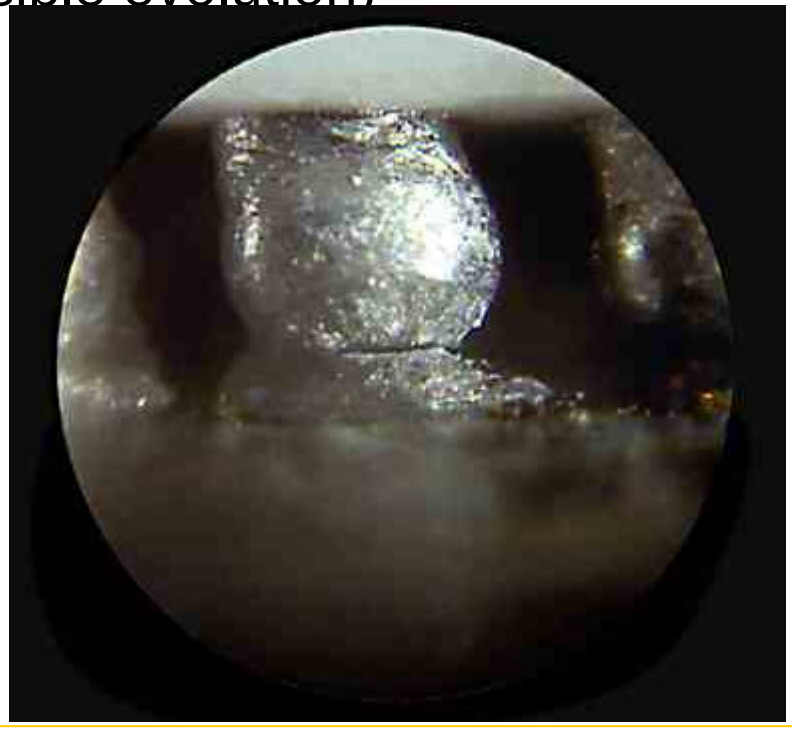
- What makes it to difficult...
  - Bump dimensions -> ~60µm ϕ and height
  - Bump position ->at die periphery
  - Default dimension and nature -> lack of adhesion of delaminations betwee two gold layers
  - Possible complexity of assembly (many metallic or different material layers
  - Possible presence of underfill if CTE mismatch is too big
- Techniques under test
  - X Ray Microscopy - PHOENIX X-RAY / DAGE
  - Infra Red Microscopy - BARNES / QUANTUM FOCUS
  - Visual Inspection (not possible with underfill) - ERSA
  - Stress analysis with ESPI system - HIRONDELLE & ETTEMEYER

Flip Chip for microwave applications

Control ?

- Visual Inspection - Ersascope
  - Very simple and direct technique
  - adapted to BGAs
  - but not enough accurate for bump and associated default dimensions
  - This technique must be watched (possible evolution)

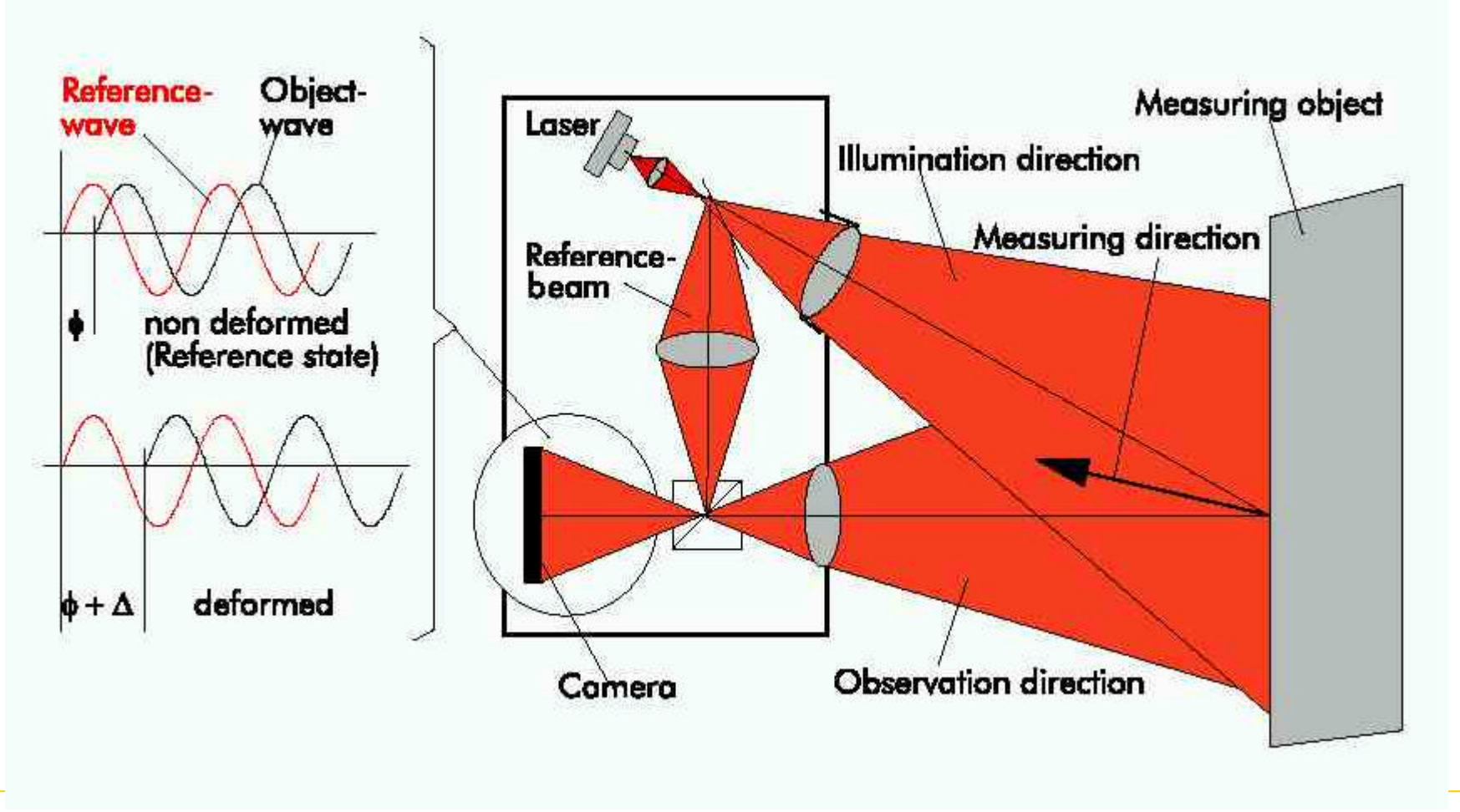




Flip Chip for microwave applications

Control ?

- ESPI technology of ETTEMEYER
  - European study HIRONDELLE (not finished)
  - stress and deformation analysis through interferometry



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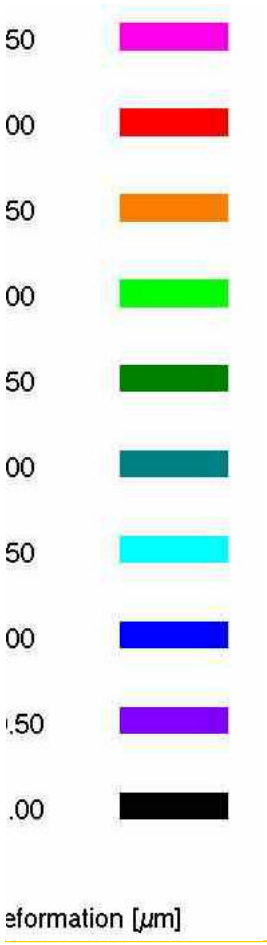
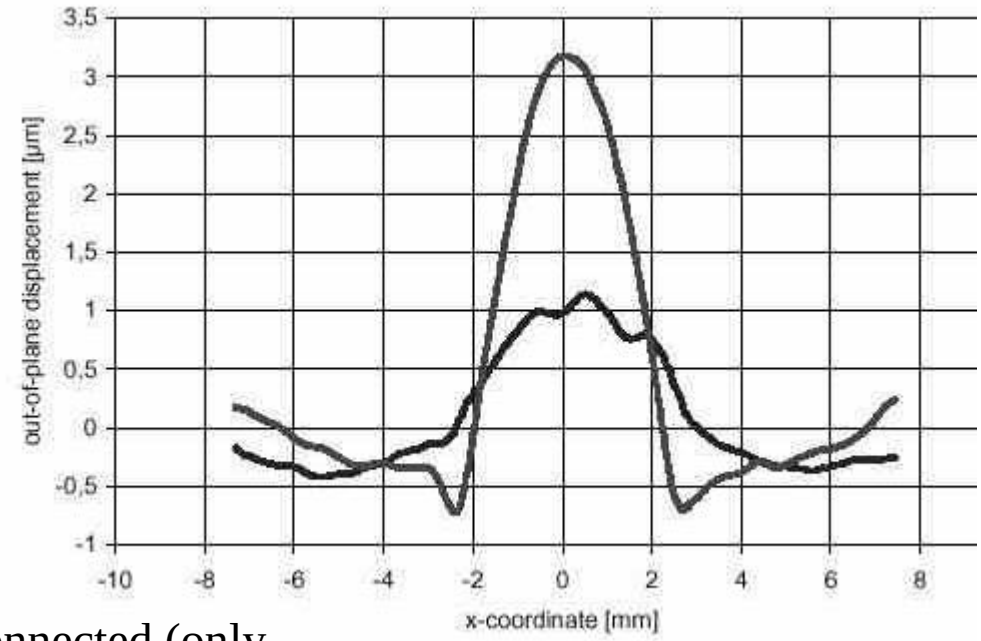
Flip Chip for microwave applications

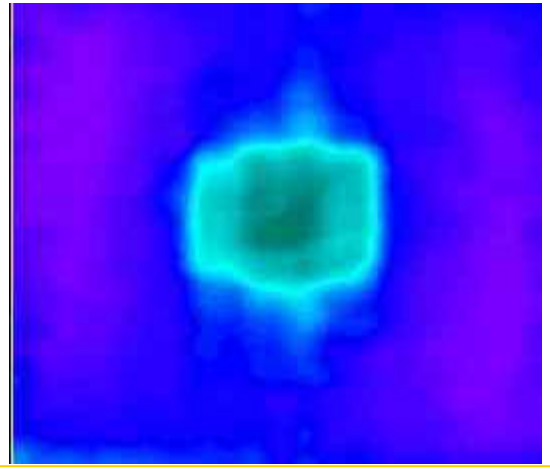
Control ?

- 3D-ESPI out of plane displacement measured between 25°C and 125°C on flip chip assembly of GaAs die on AlN substrate
  - ➲ further trials with less and smaller defaults
  - ➲ other ones with MMICs

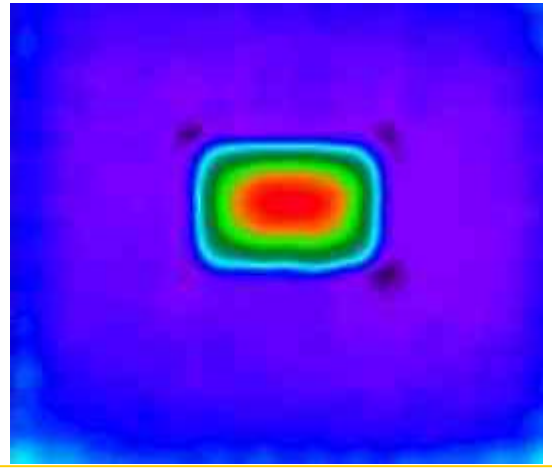


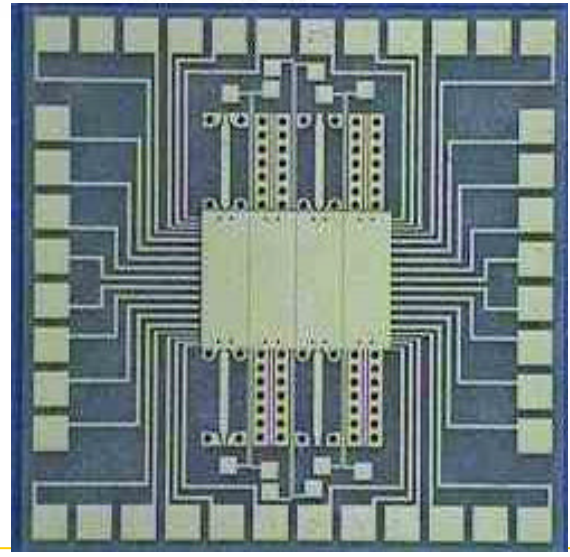


All bumps connected



Half of bumps connected (only peripheral)



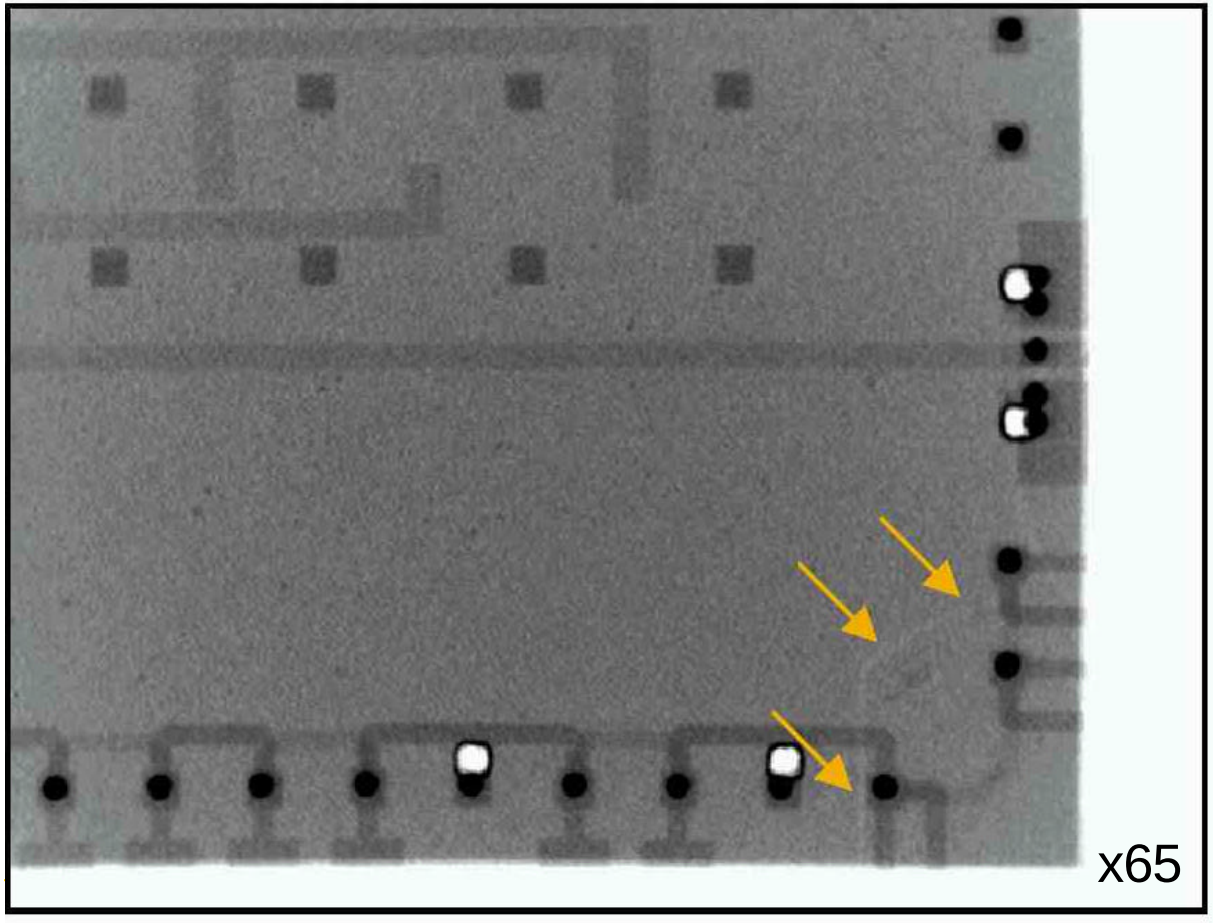


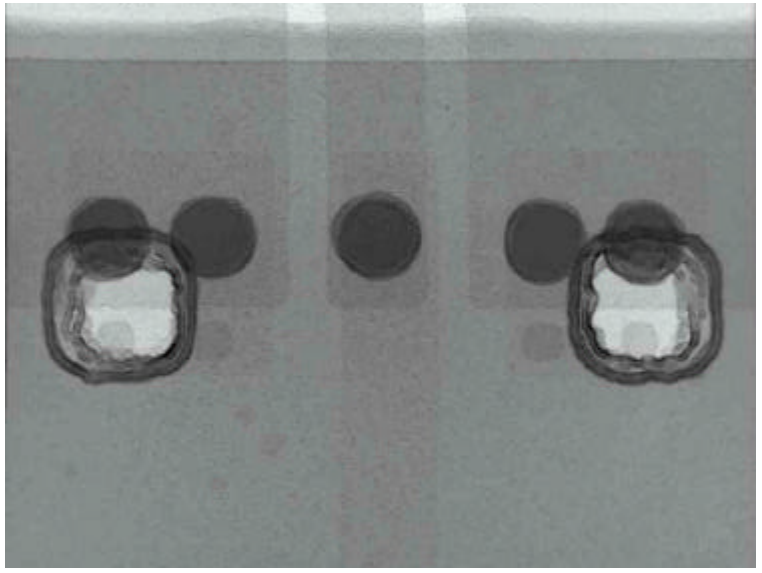
ALCATEL SPACE

Flip Chip for microwave applications

Control ?

- X- ray microscopy (PHOENIX)
  - nanofocus tube -> 0.3µm lateral resolution
  - but defaults <1µm detection mainly depends on used detector contrast
  - could not see any default on bumps



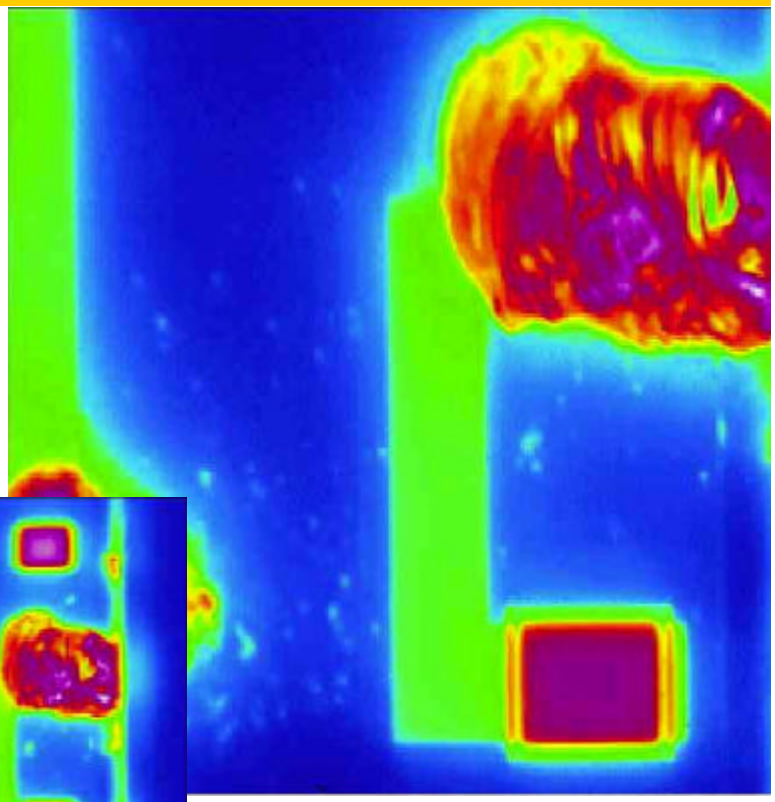


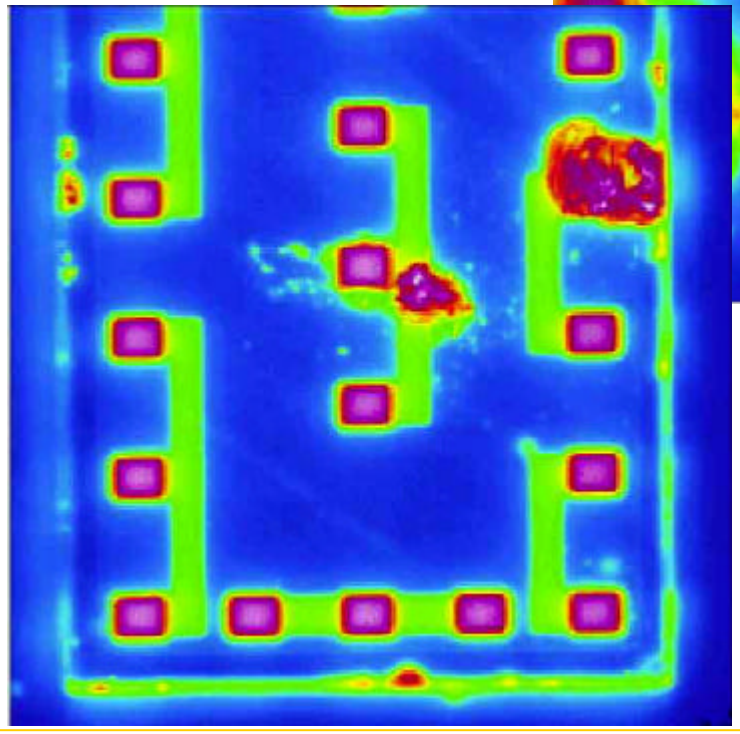
x360

Flip Chip for microwave applications

Control ?

- Infra Red Microscopy (QUANTUM FOCUS)
  - Much more precise than a few years ago
  - good resolution
  - but bumps hidden by metallisations
  - some further possible tests :
    - Temperature pulse
    - Faster acquisition





Proposed Solution - Sampling

- Widely used elsewhere but could it be applied to Space equipment fabrication ?
  - application domains :
    - when control is destructive
    - when control takes too long
    - when control is too expensive
  - Goal
    - decide whether or not the lot is acceptable
    - not for quality estimation
  - between 100% and 0% control
    - but with a good knowledge of error probability
    - several kinds of Acceptance Sampling Plans

Flip Chip for microwave applications

Control ?

- Conditions
  - process must already be qualified
  - measurement precision must be known -> error due to :
    - different kind of samples (part to part variation),
    - operator (reproducibility)
    - and error inherent in measurement tool (repeatability)
- Which acceptance or rejection criteria ?
    - Can some defaults be accepted ? (depending on default nature or position)
    - look for norms depending on chosen control test.
- Which control for flip chip inspection ?
  - Cuts and SEM inspection (most precise)
  - Shear tests (easiest)
  - Pull tests (maybe better results than shear tests but much more difficult to implement)