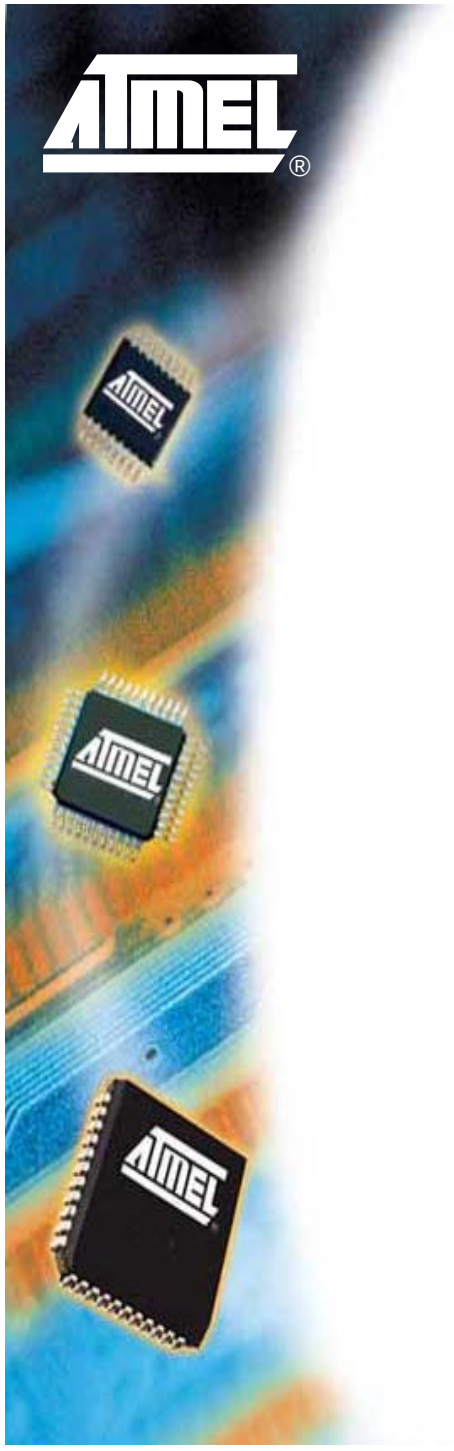

State of the Art of HiTCE Ceramic Packages

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ESTEC – NOORDWIJK – April 27th 2005

STATE OF THE ART OF HITCE CERAMIC PACKAGES

SOME DEFINITIONS FIRST

- ✓ TCE: Thermal Coefficient of Expansion
- ✓ Reliability level 1
- ✓ Reliability level 2
- ✓ HiTCE

TCE VALUES OF EXISTING PACKAGES

- ✓ Flip-Chip CERAMIC, PLASTIC and COLUMNS BGA packages
- ✓ Level 1 & Level 2 Reliability
- ✓ TCE of involved materials

SECOND LEVEL RELIABILITY IMPROVEMENT SOLUTIONS

- ✓ History
- ✓ HiTCE

HITCE CERAMIC TECHNOLOGY – MILITARY APPLICATIONS

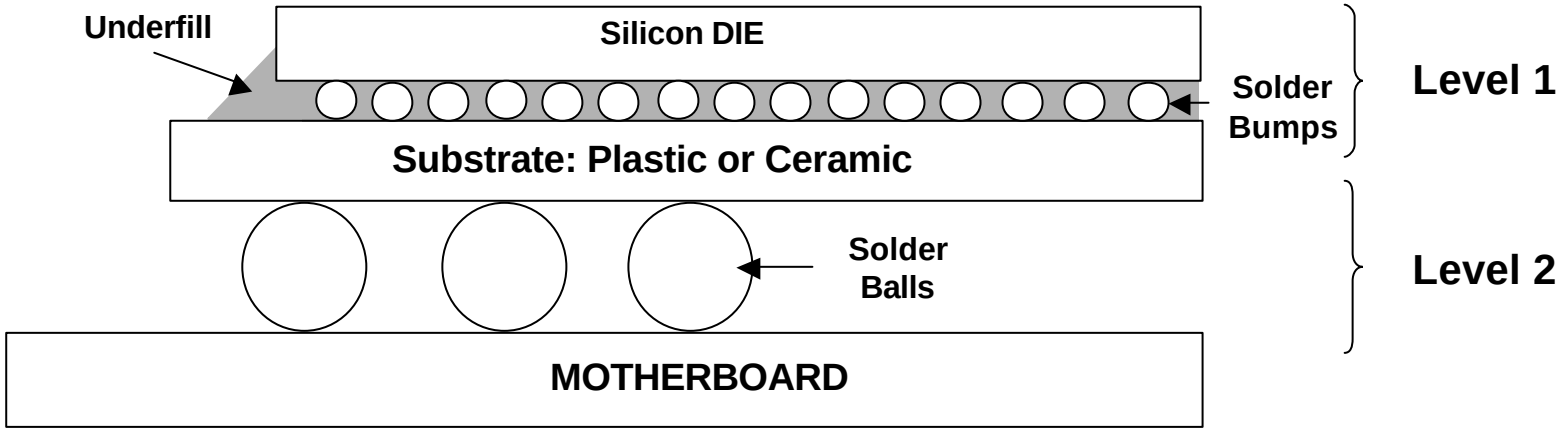
- ✓ Features
- ✓ Electrical performances
- ✓ Thermal performances
- ✓ Hermeticity – Underfill – 1st Level Reliability
- ✓ 2nd Level Reliability
- ✓ Lead-Free solution

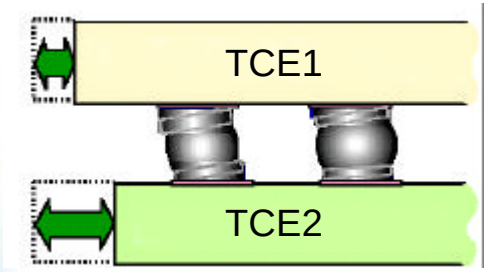
SUMMARY & CONCLUSION

ESTEC – NOORDWIJK – April 27th 2005

SOME DEFINITIONS FIRST

- ➔ TCE: Thermal Coefficient of Expansion
- ➔ Reliability level 1
- ➔ Reliability level 2
- ➔ HiTCE





TCE MISMATCH (TCE: Thermal Coefficient of Expansion)

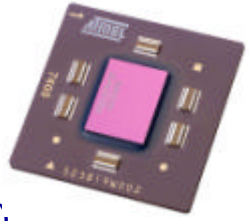
- ✓ Shear Stress on solder joint (mechanical stress)
- ✓ Crack form and propagate until breaking
- ✓ Affect the interface reliability

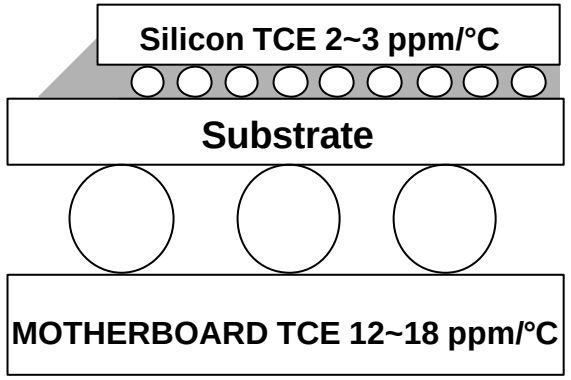
TCE VALUES OF EXISTING PACKAGES

- ➔ Flip-Chip CERAMIC, PLASTIC and COLUMNS BGA package
- ➔ Level 1 & Level 2 Reliability
- ➔ TCE of involved materials

CBGA Package

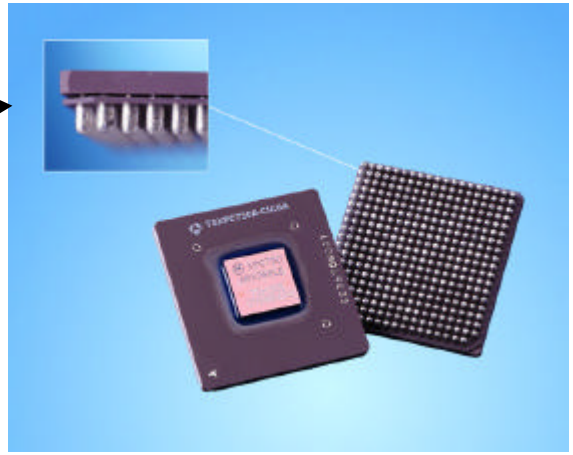
- ✓ Al2O3 ceramic
- ✓ TCE ~ 7ppm/°C
- ✓ 90/10 Pb/Sn solder ball (High Lead)





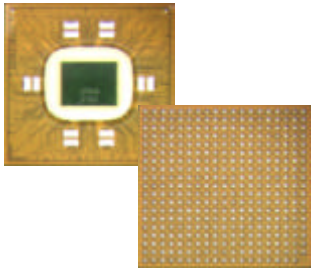
CI-CGA Package

- ✓ Al2O3 ceramic
- ✓ TCE ~ 7ppm/°C
- ✓ Solder Column Interposer (SCI)
- ✓ 90/10 Pb/Sn solder ball (High Lead)



PBGA Package

- ✓ Organic substrate (Plastic)
- ✓ TCE - 12~14 ppm/°C
- ✓ 63/37 Sn/PB solder ball (Eutectic)



SECOND LEVEL RELIABILITY IMPROVEMENT SOLUTIONS

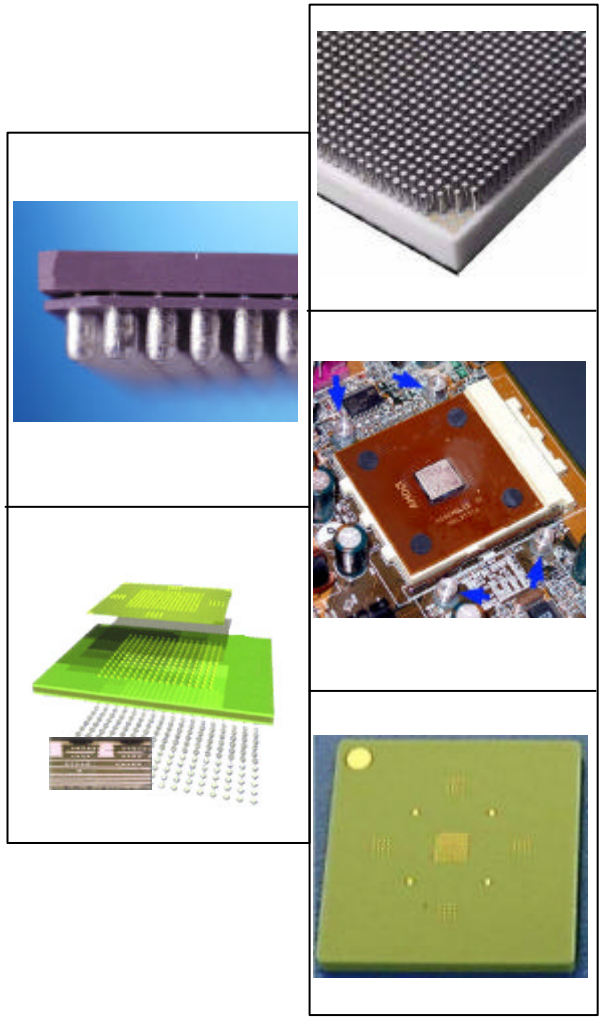
➔ HISTORY

Interconnection level

- **Ceramic Column Grid Array (by IBM)**
- **Solder Column Interposer (by NTK)**
- **Socket Mounting**
- **Build-up Organic Substrates**

Material level

- **HITCE Ceramic material (by KYOCERA)**

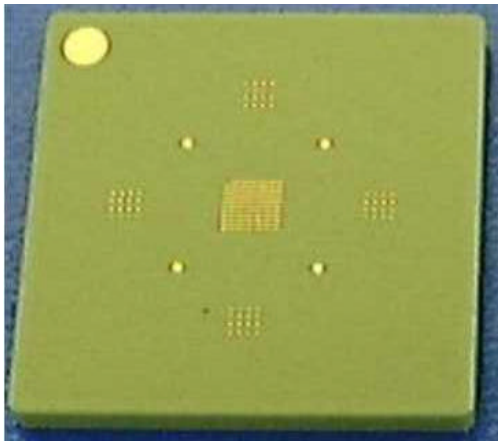


SECOND LEVEL RELIABILITY IMPROVEMENT SOLUTIONS

➔ HiTCE

Technology

- ✓ Ceramic technology patented by Kyocera
- ✓ Low Temperature Co-fired Ceramic (LTCC)
- ✓ Started in 1998
- ✓ 3 years of improvement
- ✓ 2002: Robust Manufacturing
- ✓ Production: 1Mpcs / Month (Kokubu)



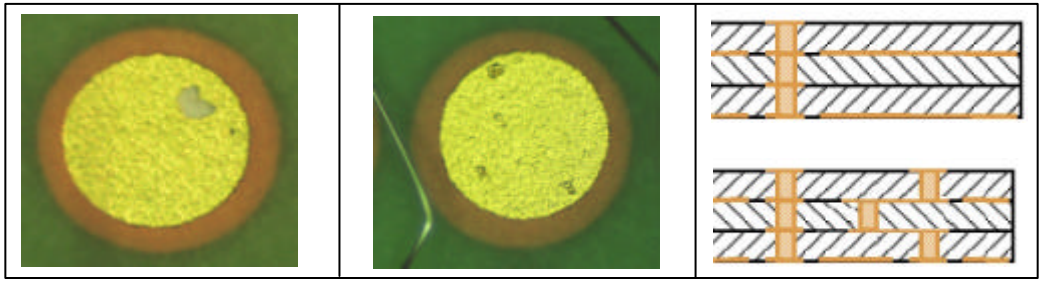
ROBUST
MANUFACTURING

Features

- ✓ Higher CTE than regular Al2O3 ceramic
- ✓ Low Resistance (Cu traces) and low dielectric constant
- ✓ Same body size & footprint as CBGA 's
- ✓ Same board assembly process as CBGA's

Improvements

- ✓ Voids
- ✓ Protrusion
- ✓ Porosity



Voids Protrusion Porosity

Situation Cleared Up Since End of 2001

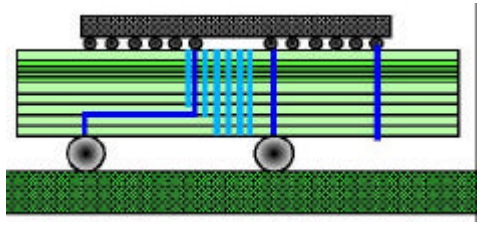
HITCE CERAMIC TECHNOLOGY – MILITARY APPLICATIONS

➔ Electrical Performances

		CERAMIC		ORGANIC
ELECTRICAL	Unit	AL2O3	HiTCE	FR4
Dielectric Constant (1MHz / 10GHz)	-	9.8	5.2~5.3	5.5
Sheet Resistance	mOhm/SQ	8~10 (W)	3 (Cu)	1 (Cu)

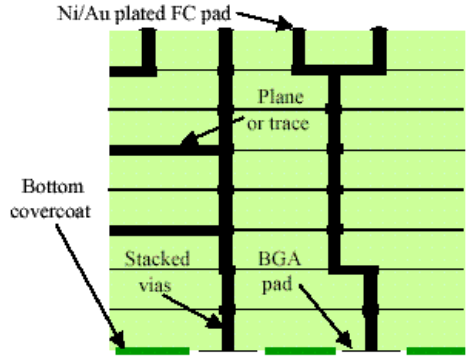
Technology

- ✓ LTCC: Low Temperature Cofired Ceramics
- ✓ Low Dielectric Constant
- ✓ Copper conductor ➔ Low resistance metallization
- ✓ Design flexibility equivalent to that of Alumina
- ✓ High Density Routing



Example

- ✓ A 5mm trace of typical width would have a series resistance of 150mΩ in Hi-TCE instead of 400mΩ in CBGA
- ✓ A decrease in propagation delay by about 25% on HITCE and 30% on PBGA compared to CBGA

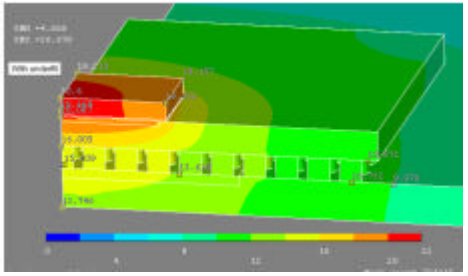


HITCE CERAMIC TECHNOLOGY – MILITARY APPLICATIONS

➔ Thermal Performances

		CERAMIC		ORGANIC
THERMAL	Unit	AL2O3	HiTCE	FR4
Coefficient of Linear Thermal Expansion	ppm/°C	7.0	10~12	12~18
Thermal Conductivity	W/m.k	18	2	0.2

Thermal Resistance Simulation Results	Al2O3	HiTCE
Thermal Resistance junction to bottom of ball	3,4 °C/Watt	6,8°C/Watt
Thermal Resistance junction ambiant, Jedec JESD51-2(2S2P board)	17,2°C/Watt	20,7°C/Watt



Thermal performance Measurements

- ✓ The performance of Hi-TCE is close to that of ceramic despite the large difference in substrate conductivity

Thermal Resitance Measurement	Al2O3	HiTCE
Thermal Resistance junction ambiant, Jedec JESD51-2(2S2P board)	18°C/Watt	19,8°C/Watt
Thermal Resistance junction ambiant @1m/s, Jedec JESD51-2(2S2P board)	14,2°C/Watt	15,7°C/Watt

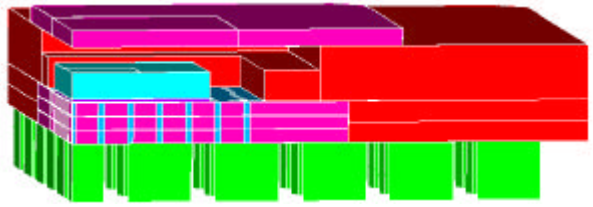
HITCE CERAMIC TECHNOLOGY – MILITARY APPLICATIONS

➔ Thermal Performances

		CERAMIC		ORGANIC
THERMAL	Unit	AL2O3	HiTCE	FR4
Coefficient of Linear Thermal Expansion	ppm/°C	7.0	10~12	12~18
Thermal Conductivity	W/m.k	18	2	0.2

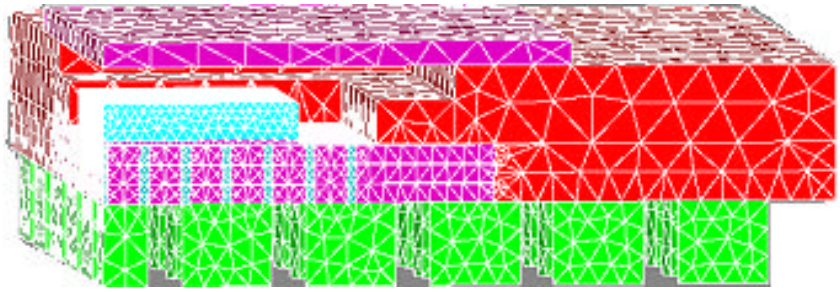
Technology

- ✓ Tungsten Thermal Conductivity: 90 W/m.k
- ✓ Copper Thermal Conductivity: 260 W/m.k



Thermal simulations

- ✓ ANSYS 6.0
- ✓ Thermal dissipation improvement
- ✓ Thermal vias
- ✓ Via density
- ✓ Via diameter / Via pitch



Thermal performance measurements

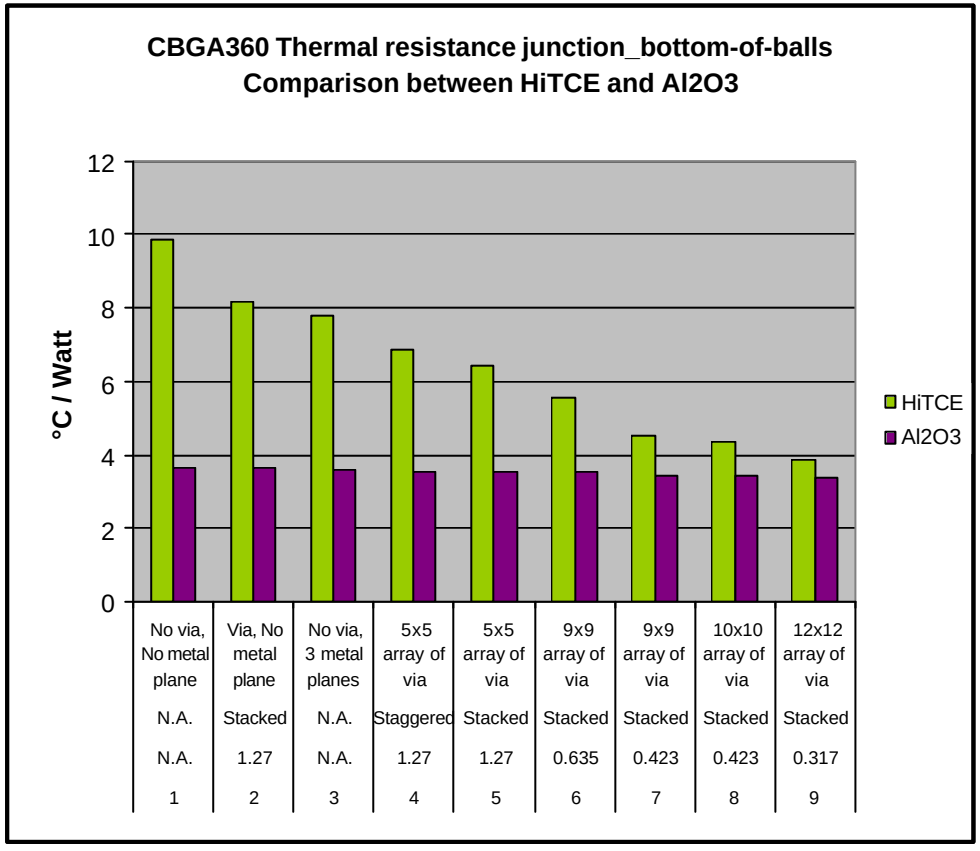
- ✓ The performance of Hi-TCE is close to that of ceramic despite the large difference in substrate conductivity

HITCE CERAMIC TECHNOLOGY – MILITARY APPLICATIONS

➔ Thermal Performances

Technology

✓ Kyocera Design Rules



	RTHj_bottom of balls	
	Al2O3	HiTCE
Case n°	°C/Watt	°C/Watt
1	3.631	9.869
2	3.610	8.145
3	3.561	7.795
4	3.545	6.892
5	3.543	6.433
6	3.514	5.563
7	3.462	4.517
8	3.454	4.339
9	3.382	3.848

Feasibility Certified by

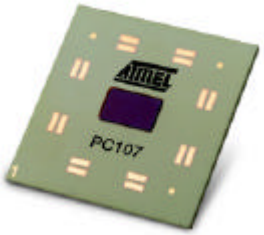
Kyocera Design & Manufacturing Teams

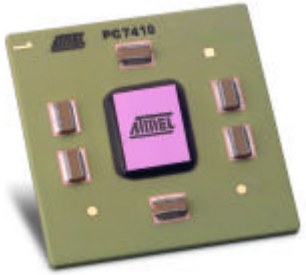
HITCE CERAMIC TECHNOLOGY – MILITARY APPLICATIONS

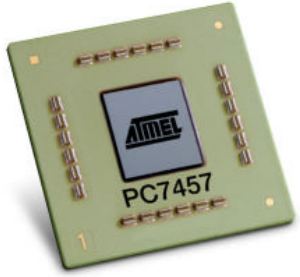
➔ Hermeticity – Underfill

Hermeticity

- ✓ Original purpose: To protect semiconductor devices from excessive moisture
- ✓ MSL 3 Qualified
- ✓ Product conditioning: 24H@125°C + Dry Pack





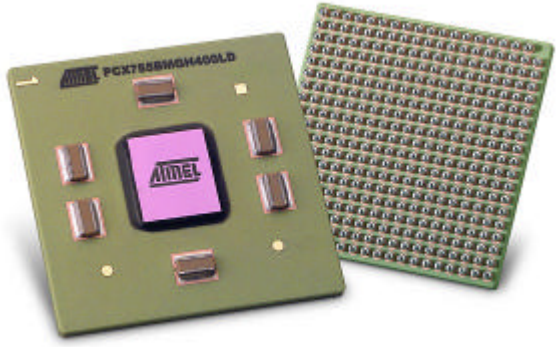


Underfill

- ✓ Sensitive element
- ✓ Drastic improvements
- ✓ Underfill certified MSL3 (Manufacturer Policy)
- ✓ Underfill MSL1 / 260°C validation (ATMEL Grenoble)
- ✓ Underfill MSL1 / 260°C product qualification in progress (Atmel Grenoble)

Today in orbit

- ✓ PC603R CI-CGA (Standard Al2O3 + Solder Column Interposer

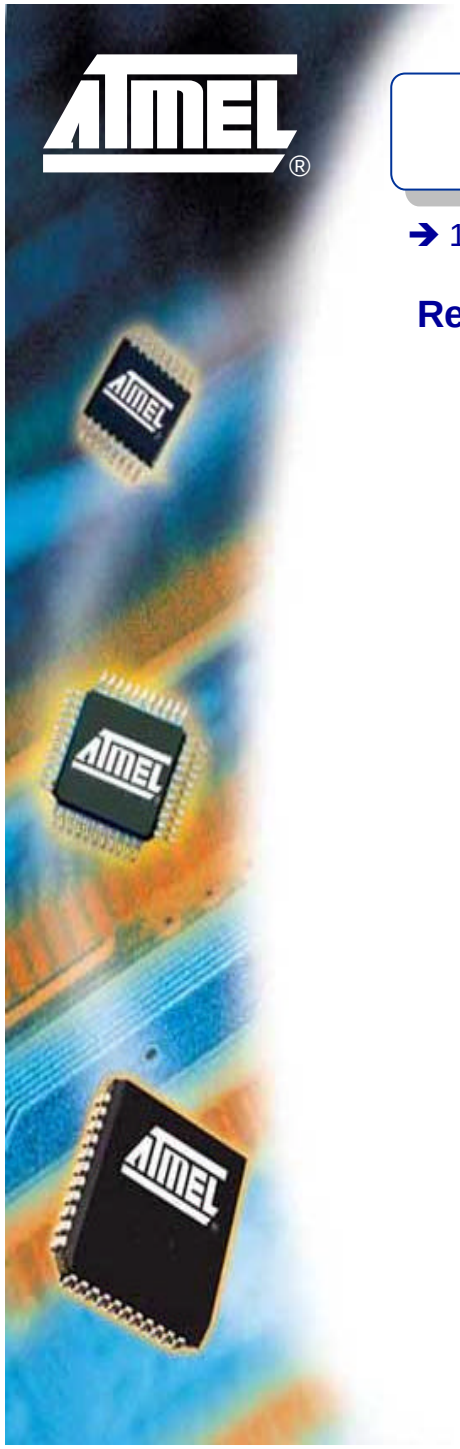


Today's flying

- ✓ HiTCE PCs 107, 7410, 7447A, 7457, 755

Flying soon

- ✓ HiTCE PCs 603R, 745, 8540, 8560



HITCE CERAMIC TECHNOLOGY – MILITARY APPLICATIONS

➔ 1st Level Reliability

Reliability level 1

- ✓ PC755 HiTCE & PC7410 HiTCE qualified : Standard Military Requirements
- ✓ Underfill improvement (Lead-free Program)

	Stress	Qual Readpoint	Results
MSL Pre-conditionning JEDEC J-STD-020A Prior to stress	Air to Air Temp Cylce -65°C to 150°C MIL-STD-883 TM1010B	2000 cylces	**PASS**
	Pressure Cooker 121°C, 100% RH, 2atm JEDEC22-A102	264 hours	**PASS**
	Liquid to liquid Thermal Shocks*	500 cylces	**PASS**
	Temperature Humidity BIAS 85°C/85% RH JESD22-A101	2000 cylces	**PASS**
	Assembly Die Pull*	Pass with both acceptable failure mode and strength	

*Testing done by Motorola

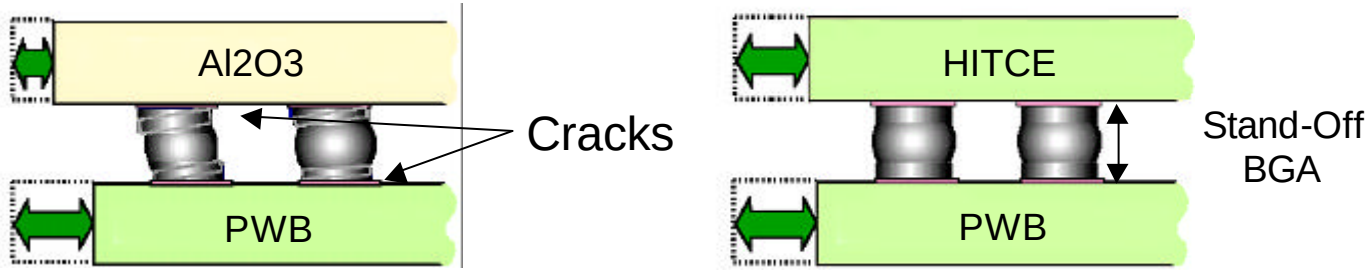
HITCE CERAMIC TECHNOLOGY – MILITARY APPLICATIONS

➔ 2nd Level Reliability

Reliability level 2

- ✓ Stand-Off BGA ~ Stress Buffer
- ✓ TCE Matching (10~12ppm°C / Range: -40°C up to 400°C)
- ✓ With or Without Metallization
- ✓ Young's Modulus of Elasticity

		CERAMIC		ORGANIC
MECHANICAL	Unit	AL2O3	HiTCE	FR4
Flexural Strength	MPa	400	175	430
Young's Modulus of Elasticity	GPa	310	75	-
Coefficient of Linear Thermal Expansion	ppm/°C	7.0	10~12	12~18



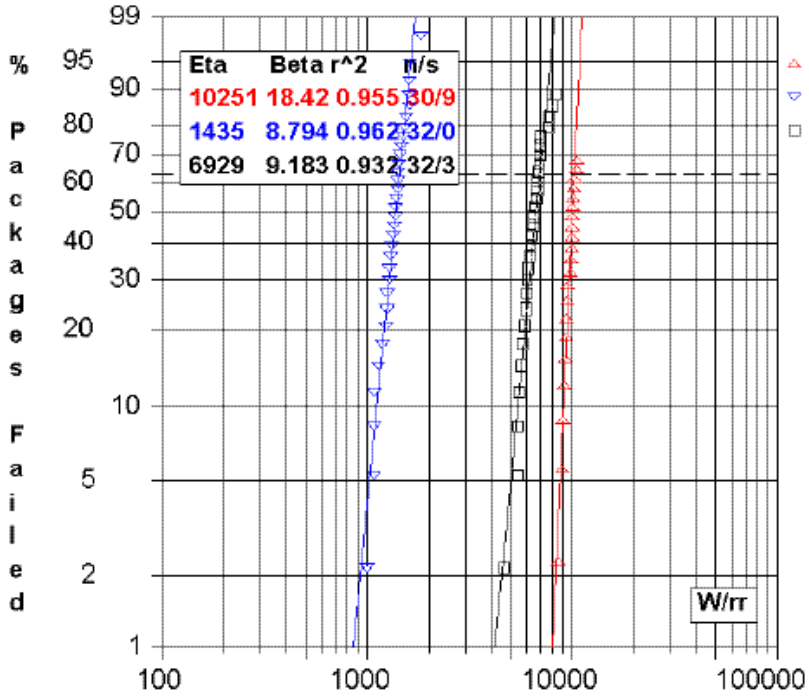
The CTE of the HiTCE package fits with the optimum range

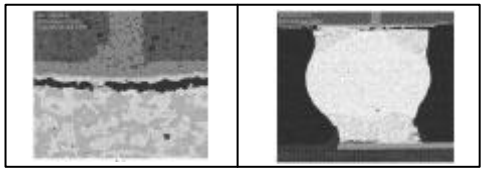
HITCE CERAMIC TECHNOLOGY – MILITARY APPLICATIONS

➔ 2nd Level Reliability

Testing Results ~ 0°C/100°C Range

- ✓ HITCE is 7.1x greater than standard ceramic
- ✓ HITCE is 1.5X greater than FC PBGA





Number of 0 to 100C Board-Level Cycles

△ HighCTE CBGA-90/10 Sphere
▽ HTCC CBGA-90/10 Sphere
□ FC PBGA-63/37 Sphere

Testing done by Motorola

0°C/100°C BOARD RELIABILITY TESTING

HITCE CERAMIC TECHNOLOGY – MILITARY APPLICATIONS

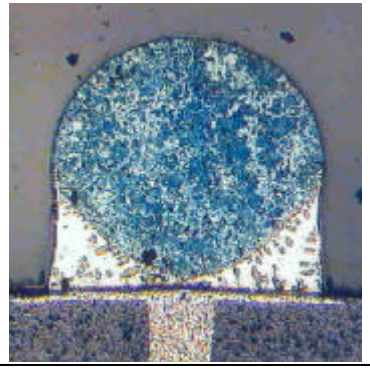
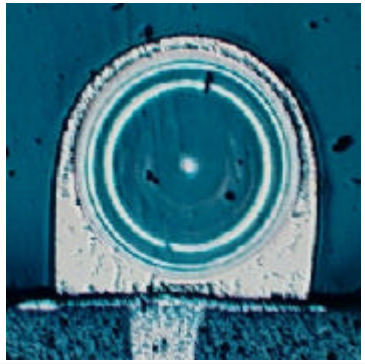
➔ Lead-Free Solution

RoHS Directive: Restriction of Hazardous Substances

- ✓ RoHS Annexe 4 - Exemptions
- ✓ Lead in high melting temperature type solders (i.e. tin-lead solder alloys containing more than 85% lead)

Polymer Core Balls qualification in progress

- ✓ Second Level Reliability Qualification: TC – 40°C / +125°C
- ✓ Polymer balls / SnAgCu Balls / LGA

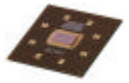
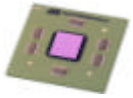
High Lead balls 90/10 Pb/Sn Conventional CBGA Eutectic Solder		Polymer Balls Polymer Core SnAg / Cu plating Conventional CBGA SAC Solder	

Summary & Conclusion

Existing Packaging Technologies

- Some Reliability Limitations when used in Military/Avionics Environments

Hi-TCE Ceramic Technology Performance Comparison

	PACKAGE TYPE			
	Al2O3 Ceramic BGA 	Flip chip Plastic BGA 	**Al2O3 w/ Columns** 	**Hi-TCE Ceramic BGA** 
Electrical Performances	☺	☺	☺	☺
Component Reliability	☺	☹	☺	☺
Board Level Reliability	☹	😐	😐	😐
Typical number of thermal cycles –40,+125°C	250	1000	1000	1000
Board Assembly Process	☺	☺	😐	☺

Hi-TCE Technology is targeted for Next Grenoble Generation Devices

- Ongoing Product Development: Power PC8540 & PC8560 microprocessors

What about SPACE ?

ESTEC – NOORDWIJK – April 27th 2005