

Use of MCM Smart HTCC technology Application to Astrium Space Digital Products

ESA, 3 May 2006 DAD 1.01.09



PRESENTATION OVERVIEW

- Why MCM technology?
- Short products description
 - MCM ERC32 (dual cavity product)
 - MCM DSP (single cavity product)
- Qualification status
 - DAD 1.01.09: Approval of Astrium F MCM Smart HTCC Technology



WHY MCM TECHNOLOGY :

- MCMs are leading edge technologies for miniaturisation of space electronics equipment offering:
 - High integration
 - High performances
 - Hi rel parts



- According to their properties, Hybrids and MCM are different solutions for integration on ceramic substrates:
 - Hybrids thick film technology
 - MCM modules : Routed HTCC (high temperature ceramic cofired) package



WHY MCM TECHNOLOGY :

a technology compliant with space requirements in terms of performances and costs

Interest Mission	Full HIREL	Mass & Volume	Low NR cost	Reduced Schedule
Science	Х	X	Х	×
Observation			Х	×
Telecom	X	X		x
Galileo		X	Х	×

WHY MCM TECHNOLOGY : an improved development schedule



MCM Technology allows to reduce schedule of processor core development by a 2-factor thanks to:

•Generic architecture / turnkey core computer

Available low/mid levels softwareNo need for basic S/W validation

•Available validation tools



WHY MCM TECHNOLOGY : a true advantage for space industry allowing technical solutions



- ➤ Full Hi-Rel Parts :
 - packaging of non Hi-Rel parts (DRAM/SRAM commercial parts, die evaluation 38 pieces according to PSS-01-608).
- > Packaging of components with a great number of pins :
 - > Not reachable by classical mounting technology, qualified up to 472 pins
 - > ASIC VASI : 500 pins, ASICs/VLSI beyond 400 pins are authorized

A common HW architecture for different applications allows to develop common Software tools or applications : low level SW, middleware SW with a accumulated experience and heritage.

MCM TECHNOLOGY : *contribution to system performances*



Higher Integration (INMARSAT 4 payload was achievable only because of MCM)

Building block which decreases non recurring tasks and encourages prime to use the function as it exists

EMC sensitivity is reduced

Possibility to upgrade COTS to Space quality level

>Time to market (product of the shelf)

≻Technical packaging answer to complex components as ASICs (500 I/Os)



MCM ERC32



The MCM ERC32 : A highly integrated Processor Core





CPB board (ERC32 14 MHz, 16 Mo SRAM, m<600g S = 37 280 mm²)

MCMERC32 (ERC32 25 MHZ, 32 Mb DRAM, 6 Mb SRAM, m = 150 g, S =5280 mm², 0 WS)

 Integration of a CPU/DSP function including the memory in a single package Multi-Chip Module:

- To deliver a fully hardware & software validated function
- To save space & mass for other functions Page 9

Dual cavity product: MCM ERC32



- The MCM ERC32SC is a very integrated solution providing a processor core that embeds the ERC32SC, its companion chip and memories
- The MCM ERC32SC main features are :
 - Processing core capabilities : Based on ERC32SC SPARC microprocessor, 25 MHz / 20 MIPS 48 Mbytes of protected memory (6Mbytes for instruction, 32 Mbytes for data) -Coprocessor (incl. MIL-STD-1553 interfaces, general User Extension Interface, serial links, RTC, ...).
 - Low mass : 110 g and low power consumption : 12 W.
 - Radiation Tolerant 30 Krad (can be improved by shielding).
 - Full Hi-Rel parts : hi-rel upgrade of commercial parts
 - ITAR free.







MCM DSP

MCM DSP21020: an integrated DSP21020 core



- DSP21020 Core including:
 - Program & Data memories,
 - EDAC protection
 - 16 bit versatile I/O port (serial & parallel I/O interface, UART, pulse generator),
 - 40 bits user interface,
 - 1355 links.
- Single cavity cofired multi-layers ceramic package
- IHD & QFP packages available
- Compliance with the Space Qualification Level & Quality Rules (development & manufacturing)
- Radiation Tolerant Technology : 30 Krads
- Operating temperature range (case temperature) : -55°C to +85°C
- Watt: 5 W @ 15 MHz
- Power voltage : 5 V
- Status in EPPL issue 6: in part 2





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Single cavity product: MCM DSP



- First generation of MCM has permitted to adjust the design with the help of an internal technology issued from hybrids (Very Fine Lines)
- Second generation of MCM shows a reduction of the number of interface and a robustness in the substrate production
- Assembly process is quite the same







MCM DSP 2nd generation

Dual cavity product: MCM ERC32



- Some technological differences between VFL and HTCC packages
 - > Accuracy of HTCC is a little less than VFL process:
 - Bondings of large dice are on 2 rows instead of one
 - ➢ VFL process is a "5"layers" max as average for HTCC is "12 layers"









Qualification status

DAD 1.01.09

Methodology



- Two steps :
 - Evaluation phase:
 - · Plan ref. HYB.MCM.NT.00421.V.ASTR
 - Qualification phase :
 - · Plan ref. HYB.MCM.NT.00415.V.ASTR

Objectives



- to identify new processes, new technologies for smart HTCC MCM
- to define an evaluation flow and a qualification flow
- to get ESA approval on work flow
- to realise trials and provide in time results to ESA/CNES experts
- to deliver qualification reports
- to get ESA/CNES approval

Domain of qualification: single and dual cavity MCMs

Evaluation tests flow



- Processes to be evaluated were:
 - AIN HTCC packaging (Kyocera manufacturer)
 - Gluing of microchips on AIN substrate with epoxy glue and repair process evaluation
 - Gluing of large dice on AIN substrate with thermoplastics glue and repair process evaluation
 - Al wire bonding of microchips on AIN
 - AI wire bonding of resistive network (thin film on AI2O3)
- All the tests gave satisfaying results



Qualification tests flow





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Item Nb	Test description	Test Method	Conditions / Remarks	
1	Bond pull test	Mil 883/2011	Condition D	
2	Internal visual inspection	Mil 833/2017	Classe K	
3	Seal test Fine leak Gross Leak test	MIL-STD-883 Method 1014 A2 PFH038	Pressure of exposure : 1.5 bars Time of exposure : 21 h	
4	Electrical measurement	Detailed specification MCM-DSP-SPEC-DA0018353-V- ASTR		
5	Screening	PID GM.HYBR.NT.879.V.ASTR Edition :02 Rév. :02	Detailed in the table of the §4.4	
6	Thermal cycling	MIL-STD-883 Method 1010	Condition B : -55°C / +125°C 100 cycles	
7	Mechanical shocks	MIL-STD-883 Method 2002	5 shocks 1000g, 0.5 ms along Y1 axis	
8	Operating life test	MIL-STD-883 Method 1005	2000 h @ +125 °C Electrical measurements at low, ambient and high temperatures are performed at 1000h and 2000h. With parameters drift calculation to be performed on electrical measurements results at ambient temperature.	
9	Random vibrations		In each of the orientations X, Y and Z $0 - 2000 \text{ Hz} : 1.25 \text{ g}^2 / \text{ Hz}$ Global = 50 gRMS Duration : 120 s	





Item Nb	Test description	Test Method	Conditions / Remarks
10	RGA	MIL-STD-883 Method 1018 Procedure 1	5000 ppmv H2O maxi. allowed + record of other gas species
	DPA		
	External visual inspection	MIL-STD-883 Method 2009.8	
	Seal test :Fine leak	MIL-STD-883 Method 1014 A2	
11	Gross leak	PFH038	
	PIND test	MIL-STD-883 Method 2020	Condition A
	Internal visual inspection	MIL-STD-883 Method 2017	Class K
	Bond pull test	MIL-STD-883 Method 2011	Condition D / Pull all wires
	Die shear test	MIL-STD-883 Method 2019	Shear all chips
12	Lead integrity	MIL-STD-883 Method 2004	Condition B2
13	Solderability test	MIL-STD-883 Method 2003	



Parts distribution for evaluation and qualification

Test file	ESA-PSS-01-606 requirements	EVALUATION		QUALIFICATION
		Quantity of test structure	Quantity of daisy chained parts	Functional parts
Sub-group 1	3 DSP + 3 ERC32	2 DSP + 2 ERC32		2 DSP + 1 ERC32
Sub-group 2	3 DSP + 3 ERC32	2 DSP + 2 ERC32	2 IHD 400 + 1 334BR	2 DSP + 2 ERC32
Sub-group 3	2 DSP + 2 ERC32		-	-
Sub-group 4	1 DSP + 1 ERC32			1 DSP + 1 ERC32 (mechanical samples)
Sub-group 5	6 DSP + 6 ERC32	-		2 DSP + 2 ERC32
Sub-group 6	3 DSP + 3 ERC32	1 DSP + 1 ERC32	2 IHD 400 + 1 334BR	



MCM PRODUCT LINE QUALIFICATION: SCHEDULE

Status today





MCM PRODUCT LINE QUALIFICATION: SCHEDULE

Status today

