Low Power DC/DC Converter Future Trends - ESA ESTEC

13th April 2005

Prepared by EADS Astrium CRISA

Overview

- The ESA initiative is recognised as a comprehensive approach to a product line of hi-rel & low cost DC/DC Converters
- Several companies
- Many times direct competitors, but...
- “while we fight, others take the business”

European industry has shown proven capability when determination exists

Requirements vs. a Competitive Product

- Initiative focused on “standard applications”
- Program specification barely descends to DC/DC Converter requirements definition
- We often accept standard DC/DC performance characteristics
- Not to over-specify if we “make” the design

Ask to the DC/DC Converter what you ask to an standard DC/DC Converter

“Put the rest outside if you need it”

The Real Needs - Digital Electronics (1/3)

- CPU - FPGA - Control Elements
  - TSC21020 - DSP
  - ERC32 TSC695 - 32 bit microprocessor
  - 80C32 - 8 bit microcontroller
  - Memories, various manufacturers

+ 5V @ 2A, less than 2W

- ASICS
  - MG2RT technology, ATMEL

+ 5V (peripheral) & + 3,3V (core)
Normally + 5V both, less than 250mA

The Real Needs - Digital Electronics (2/3)

- FPGA - ACTEL
  - RT14100 - + 5V, trends to obsolescence
  - SX - +5V peripheral, core +2,5V
    less than 250mA
- LVDS - Low Voltage Digital Signalling
  + 5V & + 3,3V @ 35mA / 4 driver
- RS422 - + 5V @ 25mA / 4 driver
- MIL-STD 1553 bus
  + 15V & + 5V @ 600mApk for 2 Ch. & simultaneity
  or…
  - 15V & + 5V, trends to obsolescence

The Real Needs - Digital Electronics (3/3)
- SUMMARY -

EADS ASTRIUM CRISA

- All +/- 5% tolerance EOL
- 300mVpp ripple & spikes
- Built-in soft start
- Shut down pin
- No switch-off by SEU, SEE transients <10% TBC
- Sequencing capability, “the lower, first”
- Overvoltage protection, external?
- Reset signal, external time-out capacitor, CMOS levels, + 4,5V On & + 4V Off thresholds

CORE
External
Both

The Real Needs - Analog Electronics

- Housekeeping & external thermistors, voltage & current acquisitions, … “12 bit”

  +/- 15V & +5 V typically

  +/- 5% tolerance EOL

  +/- 2% ripple - 500mVpp spikes

  +/- 12V & +5 V some cases, e.g. AD676

  +/- 1% ripple

  +/- 3% spikes in +/- 12V

  +/- 3% spikes in +5V

- Digital & Analog GND at ADC
- Symmetrical outputs < 250mA
- + 5V < 100mA

The Mechanical & Thermal Interface

- Converter on PCB
- I/P & O/P pins
- Heat evacuation through screws
- Reference temperature 70ºC
- Size to be minimised
- Mass to be minimised

The General Design Requirements

- Three output models, +/-15V & +5V or +/-12V & +5V
- Single output models, +5V, +3,3V
- Part of the CM & DM filters
- Make possible several DC/DC connected to same bus
- 2 Product Ranges w.r.t. Bus voltage,
  - +28V regulated or not
  - +50V regulated
- Tolerance to “typical” EMC environment
- >36MeV/mg/cm^2, > 50kRad

Some Ideas on the Design

- ITAR free
- SMT “as much as possible”
- Same PWM controller open different ones
- Same transformer size
- Power Switch Bipolar, FET?
- No special protections, only duty limitation & bus undervoltage (overvoltage TBC)
- Synchronisation capability?
- Parts Quality Level depending on programs
- Extended range commercial components + radiation test at module level

Conceptual Block Diagram