Impact of irradiations performed at liquid helium temperatures on the operation of 0.7 μm CMOS devices and read-out circuits

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***Abstract*—It has become clear that the effect of total ionizing dose (TID) and displacement damage on device performance strongly depends on its operation temperature. It is the aim of this paper to describe a dedicated set-up for executing biased irradiation testing at low temperatures. As a test vehicle prototype chips for the HERSCHEL mission, fabricated in a standard 0.7 μm CMOS technology, have been used. In order to get a better insight in the fundamental radiation damage mechanisms, also simple test structures (transistors) have been exposed to the same radiation dose of ^{60}Co γ's or 60 MeV protons. It is shown that from a viewpoint of TID damage the read-out circuits will survive the mission's estimated total dose. There is a good agreement between the observed circuit performance shift and the parameter shift derived from the n- and pMOSFETs.**

***Index Terms* – CMOS, proton irradiation, cryogenic electronics, liquid helium temperatures, TID damage.**

I. Introduction

For the development and design of cryogenic electronics, silicon Complementary Metal-Oxide-Semiconductor (CMOS) is the technology of choice [1]-[4]. Particularly at liquid helium temperatures (LHT), CMOS devices exhibit superior performance compared for example with their bipolar counterparts [4]. In fact, the low temperature operation of MOS transistors offers some clear advantages compared with room temperature, if one considers the improvement in carrier mobility and device leakage [4]. One aspect, however, which may raise significant concern in view of space applications is the response to radiation damage [5]-[6]. It is known for some time that Total Ionizing Dose (TID) damage leads to a higher charge trapping in SiO_2 at low temperatures [5]-[9] and, hence, to a worse degradation of the static device and circuit parameters. This is essentially related to the immobility of created holes in the oxide, which prevents them from transport to the Si-SiO_2 interface.

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As a consequence, significant positive fixed charge and negligible interface charge is formed during cryogenic irradiations. Of course, it would be convenient if one can extrapolate to some degree the room temperature radiation response to the case of low temperature operation. However, experience has learnt that this is not a good approach [10]-[11]. Therefore, a need exists for cryogenic radiation testing, comprising both γ- and proton irradiations, if space applications are envisaged.

It is the purpose of this paper to describe a dedicated set-up, which has been developed in the frame of an ESTEC contract, allowing both γ- and proton irradiations in a broad temperature range. The driving force for this effort was the radiation testing of the cryogenic read-out electronics (CRE) circuits for the Photodetector Array Camera & Spectrometer (PACS) instrument, which are under development for the HERSCHEL mission [12], to be launched in the spring of 2007. Results will be reported of the radiation testing at liquid helium temperatures (LHT) of transistors fabricated in the 0.7 μm CMOS technology used for the prototyping of the circuits. These will be compared with previous data, obtained after a room temperature γ- or proton irradiation of similar devices [13]-[15]. The different degradation behaviour observed in both cases strongly emphasizes the role of the radiation testing temperature. Overall, less pronounced parameter changes have been observed in this work, which is supported by the minor performance shift found for the CREs under γ-irradiation. However, cryogenic 60 MeV proton irradiations may create catastrophic failure at total doses in the range of 10 krd(Si). This points out the relevance for both proton and γ-radiation testing for cryogenic space electronics.

II. Experimental

A cryogenic radiation set-up should not only allow to irradiate at low temperatures but at the same time to bias the circuit and perform electric testing before, during and immediately after the exposure, in order to avoid annealing. For that purpose, a flow cryostat from JANIS was used, which contains 10 coaxial cable connections and 19 unscreened wires in twisted pairs, sufficient to power the PACS electronics. Test devices were mounted in 40 pins dual-in-line packages, which were placed on a dedicated sample holder. Figure 1 shows a mounted device for the case

of the γ-irradiations, while Fig. 2 exhibits the modified assembly for the 60/65 MeV proton irradiations. The former took place in ESTEC, the latter at Cyclone in Louvain-la-Neuve. The cryostat was closed with a glass window during the γ-exposures, which was replaced by a 150 μm thick stainless steel foil for the 60/65 MeV protons, since the energy loss in the thick glass window would otherwise be too high. The set-up was placed vertically on a movable table and a mechanical support, which enables to adjust the height and lateral position. Before cooling, the sample space was evacuated, using a turbo-pump.

Cooling was performed by pumping continuously liquid helium through the heat exchanger of the cryostat; the temperature was controlled by a silicon diode sensor (standard DJ 670 type) and a Lake Shore Temperature Controller. It took typically about 1 h to reach the floor temperature of about 5 K. Very stable temperature operation was achieved, as can be judged by Fig. 3. The biasing and irradiation did not induce a marked temperature increase. An important observation is that for the dosimetry, the distance of the cryostat with respect to the γ-ray source was very critical (a few mm resulted in 20 rd(Si)/min difference). For the proton irradiations, on the other hand, it was decided to collimate the beam to a diameter of 3 cm, in order to limit activation of the copper parts from the sample holder.

The operation of the circuits was monitored during the irradiations, by the set-up shown in Fig. 4. For the characterization of single transistors, a constant bias of +5 V was applied to the gates of the nMOSFETs, while all the other terminals were grounded, including the gate of the p-MOSFETs. The transistors were part of an amplifier circuit, allowing direct assessment of the individual devices. It should also be remarked that the gates were foreseen with an Electrostatic Discharge (ESD) protection diode. Before and after the irradiation, input- and output curves were registered using an AGILENT Parameter Analyzer.

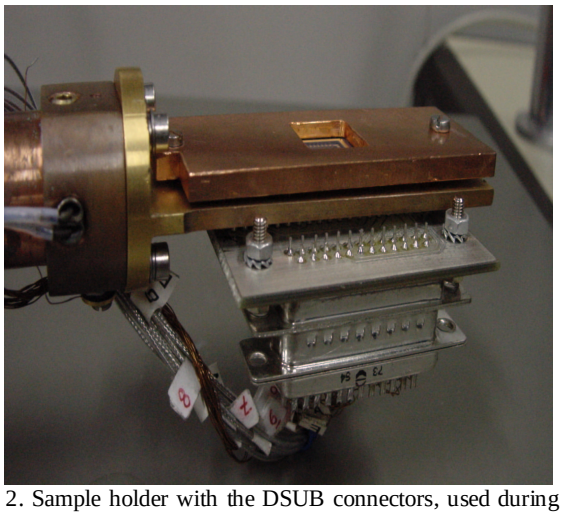

Fig. 2. Sample holder with the DSUB connectors, used during the proton irradiations.

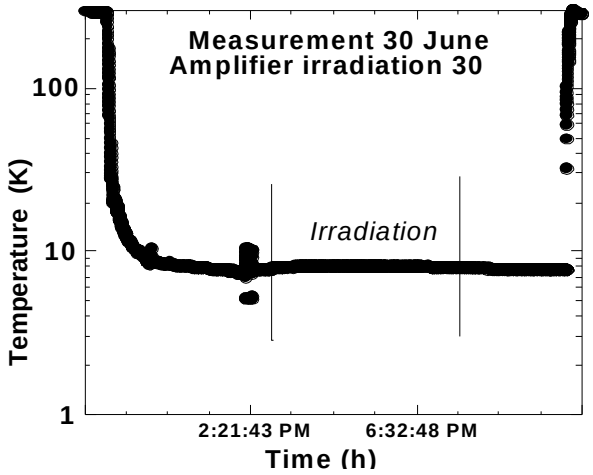

Fig. 3. Evolution of the sample temperature during cooling, γ-irradiation and warm up.

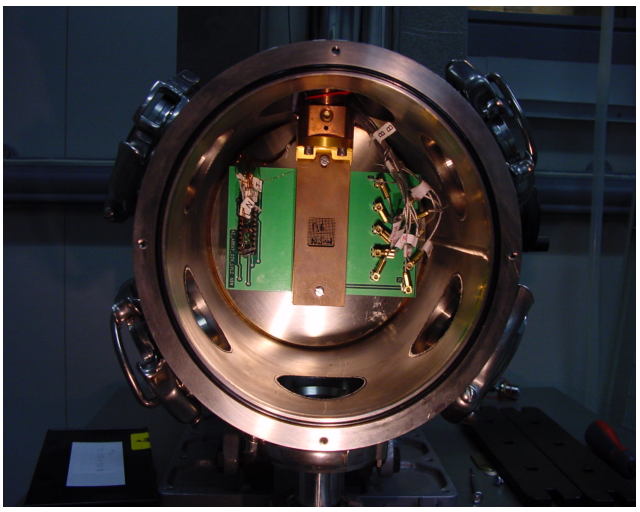

Fig. 1. PACS circuit mounted in the cryostat before the γ-irradiations at ESTEC.

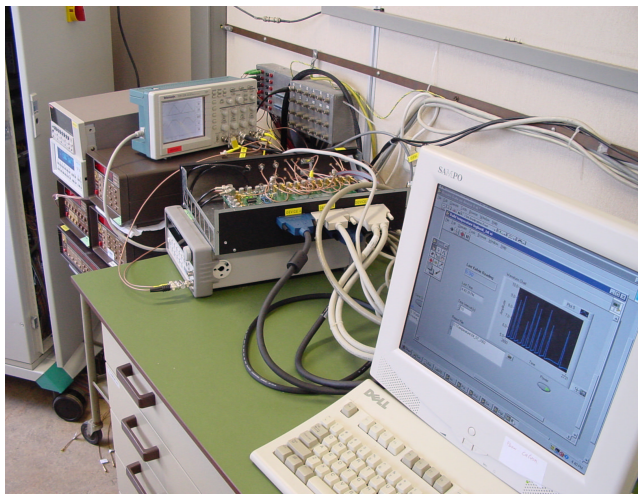

Fig. 4. Control and biasing electronics for the PACS circuitry.

III. MEASUREMENT CONDITIONS AND TRANSISTOR RESULTS

The ^{60}Co γ-irradiations were performed at a dose rate of ~100 rd(Si)/min up to a total dose of 15 or 30 krd(Si), while the 60 and 65 MeV proton irradiations have been executed in two rounds at a dose rate of 10^8 p/cm^{2}s or $3x10^8$ p/cm^{2}s, respectively, up to a fluence of ~10^{11} p/cm^2. These are the radiation levels expected during the HERSCHEL mission.

The components have been fabricated in a 0.7 µm single polysilicon CMOS technology at AMI Semiconductor (Oudenaarde, Belgium), whereby the gate length of the transistors (L) was 10 µm; their width W=22 µm (n-) or 130/65 µm (pMOSFET). Figures 5 and 6 show typical input characteristics at LHT before and after a 15 krd(Si) γ-irradiation, indicating marginal changes in the subthreshold slope S, threshold voltage V_T or the transconsductance G_m. One important observation is that the ESD protection is no longer functional at liquid helium temperatures, which is derived from the 'on' diode characteristic in reverse operation. The good radiation performance is further confirmed by the output (I_D-V_{DS}) characteristics of Figs 7 and 8, showing no kink effect, which is usually a problem for n-channel devices at 4.2 K [4],[6].

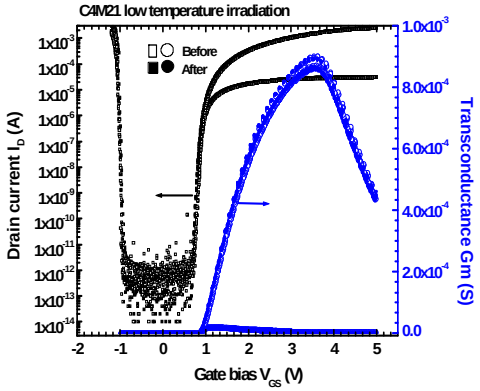

Fig. 5. Drain current and transconductance before and after gamma irradiation versus gate voltage V_{GS} from 0 V to 5 V with 10 mV steps for a drain bias of 25 mV (o) and 2.5 V (□) at 7 K. The curves have been measured for a 22 µm/10 µm nMOSFET.

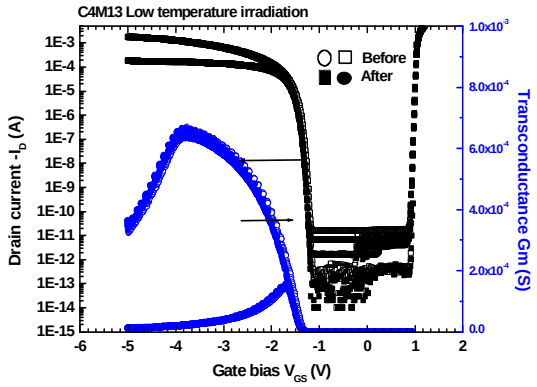

Fig. 6. Drain current and transconductance before and after gamma irradiation versus gate voltage V_{GS} from 0 V to –5 V with –10 mV steps for a drain bias of –25 mV (o) and -2.5 V (□) at 7 K. The curves have been measured for a 65 µm/10 µm pMOSFET.

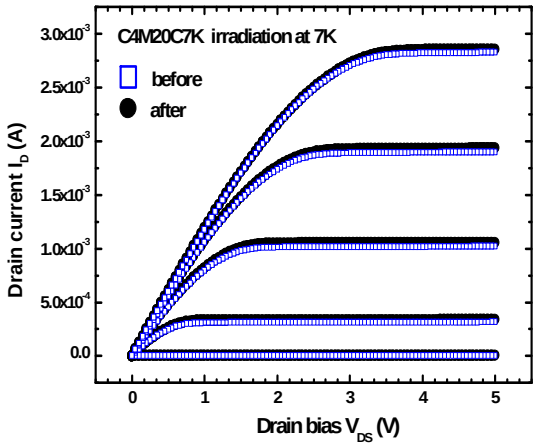

Fig. 7. Drain current versus drain voltage V_{DS} from 0 V to +5 V with 10 mV steps for different gate biases from 1 to 5 V with 1 V steps at 7 K, before and after a 15 krd(Si) γ-irradiation.

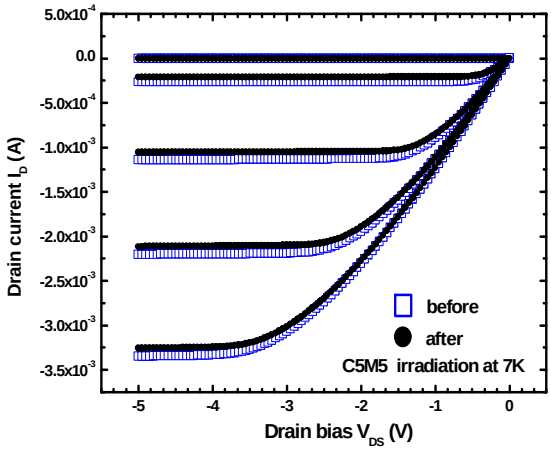

Fig. 8. Drain current versus drain voltage V_{DS} from 0 V to –5 V with -10 mV steps for different gate biases from -1 to –5 V with –1 V steps at 7 K, before and after a 15 krd(Si) γ-irradiation.

Generally, no degradation of the subthreshold characteristics has been observed in Figs 5 and 6. However, occasionally, a hump in the subthreshold I_D-V_{GS} was found pointing to parasitic conduction along the LOCOS (LOCal Oxidation of Silicon) edges of the transistors. This is illustrated in Fig. 9. It has been reported before [16],[17] that this type of leakage current becomes more pronounced when a transistor is cooled down. This is related to the stronger temperature dependence of the threshold voltage of the device isolation related edge transistor, which shifts the 'on' region beyond the main channel at room temperature, while the corresponding V_T is lower at cryogenic T.

Normally, one expects this type of leakage to worsen upon irradiation for an n-channel transistor, since the expected hole trapping will be more pronounced in the thicker LOCOS oxide, generating a more pronounced V_T lowering [18]-[19]. In contrast, Fig. 9 demonstrates that under a LHT gamma irradiation, the LOCOS related edge leakage disappears after a total dose of 15 krd(Si). This suggests and increase of the parasitic V_T, which can be a

consequence of the creation of a net negative charge in the oxide or at its interface. However, as interface-state generation is absent at cryogenic temperatures we have to assume that electron trapping has occurred during the γ-exposure at LHT.

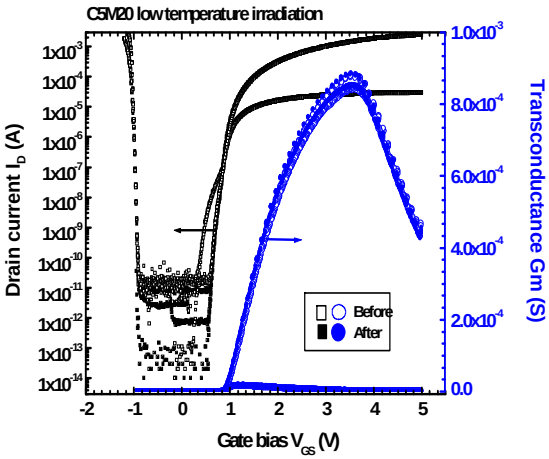

Figure 9: Drain current and transconductance before and after gamma irradiation versus gate voltage V_{GS} from 0 V to 5 V with 10 mV steps for a drain bias of 25 mV (o) and 2.5 V (□) at 7 K before and after a 15 krd(Si) γ-irradiation.

IV. CIRCUIT DESCRIPTION AND CRYOGENIC RADIATION TESTING

A. *Circuit Description*

The Photodector Array Camera & Spectrometer (PACS), one of the focal plane instruments aboard the HERSCHEL Space Observatory (launch spring 2007), combines an array of bolometers and 2 arrays of Ge:Ga detectors (stressed and unstressed) to perform photo/spectrometric imaging in the wavelength 57-210 μm [12]. Since the 16x25 Ge:Ga arrays work at 1.2 K for optimal detectivity, the readout, placed as close to the detector array as possible, is required to work at 4.2 K in order to avoid strong thermal gradients and interference with the detectors. An 18-channel readout, based on a self-biasing AC-coupled Capacitive Feedback Transimpedance Amplifier input stage ("CTIA"), has been proposed to meet the specifications on noise, detector stability, drift and power consumption. Figure 10a shows a block schematic of a single channel. During a so-called destructive reset phase, the integrating capacitor is shorted and the reset level or start of the integration ramp is set as well as the biasing voltage ("zero bias") of the detector at the input.

In the recording phase, the small detector signal currents get integrated on a feedback capacitor C_f. To accommodate for a large range of input signals, the value of the capacitor is selectable. The level shifter following the input stage enables the use of pMOS[1] buffers for sample-and-hold stage and multiplexed output driver, by downshifting the output signal of the amplifier. All channels record the signals of their detector simultaneously. The slopes are sampled during "non-destructive" reset phases in a sampling-up-the-ramp scheme and time-multiplexed to a single output by a 18-bit shift register). In a small digital part, the control signals for the single channels (resets) and for the 18-bit shift register are generated out of externally supplied time signals (clock and sync).

For design testability, not only the complete Cold Readout arrays (CRE's), but also single channels and separate building blocks have been implemented on silicon. During the radiation tests, both the full arrays as well as the building blocks were irradiated in order to have diagnostic tools in case of a malfunction of the CRE array after radiation since no test-probing paths could be implemented in the final design. The specification on radiation hardness was set at 15 krd(Si) in final orbit.

The layout of the PACS Cryogenic Read-out Electronics (CRE) circuit is given in Fig. 10b [12]. Besides the full CRE, separate building blocks (buffer, digital part, amplifier) were also available for radiation testing.

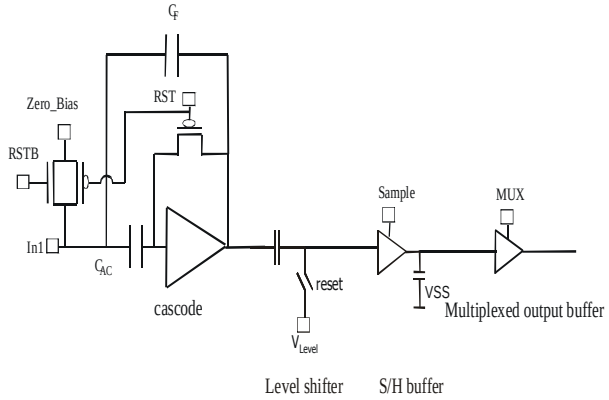

Fig. 10a. Layout of one channel of the PACS CRE array.

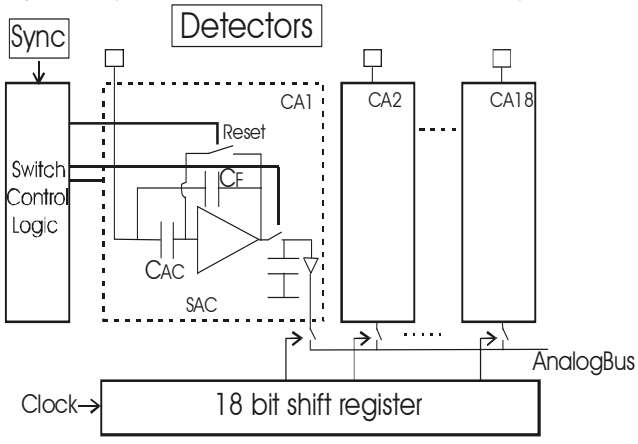

Fig. 10b. Block schematic of a complete PACS CRE array.

[1] pMOS transistors are preferred over nMOS transistors in cryogenic circuit design since low temperatures have less influence on their behaviour.

B. Cryogenic gamma irradiations

In this section, the results of the gamma irradiation tests on PACS CRE electronics and its building blocks are described. The radiation response of a pMOS buffer circuit at 8 K is illustrated in Figs 11 and 12, for different γ-doses. Overall, the degradation observed in the transistor characteristics is in line with the small changes found for the circuit operation. In Figures 11 and 12, the input-output characteristic of buffer002, level shift and gain for different instants before and during the radiation are represented. It is found that the output level shifts over less than 50mV as a result of the radiation. This shift can be explained by a V_T shift of the pMOS transistors, observed in the component tests. However this radiation-induced shift of the offset level is of no concern in the circuit, since the measurements are based on the slopes rather than the absolute DC levels. The variation in gain over the total dose of 15 krd is comparable with the maximum acceptable shift over 1 hour at 4.2 K and thus not problematic either.

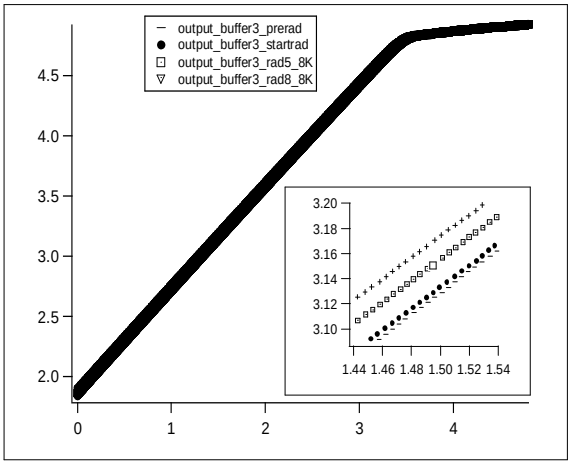

Fig. 11. Input-Output characteristics of a pMOS buffer at low temperature, before and during gamma irradiation. Measurement 8 is done at 15 krd(Si).

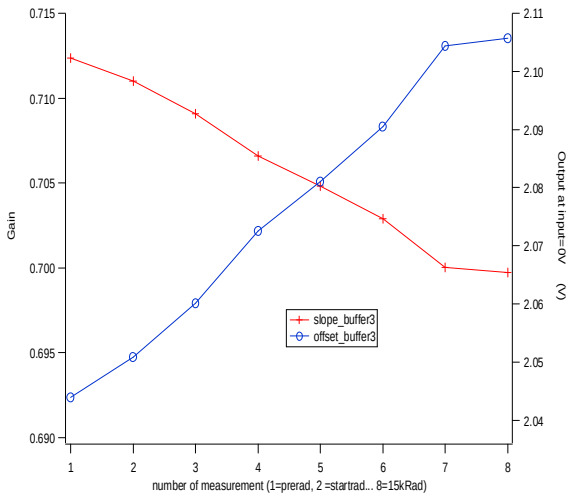

Fig. 12. Gain and offset of a pMOS buffer at low temperature, before and during gamma irradiation.

C. Cryogenic proton irradiations

Immediately after the start of the proton irradiation, it was noticed that the slope of the array changed and all channels seemed to integrate the same input current as shown by Fig. 13. A possible explanation for this phenomenon could be that the shift register is stuck-at-one at the output for channel 18, but a more likely explanation is that all of its outputs are stuck-at-one, connecting all channels in parallel to the output. The latter would also explain the shift in slope between start of the radiation and 9 krd. When all channels are connected to the output, the apparent gain of the output buffer is smaller as the variations in channel 18 are damped by the other 17 non-integrating channels.

After approximately 10 krad, the measurements show a systematic degrading of the digital logic in the readout array. The MUX signal is not always present, resulting in gaps in the slope. The integration, however, seems to continue as the output resumes to a normal value after this discontinuities, indicating that the analogue part, where the integration takes place is not affected by the radiation. An effect appearing almost simultaneously with the interruption of the MUX signal is the disruption of the reset signal, resulting in an occasional double integration time. At 11.75 krd, the reset signal seems to have completely disappeared and all channels stay constantly saturated. At 15 krd, no output is present anymore.

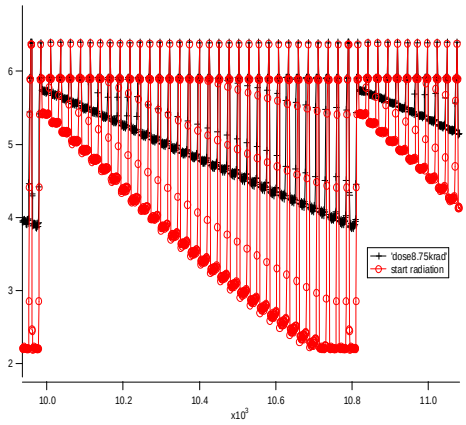

Fig. 13. Changing slope of a PACS circuit output signal during irradiation up to a dose of 9 krd.

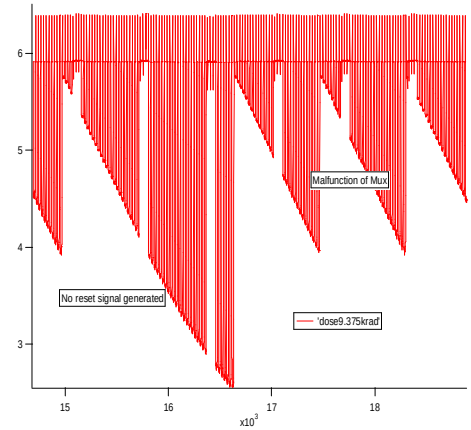

Fig. 14. First errors in output - MUX signal is stuck at zero and reset is missing.

Cryogenic proton irradiation of a second device (same production run) yielded a very similar behaviour. However, during a second proton irradiation round at 65 MeV, all tested circuits survived a total dose of 20 krd(Si) and higher, both at RT and 4.2 K. This illustrates the need for sufficient statistics of the cryogenic radiation testing. It should be emphasized that all tested circuits came from the same processing batch and wafer, eliminating process variations as the origin of this different behaviour.

V. Discussion

One of the more fundamental goals of the present study was to investigate the role of the irradiation temperature on the degradation of CMOS at LHT. It has been demonstrated previously that room-temperature (RT) exposures had a pronounced impact on the cryogenic operation of MOSFETs belonging to the same technology [13]-[15]. This is illustrated more clearly in Fig. 15, showing the input characteristics at 4.2 K of a 10 µmx5 µm nMOSFET with Lowly Doped Drain (LDD) before and after a 10^{11} p/cm^2 60 MeV biased proton irradiation at 300 K. A marked reduction of the V_T and a strong increase of the drain current and transconductance are obvious. Compared with Fig. 5, a room-temperature 60 MeV proton exposure seems to produce much more pronounced changes. The same applies for the output characteristics of Fig. 16 for a 100 krd(Si) γ-irradiated nMOSFET without LDD: while the low-temperature kink is present before, it has disappeared after the RT irradiation.

These results demonstrate the impact of the testing conditions on the assessment of the radiation performance of cryogenic CMOS. It appears here that executing the exposures at room temperature and allowing for some annealing before cryogenic testing leads to more degradation of simple test structures. This points to the importance of, e.g., radiation-induced interface-states, which are created at room temperature on the overall device performance. Needless to say that also the technological details (LDD or no LDD,…) can have a strong impact on both the cryogenic behaviour [13,14] and the radiation response [15].

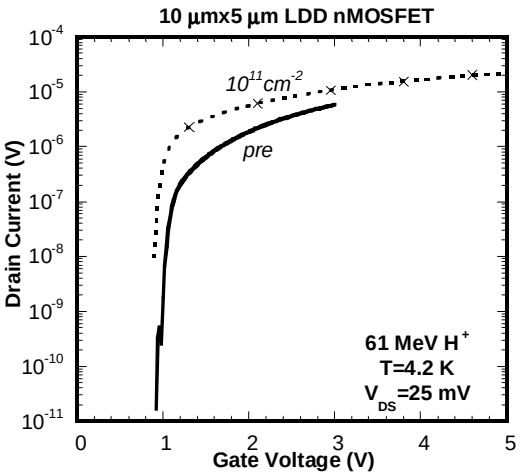

Fig. 15. Input characteristics in linear operation (V_{DS}=25 mV) and at 4.2 K for a 10 µmx5 µm nMOSFET with LDD, exposed to 10^{11} p/cm^2 at 300 K.

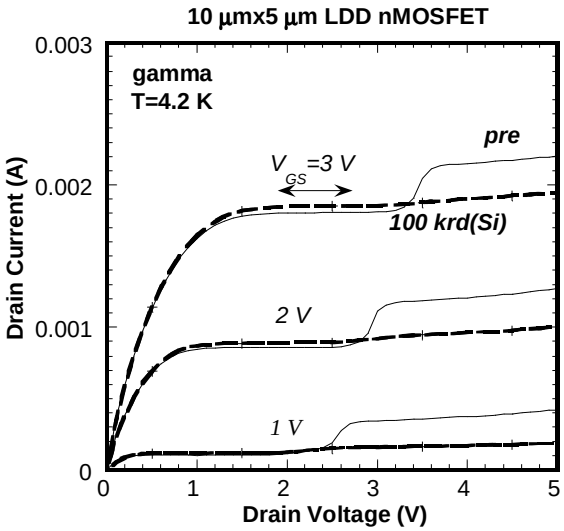

Fig. 16. Output characteristics at 4.2 K for a 10 µmx5 µm nMOSFET before and after exposure to a 100 krd(Si) γ-irradiation at 300 K.

With respect to the circuits, the following can be concluded: while total-dose testing at LHT did not reveal any particular functionality problems for the doses expected during the HERSCHEL mission, this is not the case for high-energy proton irradiations. Both at room temperature and at LHT catastrophic device failure could be observed in certain cases (although not systematic) for proton fluences lower than required for the mission. At the moment, there is a strong suspicion that the digital part is failing probably due to a combination of TID charging of gate or more likely isolation oxides and some transient effect. More work is needed to find the exact origin.

VI. Conclusion

The set-up, which has been developed, offers a flexible solution to carry out cryogenic irradiations and in-situ electrical testing for space electronics. At the same time, it was confirmed that the radiation response at liquid helium temperatures may differ from the one at room temperature. More importantly, it was also found that the behaviour after low temperature γ-exposures cannot be translated to the case of protons, which is equally important for space applications.

VII. Acknowledgments

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