Radiation-Induced Back Channel Leakage in 60 MeV-Proton-Irradiated 0.10 μm-CMOS Partially Depleted SOI MOSFETs

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***Abstract*-- In this paper, the degradation of 0.10 μm-CMOS Partially Depleted (PD) SOI MOSFETs subjected to 60 MeV proton irradiation for space applications assessment is analyzed. It is observed a radiation-induced increase of the leakage current in the subthreshold region of the NMOSFETs characteristics, which is more important in the case of mounted devices irradiated under bias. By studying the static and transient characteristics on devices with different geometries and bias conditions, the degradation is demonstrated to be originated by positive charge trapping in the buried oxide, inducing an edge parasitic back channel conduction. The effective density of trapped holes is estimated to be around $7.5 \cdot 10^{11}$ charges/cm^2 for the devices biased during the irradiation, whereas this is found to be about three times smaller in the case of the devices not biased during the irradiation.**

Under the studied experimental conditions, no significant changes are observed in the above threshold region of the N and PMOSFETs characteristics, making this technology suitable for space applications. Furthermore, the irradiation is not found to significantly change neither the magnitude nor the position of the Electron Valence Band gate tunneling-induced 2nd peak of the transconductance, characteristic of these ultrathin gate oxide PD SOI transistors. This is in agreement with the results obtained from non-irradiated devices measured at positive back gate voltages, what is found to generate an irradiation-like parasitic back channel conduction. It is also derived that no significant changes in the majority carriers generation and recombination lifetimes are introduced by the irradiation, which is supported by the results coming from the measurements of front gate switch-off I_D transients.

***Index Terms*—Buried oxide, floating body effects, proton irradiation, radiation effects, silicon on insulator (SOI), switch off transient, total dose effects, transconductance peak.**

I. INTRODUCTION

SILICON-on-Insulator (SOI) MOSFETs have several intrinsic potential advantages over their bulk Si counterparts as components to be operated in radiation-harsh environments [1,2]. In particular, the thin semiconductor film provides better resistance against transient ionization effects like Single Event Upsets or Latch-up [3]. However, the thick SOI buried oxide introduces an additional constraint due to total ionizing dose charge trapping [3]. Moreover, the presence of floating body effects [4], some of them recently originated by the aggressive front gate oxide scaling [5,6], can limit to some extent their performance.

The continuous miniaturization process has implicitly led to radiation-hard front gate oxides, with thickness below the trapped-hole tunneling limit. This explains the reported radiation tolerance of 0.35 μm [7,8] and 0.25 μm [9] Partially Depleted (PD) CMOS on SOI. However, since the early times, there has been an important concern about total ionizing dose charge trapping in the buried oxides [10-11]. Studies have been carried-out on SOI technologies with a wide range of substrate qualities [12] and, in a number of cases, a significant impact of buried oxide trapped charges on device front characteristics has been pointed out [10,13].

The increasing gate coupling associated with the reduction of the semiconductor film thickness is expected to make SOI MOSFETs more sensitive to buried oxide charge trapping [14]. In this way, while an increase of the leakage current in the subthreshold region is reported for PD SOI NMOSFETs [15], a decrease of the top-gate threshold voltage is observed in Fully Depleted (FD) NMOSFETs [15].

In this paper, the degradation of deep-submicrometer 0.10 μm-CMOS Partially Depleted (PD) SOI MOSFETs subjected to 60 MeV proton irradiation for space applications assessment is analyzed. The irradiation is found to be responsible for an increase of the leakage current in the subthreshold region of the NMOSFETs characteristics. The radiation-induced damage is investigated by studying the static and transient characteristics of devices with different geometries and bias conditions.

The impact of the irradiation on the magnitude and position of the Electron Valence Band gate tunneling-induced 2nd peak of the transconductance, characteristic of these ultrathin gate oxide PD SOI transistors [5,6], is also evaluated. Finally, the impact of irradiation on the front gate switch-off I_D transients from gate voltages above and below the threshold voltage for Electron Valence Band gate tunneling is also studied.

Manuscript received September 12, 2003. The work of J. M. Rafí was supported by a Postdoctoral Marie Curie Fellowship from the European Commission.

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II. DEVICES AND EXPERIMENTAL PROCEDURE

The PD SOI MOSFETs irradiated in this study were fabricated in a 0.10 μm-CMOS process using a PELOX (Polysilicon Encapsulated LOCOS) isolation scheme, a 2.5 nm Nitrided gate Oxide (NO), a 150 nm polysilicon gate and 80 nm nitride spacers. Processing was performed on 200 mm diameter UNIBOND wafers, resulting in a final film thickness of 100 nm. The buried oxide thickness was 400 nm (fig. 1).

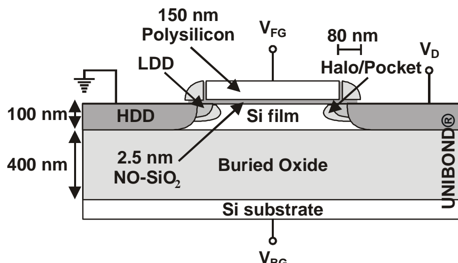

Fig. 1. Sketch of a PD SOI MOSFET showing some of its main characteristic features and the nomenclature for the applied biases.

The test structures have common gate and source configuration with separate drain pads. There is no film contact. Transistors with polysilicon gate lengths (L) ranging from 0.08 μm to 10 μm and gate widths (W) from 0.2 μm to 10 μm were studied in this work. In order to be able to perform a biased irradiation, some chips were mounted in 24 pins dual-in-line packages.

Both, "on wafer" and "mounted" chips were subjected to two consecutive (40 days in between) 60-MeV proton irradiations at the Cyclone cyclotron facility (Louvain-la-Neuve), each one up to a fluence of 10^{11} protons/cm^2, which corresponds to a dose of about 13.5 krd(Si), suitable for space applications radiation-hardness assessment [3].

During the irradiation, the gates of all the mounted transistors (NMOSFETs and PMOSFETs) were biased at the positive bias corresponding to the power supply voltage for this technology (+1.5 V), while all the other terminals were grounded. All measurements were performed using an HP-4156 Parameter Analyzer in a controlled temperature room, with a light-proof and electrically shielded probe station.

III. RADIATION-INDUCED DEGRADATION

A. Mounted devices (biased during irradiation)

Figures 2 and 3 show typical drain current (I_D) and transconductance (g_m) versus front gate voltage (V_{FG}) characteristics measured at zero back gate bias (V_{BG}= 0 V) for a long channel (L=10 μm) NMOSFET and PMOSFET, respectively, before and after the two irradiation steps.

From fig. 2, a clear increase of the subthreshold leakage is observed after the first irradiation step on the NMOSFETs. In this way, for V_{FG} below the threshold voltage ($V_T \approx$ 0.35 V) and down to negative V_{FG}, an important increase of I_D level is registered above the experimental limit of detection of about 10^{-12} A for these long-L mounted devices.

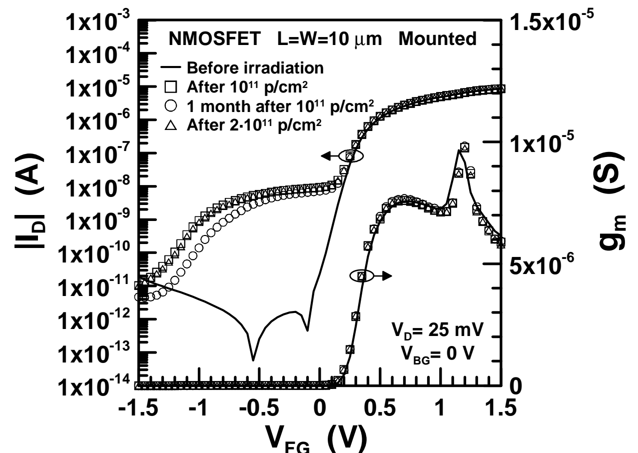

Fig. 2. I_D and g_m versus front gate voltage (V_{FG}) characteristics measured at V_{BG}= 0 V for an L=W= 10 μm mounted NMOSFET before and after the two consecutive 10^{11}proton/cm^2 irradiations.

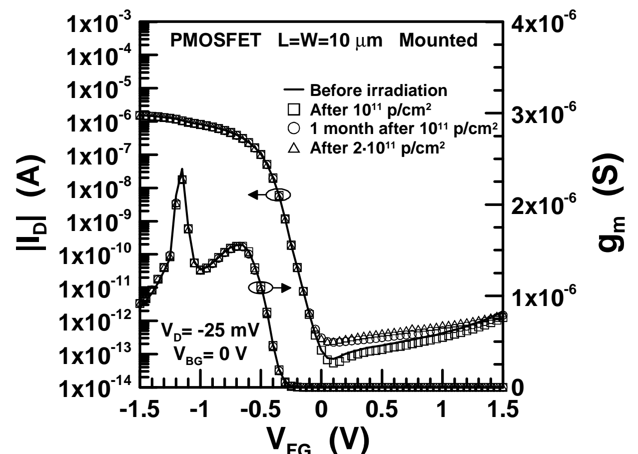

Fig. 3. I_D and g_m versus front gate voltage (V_{FG}) characteristics measured at V_{BG}= 0 V for an L=W= 10 μm mounted PMOSFET before and after the two consecutive 10^{11} proton/cm^2 irradiations.

This radiation-induced leakage current has been found to exhibit perfect symmetry to source/drain (S/D) interchange, indicating that there is no S/D asymmetry in damage distribution. From the results, the parasitic leakage is found to be somewhat reduced with post-irradiation elapsed time, pointing to the existence of some room temperature annealing of the radiation-induced damage.

In contrast, no appreciable radiation-induced degradation has been observed for the p-channel MOSFETs (fig. 3).

An important feature of the characteristics of these ultra-thin gate oxide PD SOI MOSFETs is the occurrence of a second peak in the transconductance for $|V_{FG}|$ values around 1.2 V (figs 2 and 3). This 2nd g_m peak is due to the injection of majority carriers in the floating body by Electron Valence Band (EVB) tunneling [5,6], what is quite analogous to the classical impact-ionization related kink effect. The main difference is that the excess majority carriers are introduced into the film by gate-body direct tunneling when V_{FG} surpasses the threshold for EVB tunneling. Consequently, it is observed already for small drain biases (V_D) and is, therefore, present in the ohmic operation regime. It has been also observed that this 2nd g_m peak is less pronounced for shorter

gate lengths or narrower transistors [5,6,16], which has been attributed to the impact of the junctions or the edges, enhancing the generation-recombination processes and reducing the floating body effects.

Figure 4 shows the length dependence of both, the conventional (mobility-related) 1st g_m peak (g_{mmax}) and the EVB-related 2nd g_m peak, measured for W= 10 μm NMOSFETs and PMOSFETs before irradiation.

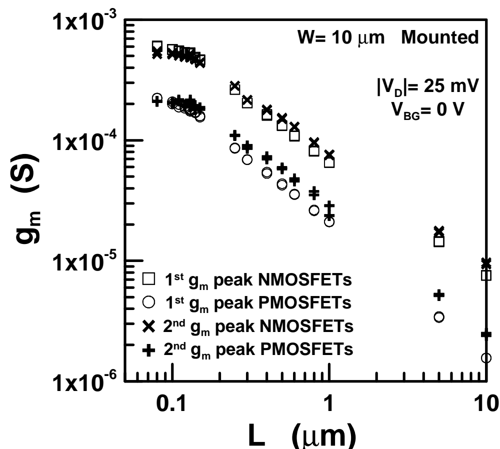

Fig. 4. Conventional (mobility-related) 1st g_m peak (g_{mmax}) and Electron Valence Band-related 2nd g_m peak versus channel length for W= 10 μm NMOSFETs and PMOSFETs measured before irradiation.

As derived from the g_m results of figs 2 and 3, no significant degradation has been observed in the above-threshold portion of the characteristics of either n- or p-channel transistors. In this way, fig. 5 shows the extracted values for threshold voltage shift (ΔV_T) and 1st transconductance peak degradation (Δg_{mmax}) versus L for mounted NMOSFETs and PMOSFETs after irradiation.

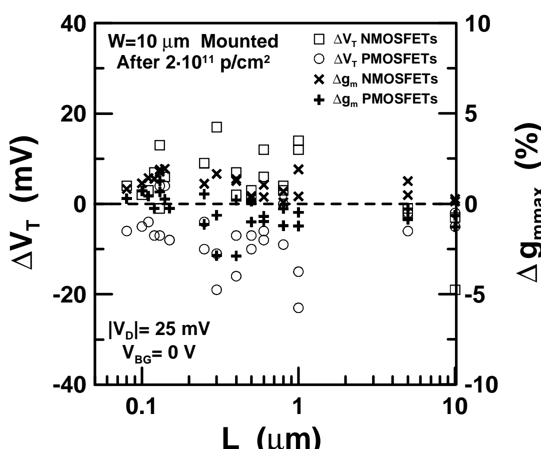

Fig. 5. Threshold voltage shift (ΔV_T) and maximum transconductance degradation (Δg_{mmax}) versus gate length (L) for mounted NMOSFETs and PMOSFETs after the two consecutive 10^{11} proton/cm^2 irradiations.

Regarding to the 2nd g_m peak, it was expected that after irradiation an increase of the recombination rate of the majority carriers could occur, what could have given rise to some decrease in the magnitude of the 2nd g_m peak. However, under the studied experimental conditions, no clear trend for the degradation of the 2nd g_m peak has been found on either, n- or p-channel transistors (fig. 6). At the same time, no clear shift on its V_{FG} position has been observed. This suggests that no significant change in majority carriers recombination lifetime was introduced by the irradiation, which is also supported by the results coming from the measurements of front gate switch-off I_D transients, which will be shown later.

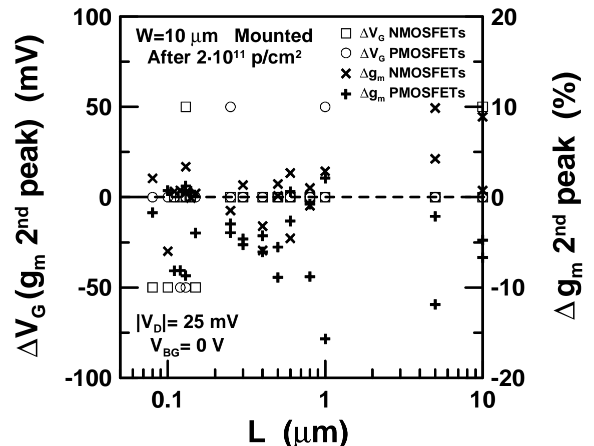

Fig. 6. Gate voltage shift (ΔV_G) and g_m degradation (Δg_m) corresponding to the 2nd g_m peak for W= 10 μm NMOSFETs and PMOSFETs with different L after the two consecutive 10^{11} proton/cm^2 irradiations.

B. On wafer devices (non-biased during irradiation)

Figures 7 and 8 show typical I_D and g_m versus V_{FG} characteristics measured at V_{BG}= 0 V for on wafer long channel (L=10 μm) NMOSFET and PMOSFET, respectively, before and after the two irradiation steps. In this case of devices non-biased during the irradiation, a significant increase of the subthreshold leakage current is also observed on the NMOSFETs after the first irradiation step. In this way, a radiation-induced hump in the I_D-V_{FG} characteristics is appreciated for V_{FG} between –0.5 V and 0 V (fig. 7).

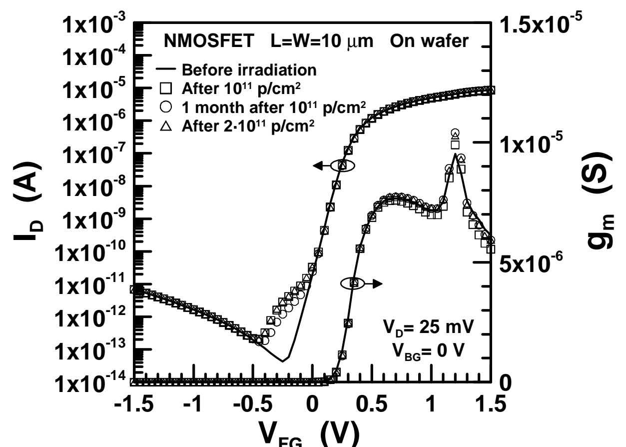

Fig. 7. I_D and g_m vs. V_{FG} curves measured at V_{BG}=0V for an on wafer NMOSFET before and after the two consecutive 10^{11}p/cm^2 irradiations.

As for the mounted devices, no appreciable degradation is observed for PMOSFETs (fig. 8) or for the above V_T portion

of all the characteristics, being in agreement with capacitance-voltage and current-voltage measurements performed on MOS capacitors fabricated with a similar CMOS process but on a bulk wafer (figs 9 and 10). As expected for this ultra-thin oxide, no appreciable changes were observed for the front gate oxide characteristics. Moreover, no radiation-induced I_D subthreshold leakage was observed on the similar MOSFETs processed on the bulk wafer.

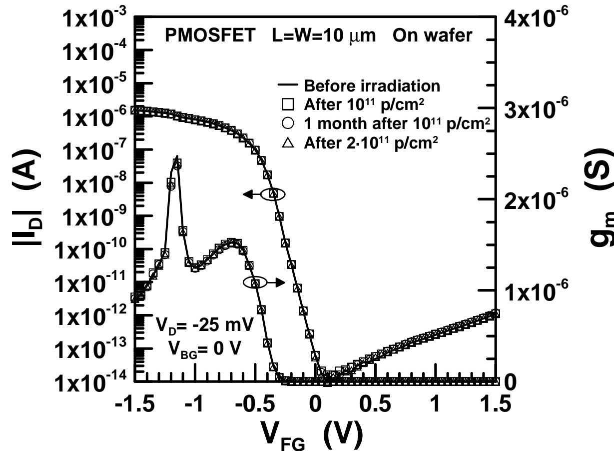

Fig. 8. I_D and g_m vs. V_{FG} curves measured at V_{BG}=0V for an on wafer PMOSFET before and after the two consecutive 10^{11}p/cm^2 irradiations.

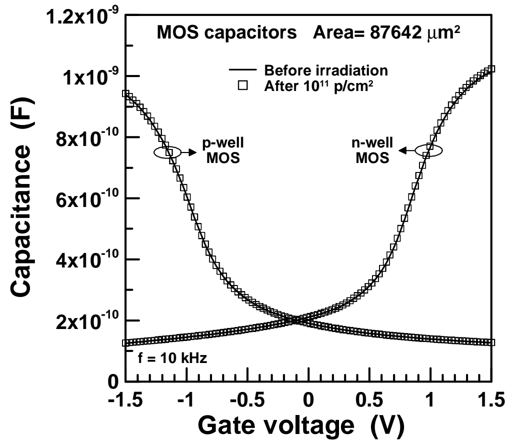

Fig. 9. Capacitance-voltage characteristics measured for p- and n-well MOS rectangular capacitors before and after 10^{11} proton/cm^2 irradiation.

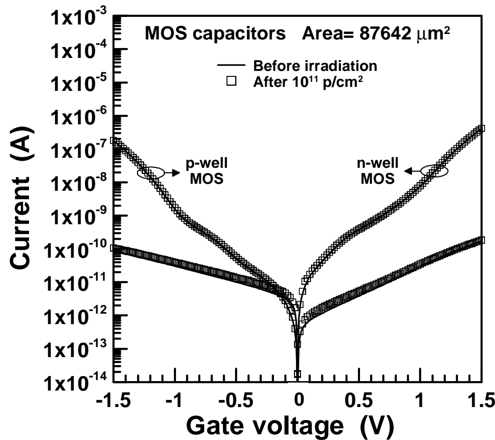

Fig. 10. Current-voltage characteristics measured for p- and n-well MOS rectangular capacitors before and after 10^{11} proton/cm^2 irradiation.

IV. Impact of V_{BG} on Irradiated Devices

In order to investigate the origin of the observed degradation in the n-channel transistors, post-irradiation measurements were performed applying different back gate biases. Figure 11 shows I_D-V_{FG} characteristics for an irradiated NMOSFET measured at V_{BG} values ranging from 0 V to –20 V. From the figure, a clear progressive reduction of the I_D subthreshold leakage is observed for V_{BG} values between 0 and –7 V. Moreover, the measurements at V_{BG}= -8 V or more negative V_{BG} are found to fit with the characteristics before irradiation.

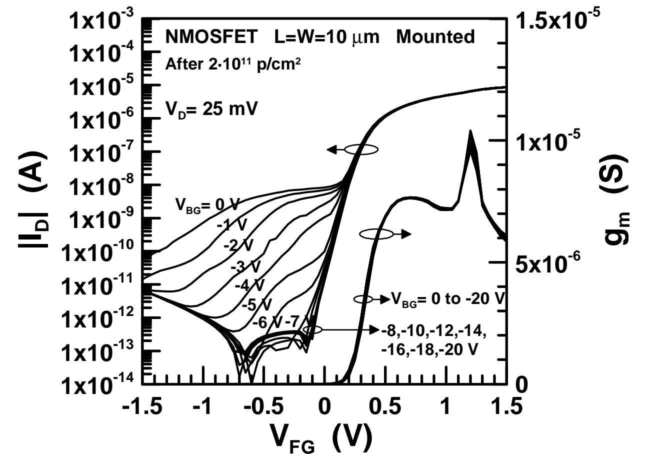

Fig. 11. I_D and g_m versus V_{FG} characteristics measured at different negative V_{BG} voltages for an L=W= 10 µm mounted NMOSFET after the two consecutive 10^{11} proton/cm^2 irradiations.

Following this trend for the radiation-induced degradation as a function of V_{BG}, fig. 12 shows I_D versus V_{FG} characteristics measured at V_{BG}=0 V for irradiated n-channel transistors with L ranging from 10 µm to 0.10 µm. From the figure, the presence of I_D subthreshold leakage is observed for all L values, with no clear length dependence. On the other hand, when a strong enough negative V_{BG} is applied, no parasitic current is observed and the I_D versus V_{FG} characteristics are found to fit with before irradiation curves.

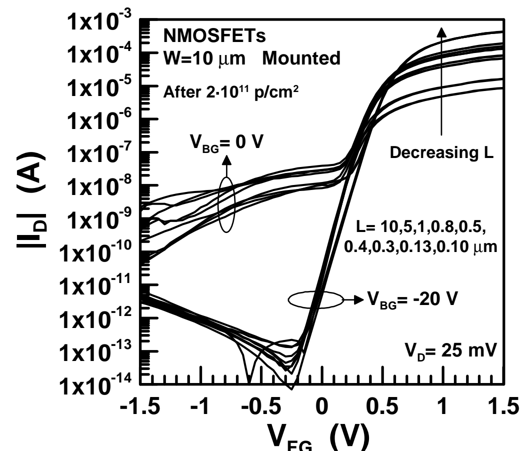

Fig. 12. I_D versus V_{FG} characteristics measured at V_{BG}= 0 V and –20 V for mounted NMOSFETs with different gate lengths (L) after the two consecutive 10^{11} proton/cm^2 irradiations.

V. IMPACT OF V_{BG} ON NON-IRRADIATED DEVICES

In order to investigate the impact of V_{BG} on non-irradiated NMOSFETs characteristics, I_D-V_{FG} curves were measured at different V_{BG} values ranging from –20 to 20 V. The results corresponding to an L= 10 μm n-channel transistor are shown in fig. 13. From the figure, the formation of a subthreshold leakage hump starts to be appreciable for V_{BG} values around 3 V, and this parasitic conduction increases for higher positive V_{BG} voltages. On the other hand, no changes are observed when the back gate is biased in accumulation (V_{BG}<0). Regarding to the portion of the characteristics above V_T, no significant changes are observed on V_T and g_{mmax} when applying the different V_{BG} in the range from –20 V to 20 V.

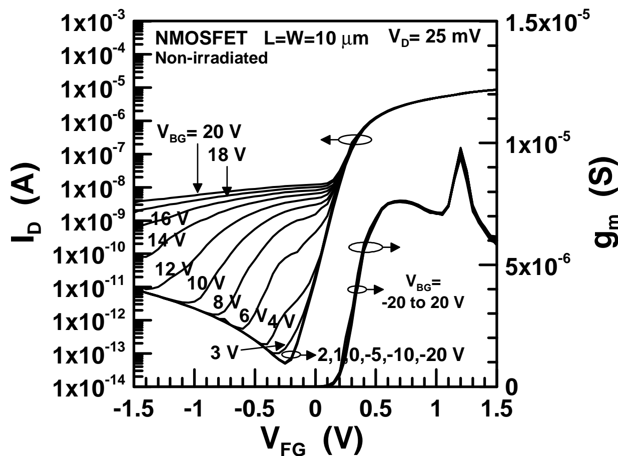

Fig. 13. I_D and g_m versus V_{FG} characteristics measured at different positive and negative V_{BG} for a non-irradiated L=W= 10 μm NMOSFET.

From figs 11 and 13 results, a strong similarity is found between I_D characteristics of irradiated NMOSFETs measured at V_{BG}=0 V and non-irradiated ones measured at positive enough V_{BG}. In this way, figs 14 and 15 show, the comparison between I_D versus V_{FG} characteristics measured for a mounted and an on wafer irradiated transistors measured at V_{BG}= 0 V, as well as non-irradiated ones measured at V_{BG}= 14 V and 4.5 V, respectively. From the figures, the similarities are evident.

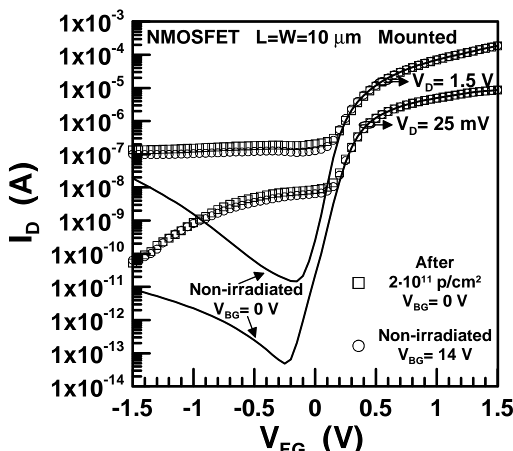

Fig. 14. I_D versus V_{FG} curves measured at V_{BG}= 0 V for an irradiated mounted NMOSFET (after the two consecutive 10^{11} proton/cm^2 irradiations) and for a non-irradiated one measured at V_{BG}= 0 V and 14 V.

Furthermore, in agreement with the irradiation results, the generation of an irradiation-like back channel parasitic conduction by applying a positive bias to the back gate is not found to affect neither the magnitude nor the position of the EVB-induced 2nd peak of g_m.

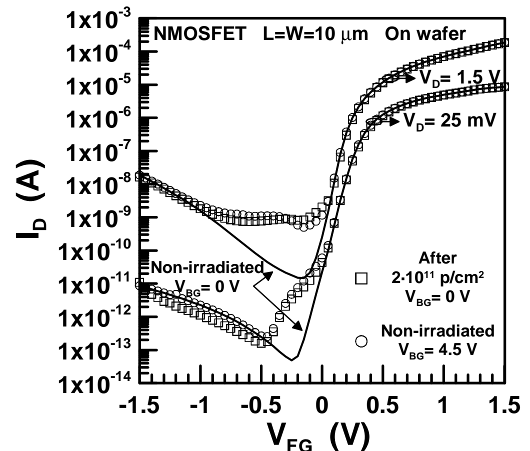

Fig. 15. I_D versus V_{FG} curves measured at V_{BG}= 0 V for an irradiated on wafer NMOSFET (after the two consecutive 10^{11} proton/cm^2 irradiations) and for a non-irradiated one measured at V_{BG}= 0 V and 4.5 V.

VI. BACK CHANNEL LEAKAGE AND TRAPPED CHARGES

In order to investigate the existence of a back gate threshold voltage shift (ΔV_{TBG}) responsible for the inversion of the back channel in the irradiated NMOSFETs measured at V_{BG}= 0 V, back channel characteristics were measured for irradiated and non-irradiated NMOSFETs. Figure 16 gives evidence for the existence of a radiation-induced negative ΔV_{TBG} of about 14 V and 4.5 V for mounted and on wafer devices, respectively. In fact, in the two previous sections this has been shown to be responsible for the observed subthreshold degradation of the front gate I_D characteristics.

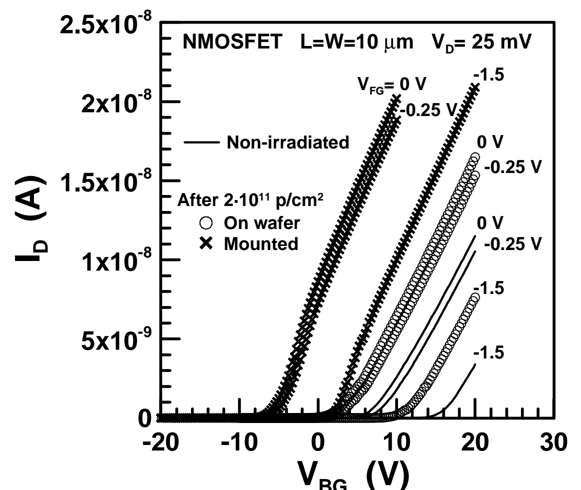

Fig. 16. Comparison between back channel characteristics (I_D versus V_{BG}) measured for an irradiated mounted and on wafer NMOSFETs (after the two consecutive 10^{11} proton/cm^2 irradiations), together with a non-irradiated one, measured for three different V_{FG} bias conditions.

Neglecting any possible interface state generation, and assuming a radiation-induced uniform effective density of positive trapped charges placed in the buried oxide and near the film interface (N_{OXBG}), following equation (1), a value of about $7.5\cdot10^{11}$ charges/cm^2 is estimated for N_{OXBG} corresponding to the mounted devices.

$$\Delta V_{TBG} \approx 14\ \mathrm{V} = \frac{\Delta N_{OXBG}}{C_{OXBG}} \ \Rightarrow\ \Delta N_{OXBG} \approx 7.5\cdot10^{11}\ \mathrm{cm^{-2}} \quad (1)$$

$$\text{with } C_{OXBG} = \frac{\varepsilon_{BOX}}{T_{BOX}} = \frac{3.9\cdot 8.85\cdot10^{-14}\ \mathrm{F/cm}}{400\cdot10^{-7}\ \mathrm{cm}}$$

The presence of these effective positive charges in the irradiated devices can explain the parasitic conduction associated with the inversion of the back channel or its edges with the field isolation (fig. 17).

The results on non-biased chips point out to a N_{OXBG} value about three times smaller for these devices irradiated without applying any bias. This difference could be explained by a different electric field distribution existing in the buried oxide between the two conditions. In this way, for the two cases, an electric field pushing the radiation-generated holes (ionization) in the buried oxide towards the film interface can be expected. However, whereas in the non-biased case this field would be only determined by the build-in potential between the p-type silicon film and the lower doped p-type silicon substrate (underneath the buried oxide), the potential drop existing between the n-type source and drain contacts and the p-type film should be added for the case of the devices irradiated under bias [17,18].

In order to distinguish between parasitic conduction due to the inversion of the back channel or mainly concentrated in its edges with the PELOX field isolation [19,20], the I_D subthreshold leakage dependence on gate width was investigated. Figure 18 shows that the magnitude of the I_D leakage hump (@V_{FG}=-0.25 V) (fig. 7) for irradiated on wafer NMOSFETs (measured at V_{BG}= 0 V) is found to increase when reducing W from 10 μm to around 1 μm. However, for narrower W an important decrease of the leakage current is found, so that no radiation-induced subthreshold hump can be appreciated in W= 0.4 μm on wafer irradiated NMOSFETs. These results are found to be in good agreement with the ones extracted from non-irradiated devices with different W measured at V_{BG}= 4.5 V, which are also shown in fig. 18.

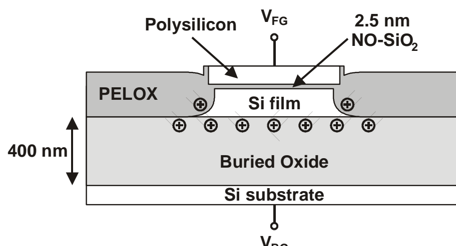

Fig. 17. Sketch of a PD SOI MOSFET showing radiation-induced positive charge trapping in the buried and field (PELOX) oxides.

The gate width dependence of the I_D subthreshold hump results in fig. 18 can be explained by the W-dependence of the back gate threshold voltage (V_{TBG}) for the transistors of this technology (also shown in fig. 18). In this way, while a small decrease in V_{TBG} is appreciated when reducing W from 10 μm to around 0.7 μm, a significant increase of V_{TBG} is observed in the narrower devices.

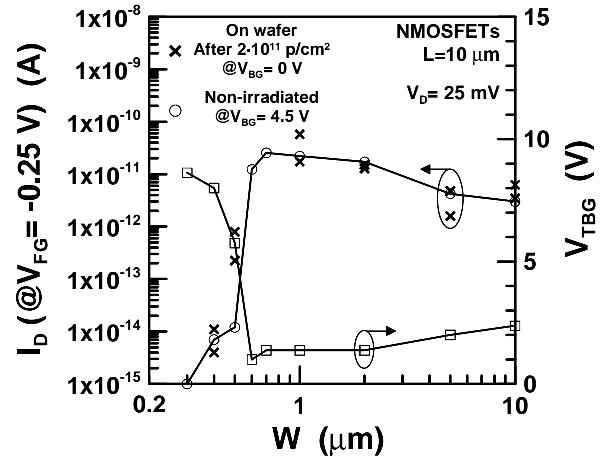

Fig. 18. Comparison between the radiation-induced I_D subthreshold hump (I_D @V_{FG}= -0.25 V) measured at V_{BG}= 0 V for on wafer NMOSFETs with different gate widths (W) after the two consecutive 10^{11} proton/cm^2 irradiations and non-irradiated devices measured at V_{BG}= 4.5 V. There are also shown the back gate threshold voltages (V_{TBG}) as a function of W for non-irradiated devices measured at V_{FG}= -0.25 V.

In order to better analyze the origin of the observed parasitic conduction, I_D-V_{BG} curves up to high V_{BG} were measured. In this way, fig. 19 results show the switch-on of an additional back channel conduction path for V_{BG} voltages around 80 V. This additional conduction is found to be dependent on W and it is attributed to the creation of the inversion back channel layer. In this way, the conduction observed for V_{BG} voltages up to around 80 V, which is no dependent on W, is mainly attributed to a parasitic conduction along the edges between the buried oxide and the PELOX field isolation (fig. 17) [13,21].

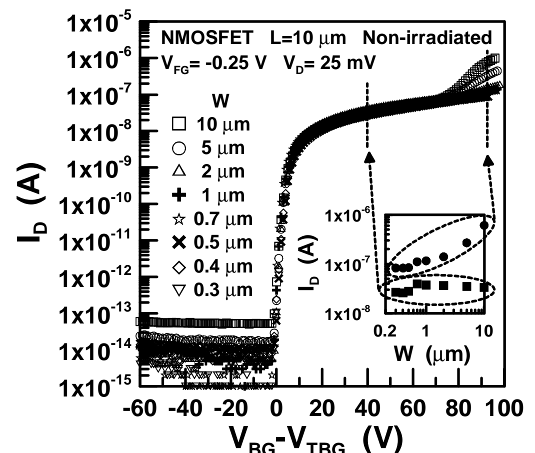

Fig. 19. I_D versus V_{BG}-V_{TBG} characteristics measured at V_{FG}= -0.25 V for non-irradiated L= 10 μm NMOSFETs with different gate width (W). In the inset, it is shown the I_D dependence on W at V_{BG}-V_{TBG}= 40 V and 90 V.

VII. IMPACT OF RADIATION ON SWITCH-OFF ID TRANSIENTS

After switching "on" or "off" the front gate of a PD SOI MOSFET, there is no substrate current to quickly adjust the film majority carrier density and the equilibrium depletion width has to be reached through generation and recombination processes. Since early times, it is known that I_D transients are observed under these conditions and their potential impact on circuit performance has been a matter of concern [4]. Originating from generation and recombination processes, I_D transients are known to be a valuable tool for assessing the quality of the starting material and the process-induced or radiation-induced defects. Different techniques have been proposed to extract the generation or recombination lifetimes from "switch-off" or "switch-on" I_D transients, respectively [22,23].

Usually, a rather large area transistor is used, operating in the ohmic regime. In the switch-off experiments shown in figs 20 and 21, $|V_{FG\ on}|$ is taken above V_T, whereas $|V_{FG\ off}|$ is taken in the subthreshold regime. After switching-off the devices from $|V_{FG\ on}|$= 0.7 V to $|V_{FG\ off}|$= 0.1, an increase of the drain current $I_D(t)$ is observed for several tens of seconds until the steady state value $I_D(t=\infty)$ is reached.

It has been shown that for a fixed temperature the measured I_D transient time T_0 (defined at 90% of $I_D(t=\infty)$) can be used to extract the film generation lifetime (τ_g) of PD-SOI MOSFETs, by means of an approximated linear relationship [23]:

$$\tau_g \approx \frac{T_0}{K} \tag{2}$$

with K a technology and temperature dependent factor [23]. Using this procedure, a τ_g in the range of 0.2 µs has been extracted for the devices under study in this work [24].

In the past, similar transient techniques were applied to irradiated transistors to study the impact on the bulk and surface generation or recombination lifetimes [25,26]. As can be seen from fig. 20 results with $V_{FG\ on}$= 0.7 V, the switch-off transients of the NMOSFETs become much faster after irradiation [24], which could point to a radiation-induced reduction of τ_g. However, in this case, the reduction in transient time is not attributed to a reduction of the film τ_g, but rather associated with the radiation-induced increase of the subthreshold leakage studied in the previous sections. This is supported by the fact that the transients measured on non-irradiated NMOSFETs at V_{BG}= 14 V are found to fit very well with those corresponding to the irradiated devices measured with V_{BG}= 0 V. Furthermore, as shown in fig. 21, the transients measured on the p-channel devices, with no radiation-induced leakage, do not show any significant change after irradiation.

An interesting feature associated with the EVB tunneling phenomenon giving rise to the second peak in g_m is the fact that the switch-off transients are found to change their shape from undershoot to overshoot when $V_{FG\ on}$ is above the V_{FG} threshold for EVB tunneling ($|V_{FG\ on}|$= 1.5 V data in figs 20 and 21)). In fact, this probes the injection of majority carriers into the substrate [5,6], which have to disappear after switching off the device. The shape of these transients has been found to fit well with conventional (EVB-free) switch-on type transients [27], which enable the extraction of the majority carrier recombination lifetime [22].

As shown in fig. 20, irradiation also speeds up this hole removal in the n-channel devices, which is again associated with the subthreshold leakage conduction.

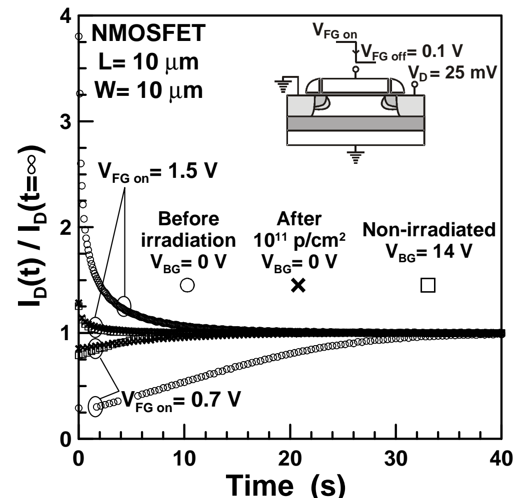

Fig. 20. Normalized switch-off I_D transients measured on a mounted L=W=10µm NMOSFET before and after 10^{11} p/cm^2 irradiation, together with the results obtained for a non-irradiated one measured at V_{BG}= 14 V.

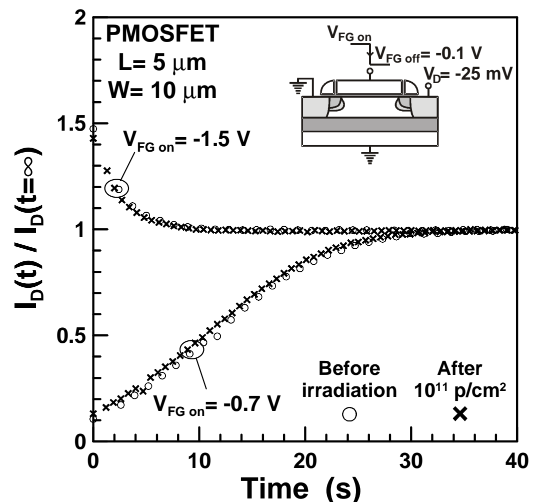

Fig. 21. Normalized switch-off I_D transients measured on a mounted L=W= 10 µm PMOSFET before and after 10^{11} p/cm^2 irradiation.

VIII. CONCLUSIONS

The degradation of 0.10 µm-CMOS PD SOI MOSFETs subjected to 60 MeV proton irradiation has been analyzed. A radiation-induced increase of the leakage current in the subthreshold region of the NMOSFETs characteristics has been observed, which is more important in the case of devices irradiated under bias. By studying the static and transient characteristics on devices with different geometries and bias conditions, the degradation is demonstrated to be originated

by positive charge trapping in the buried oxide, being responsible for an edge parasitic back channel conduction. The effective density of trapped holes is estimated to be around $7.5\cdot10^{11}$ charges/cm^2 for the devices biased during the irradiation, whereas this is found to be about three times smaller in the case of the non-biased ones.

Under the studied experimental conditions, no significant changes have been observed in the above threshold region of the characteristics. Furthermore, the irradiation is not found to significantly change neither the magnitude nor the position of the Electron Valence Band gate tunneling-induced 2nd peak of the transconductance, characteristic of these ultrathin gate oxide PD SOI transistors. This is also in agreement with the results obtained from non-irradiated devices measured at positive back gate voltages, what has been found to generate an irradiation-like parasitic back channel conduction. It has been also derived that no significant changes in the majority carriers generation and recombination lifetimes are introduced by the irradiation, which is supported by the results from front gate switch-off I_D transients.

Although for the studied experimental conditions the leakage current does not affect the above-threshold region of the characteristics, some technology or device architecture radiation-hardening actions could be needed for future advanced SOI generations [15].

IX. Acknowledgments

Hans van Meer and Kristin De Meyer are warmly thanked for providing the devices and the relevant process information. Guy Berger and his colleagues of Centre de Recherches du Cyclotron, Louvain-la-Neuve, Belgium, are gratefully acknowledged for their assistance during the 60 MeV proton irradiations.

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