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G.4 *Improving the Sensitivity of PMOS Dosimeters Using Dual Dielectrics*

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Accroissement de la sensibilité de dosimètres PMOS par l'emploi de double diélectriques

Des oxydes et des nitrures, réalisés par dépot CVD, ont été utilisés comme seconde couche sur un oxyde thermique de RADFET. Plus de trente combinaisons ont été fabriquées et testées sous irradiation. La combinaison 600 nm d'oxyde TEOS/CVD sur 400 nm d'oxyde thermique présente une sensibilité de 7,54 mV/rad (V_{IR} = +5 V, 5 krads), ainsi qu'un bon comportement dans d'autres zones dosimétriques.

I Introduction

PMOS dosimeters, or RADFETs [1], are specially designed MOSFETs which allow radiation dose to be measured due to a radiation-induced change in their electrical characteristics. Hitherto used for space applications, where large doses are monitored successfully, it is the objective to use RADFETs in low dose clinical and personnel environments, because of their advantages of size and cost. The use of novel dual dielectrics in the critical gate oxide region is explored. This involves study of a number of CVD (Chemical Vapour Deposition) oxides [2], [3] and PECVD nitride as extra layers deposited on thermally grown oxides. A CVD oxide of 1μm thickness can be deposited in less than a minute, compared to several hours for a thermal oxide. This work gives a comprehensive overview of the radiation characteristics of various thermal oxide - CVD dielectric combinations.

II Experiment

This work examines three types of dual dielectric devices: (a) thermal oxide + TEOS CVD oxide, (b) thermal oxide + Silane CVD oxide and (c) thermal oxide + PECVD nitride. All dual dielectric gate structures were fabricated by an optimised thermal oxidation (0.4μm or 1μm) followed by deposition of the CVD layer. A V_T adjust implant was given to some wafers, with the dual aim of adjusting the threshold voltage towards zero and improving the radiation sensitivity of the devices. The CVD oxide layer devices were annealed for 30 mins at 1000°C in O_2, those using nitride were annealed for 30 mins at 1000°C in N_2. Al/1%Si 1μm thickness was used for all electrodes.

Irradiations were carried out using the Co60 source at ESTEC. Devices were irradiated to a total dose of 10krads with a bias of either 0V or +/-5V (Irradiation Electric Field Eir = +/-0.125MV/cm for 400nm gate oxide) applied to the gate, dose rates 50 rads(H_2O)/min. Measurements were taken immediately post-irradiation to determine the radiation-induced threshold voltage V_T shift, which is a measure of radiation sensitivity (V_T=Vo measured using Reader circuit configuration [4]) and also the read-time drift [4]. The fading of the threshold voltage after the final irradiation was monitored for a two-month period.

III Results

(i) Radiation Sensitivity

Figure 1 illustrates that adding TEOS CVD layers of increasing thickness can greatly enhance the sensitivity of a 400nm thermal oxide for CVD thickness > 1000Å, which indicates substantial electron trapping at the thermal/CVD interface, which is counteracted by increasing TEOS thickness. This combination gives the greatest radiation sensitivity. The effect of increasing CVD Silane and Nitride layer thicknesses is that radiation sensitivity does not continue to increase. It is the 400nm ox. + 300nm Silane, 400nm ox. + 100nm Nitride combinations that are the most sensitive. Beyond these thicknesses, the overall charge contribution of the CVD is negative.

Positive irradiation bias V_{IR} results in an increase in radiation sensitivity for all combinations over the single thermal oxide device. For V_{IR}=-5V, the sensitivities increase for all dielectrics over the unbiased case, see Figure 3 for TEOS, due to less geminate recombination [5]. The V_{IR}=-5V curve shows saturation at relatively lower doses due to the build-up of a zero field region. The response to V_{IR} variation of the oxide + nitride dielectrics is similar to that of the Silane equivalents.

The V_T implant was through the thermal oxide only. Results show a large increase (Figure 4) for the 400nm thermal oxide + 100nm TEOS sensitivity.

(ii) Read-time Drift.
It is found that the combinations involving the TEOS oxide give the lowest drift levels. The Silane combinations on average give the highest drift levels while the nitride combinations exhibit 'negative drift' or decrease in Vo at larger dielectric thicknesses.

(iii) Long-term Fading
Thicker TEOS layers on a 400nm thermal oxide exhibit the best (lowest) post-irradiation fading behaviour, which is significant given their excellent sensitivities. Improved device sensitivity results in reduced %fading. In Figure 5, for the Nitride combination, V_T continues to increase for some days post-irradiation until a gradual annealing process begins. This is thought to be due to slow interface states [2].

IV Summary/Discussion

The radiation performance of the three different types of dual dielectric is quite different.
Radiation sensitivity, which is the most important criterion, of the thermal oxide/TEOS dielectric RADFETs behaves similarly to a thermal gate oxide device; increasing sensitivity for increasing dielectric thickness. The use of nitride and Silane layers in the dielectrics lead to a situation where a 'critical thickness' is reached, beyond which there is a decrease in radiation sensitivity. This can be explained by charge mechanisms in the bulk CVD, interface and due to stress. Figure 6 proposes a model which separates the contributions to charge due to the different dielectric layers and interfaces based on measured results.
Another encouraging aspect of the Thermal/TEOS devices is the excellent drift and fading responses (0.02% drift and 1.85% fading for the implanted device for V_{IR}=+5V). The single 1µm TEOS gate devices suffered from high drift levels. The more promising Thermal/TEOS gate dielectric combination is being optimised in NMRC at present.

References

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