C. Conneely, B. O'Connell, W. Lane – NMRC, Cork, IE
L. Adams – ESA/ESTEC, Noordwijk, NL

Stratégies pour atteindre des sensibilités au millirad avec des dosimètres PMOS

Nos travaux antérieurs ont montré la possibilité d'accroître la sensibilité des dosimètres PMOS par conception. Ils sont poursuivis par l'extension de la chaîne de composants. Avant celle-ci, l'analyse du bruit et des effets thermiques a été réalisée. Le besoin d'une compensation thermique devient impératif pour améliorer le rapport signal sur bruit.

Abstract

Previous work [1] at this centre has shown enhanced sensitivity for PMOS dosimeters using a design approach. This is being extended presently to longer chains of devices. Prior to this extension, thermal effects have been investigated and a noise analysis has been undertaken. The need for a temperature compensation technique becomes imperative if the signal/noise ratio is to be improved.

Introduction/ Experimental

The PMOS dosimeter or RADFET [2] is the basis of this work where the change in threshold voltage ΔV_T is the dosimetric parameter.The devices used in this investigation derive from the optimised NMRC RADFET process which is a single well technology. Typically an implant has been used to adjust the native V_T (V_{T0}) to ~ -1 volt; recently the use of depletion devices i.e. devices with a $V_T > 0$ volts has been investigated, these devices allow a greater operating range but require a separate bulk connection to bias the devices into enhancement (Fig. 1). Two thicknesses of thermal gate oxide RADFETS are tested, a 4kÅ and a 9.2kÅ. The 4kÅ device has an adjusted V_T of ~ +1.5 volts and the 9.2kÅ device has an adjusted V_T of ~ +6.0 volts. In both cases a device geometry W/L of 425/17 applies.

A. Noise Analysis

The short term noise of a MOSFET is characterised by a limitation due to flicker or 1/f noise. An experimental setup to measure this contribution has been assembled, Fig. 1B. which shows a Dynamic Signal Analyser fed by a Nanovolt pre-amplifier with fixed gain of 1000 and ac-coupled input. This system has a -3dB bandwidth from ~1 Hz to 1MHz.

The source of the 1/f noise in MOS transistors is defects in the oxide (probably oxygen vacancies), lying close to the Si/SiO2 interface [3-5]. Since these defects are precursors to radiation induced hole traps (that we rely on for high sensitivity to radiation), it seems unlikely that we can reduce this noise component without reducing dosimetric sensitivity. The measured 1/f noise agrees with the HSPICE model for 1/f noise. The relevant term is S_v = Noise spectral density (V^2 /Hz). The values scale with stack length as shown in Fig. 2 & Table 1.

Table 1:

Length of stack	HSPICE Noise Model V^2/Hz @ 100Hz	Measured V^2/Hz @ 100Hz	HSPICE Noise Model V^2/Hz @ 1kHz	Measured V^2/Hz @ 1kHz
1	11.92e-12	10.2e-12	1.19e-12	1.23e-12
2	27.40e-12	22.5e-12	2.74e-12	2.82e-12
4	65.90e-12	70.5e-12	6.59e-12	8.00e-12
8	191.3e-12	187.0e-12	19.1e-12	30.0e-12

B. Thermal Analysis

Using the circuit shown in Fig.1 where chains of depletion PMOS devices are biased into enhancement using a reverse bulkbias and a -10 µA saturation current, the change in V_0, output voltage is measured over the range 0 - 100 °C. The results are plotted in Fig. 3 & 4, where the V_T shift with temperature in mV/°C known as the Threshold Voltage Temperature Coefficient, TVTC is plotted versus V_{BS} and stack length. There appears to be a Zero TVTC, or ZTC point at the intersection of 1,2,4 and 8 devices also for increasing V_{BS} the TVTC approaches zero and then turns positive.

This data illustrates the very large shifts of V_T with temperature. Fig. 5 is an implementation of a temperature

compensation circuit utilising V_T matched RADFETS. The voltage output was taken over an 18 hour period. Over this period, results show a long term drift of 1 mV rms over a 10 °C range. There was a short term noise component also, of magnitude ~200 μV rms which suggests that an on chip configuration may be required to minimise external noise sources. However by controlling temperature to within +/- 0.3 °C a long term drift of < 200 μV should be possible, at this point the short term noise becomes dominant.

Summary/Conclusions

1/f noise on PMOS dosimeters has been examined and its scaling with stack length noted. Its manifestation as the major component of the short term noise from the circuit of Fig. 5 indicates that under conditions of tight temperature control it can be the dominant contributor to noise. The need for temperature compensation has been demonstrated, some methods for minimising thermal drift including operation close to the ZTC point and application of a high bulk bias have been discussed, a circuit arrangement allowing these effects to be minimised has been built and the results obtained show a significant reduction in drift over uncompensated devices.

References

[1] B. O'Connell, A. Kelleher et. al. "Stacked RADFETs for Increased Radiation Sensitivity", IEEE Trans. Nuc. Sci., vol.43, no.3, pp 985-990, June 96

[2] A.G. Holmes-Siedle, "The Space Charge Dosimeter - General Principles of a New Method of Radiation Dosimetry", Nucl. Instrum. Methods, vol. 121, p. 169, 1974.

[3]T.L. Meisenheimer and D.M. Fleetwood "Effect of radiation induced charge on 1/f noise in MOS devices."IEEE Trans.Nuc. Sci. NS-37, No. 6,Dec. 1990

[4] D. M. Fleetwood and J.H.Scofield "Evidence that similar point defects cause 1/f noise and radiation induced hole trapping in MOS transistors." Physical Review Vol.64, No. 5,1990

[5]T.L Meisenheimer, D.M. Fleetwood et. al."1/f noise in N and P- channel MOS devices through radiation and annealing." IEEE Trans. Nuc. Sci. Vol. 38, No. 6, 1991.