Abstract
Previous work [1] at this centre has shown enhanced sensitivity for PMOS dosimeters using a design approach. This is being extended presently to longer chains of devices. Prior to this extension, thermal effects have been investigated and a noise analysis has been undertaken. The need for a temperature compensation technique becomes imperative if the signal/noise ratio is to be improved.

Introduction/Experimental
The PMOS dosimeter or RADFET [2] is the basis of this work where the change in threshold voltage $\Delta V_T$ is the dosimetric parameter. The devices used in this investigation derive from the optimised NMRC RADFET process which is a single well technology. Typically an implant has been used to adjust the native $V_T (V_{T0})$ to $\sim$ -1 volt; recently the use of depletion devices i.e. devices with a $V_T > 0$ volts has been investigated, these devices allow a greater operating range but require a separate bulk connection to bias the devices into enhancement (Fig. 1). Two thicknesses of thermal gate oxide RADFETS are tested, a 4$k\AA$ and a 9.2$k\AA$. The 4$k\AA$ device has an adjusted $V_T$ of $\sim$ +1.5 volts and the 9.2$k\AA$ device has an adjusted $V_T$ of $\sim$ +6.0 volts. In both cases a device geometry W/L of 425/17 applies.

A. Noise Analysis
The short term noise of a MOSFET is characterised by a limitation due to flicker or 1/f noise. An experimental setup to measure this contribution has been assembled, Fig. 1B, which shows a Dynamic Signal Analyser fed by a Nanovolt pre-amplifier with fixed gain of 1000 and ac-coupled input. This system has a -3dB bandwidth from $-1$ Hz to 1MHz.

The source of the 1/f noise in MOS transistors is defects in the oxide (probably oxygen vacancies), lying close to the Si/SiO2 interface [3-5]. Since these defects are precursors to radiation induced hole traps (that we rely on for high sensitivity to radiation), it seems unlikely that we can reduce this noise component without reducing dosimetric sensitivity. The measured 1/f noise agrees with the HSPICE model for 1/f noise. The relevant term is $S_v = \text{Noise spectral density (V}^2/\text{Hz})$. The values scale with stack length as shown in Fig. 2 & Table 1.

<table>
<thead>
<tr>
<th>Length of stack</th>
<th>HSPICE Noise Model $V^2$/Hz @ 100Hz</th>
<th>Measured $V^2$/Hz @ 100Hz</th>
<th>HSPICE Noise Model $V^2$/Hz @ 1kHz</th>
<th>Measured $V^2$/Hz @ 1kHz</th>
</tr>
</thead>
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<tr>
<td>1</td>
<td>11.92e-12</td>
<td>10.2e-12</td>
<td>1.19e-12</td>
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<tr>
<td>2</td>
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<tr>
<td>8</td>
<td>191.3e-12</td>
<td>187.0e-12</td>
<td>19.1e-12</td>
<td>30.0e-12</td>
</tr>
</tbody>
</table>

B. Thermal Analysis
Using the circuit shown in Fig.1 where chains of depletion PMOS devices are biased into enhancement using a reverse bulk bias and a -10 $\mu$A saturation current the change in $V_{Tb}$, output voltage is measured over the range 0 - 100 °C. The results are plotted in Fig. 3 & 4, where the $V_T$ shift with temperature in mV/°C known as the Threshold Voltage Temperature Coefficient. TVTC is plotted versus $V_{BS}$ and stack length. There appears to be a Zero TVTC, or ZTC point at the intersection of 1,2,4 and 8 devices also for increasing $V_{BS}$ the TVTC approaches zero and then turns positive.

This data illustrates the very large shifts of $V_T$ with temperature. Fig. 5 is an implementation of a temperature
compensation circuit utilising $V_T$ matched RADFETS. The voltage output was taken over an 18 hour period. Over this period, results show a long term drift of 1 mV rms over a 10 °C range. There was a short term noise component also, of magnitude ~200 µV rms which suggests that an on chip configuration may be required to minimise external noise sources. However by controlling temperature to within +/- 0.3 °C a long term drift of < 200 µV should be possible, at this point the short term noise becomes dominant.

Summary/Conclusions

1/f noise on PMOS dosimeters has been examined and its scaling with stack length noted. Its manifestation as the major component of the short term noise from the circuit of Fig. 5 indicates that under conditions of tight temperature control it can be the dominant contributor to noise. The need for temperature compensation has been demonstrated, some methods for minimising thermal drift including operation close to the ZTC point and application of a high bulk bias have been discussed, a circuit arrangement allowing these effects to be minimised has been built and the results obtained show a significant reduction in drift over uncompensated devices.

References