PROJECT
ESA_QCA0109TS_C

TITLE
Radiation Pre-Evaluation of Xilinx FPGA XQVR300

EUROPEAN SPACE AGENCY
CONTRACT REPORT

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SUMMARY

This report presents the results from Heavy Ion and 60-Cobalt tests of Xilinx *Virtex* FPGA XQVR300 manufactured by Xilinx in a 0.22µm technology.
Virtex XQVR300 is an SRAM-based FPGA, which allow for real-time reconfigurable computing. Reprogrammable logic would offer the benefit of on-orbit design changes. Earlier SEU testing [1] on this type of device has reported high sensitivity to heavy ions. Mitigation techniques of Single Event Upsets in Virtex devices as Triple Module Redundancy and Configuration Readback (bitstream repair) have been developed by Xilinx and tested in this work.

DOCUMENT CHANGE RECORD

Changes between issues are marked with a left-bar.

Issue	Date	Paragraphs affected	Change information
1	10 Aug 2001	All	New document

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1. INTRODUCTION

This report presents the results from Heavy Ion and 60-Cobalt tests of Xilinx *Virtex* FPGA XQVR300 manufactured by Xilinx in a 0.22µm technology.
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2. *Virtex* XQVR300 DETAILS

The Virtex FPGA is an SRAM based device fabricated on thin-epitaxial silicon wafers using the commercial mask set and the Xilinx 0.22µ CMOS process with 5 metal layers. SEU risks dominate in the use of this technology for most applications. In particular, the reprogrammable nature of the device presents a new sensitivity due to the configuration bitstream. The function of the device is determined when the bitstream is downloaded to the device. Changing the bitstream changes the design's function. While this provides the benefits of adaptability, it is also an upset risk. A device configuration upset may result in a functional upset. User logic can also upset in the same fashion as seen in fixed logic devices. These two upset domains are referred to as configuration upsets and user-logic upsets. Two features of the *Virtex* architecture can help overcome upset problems. The first is that the configuration bitstream can be read back from the part while in operation, allowing continuous monitoring for an upset in the configuration and the part supports partial reconfiguration, which allows for real-time SEU correction. Secondly, the high density and rich architecture allow resource redundancy to be economically implemented in order to filter out SEU effects.

3. TEST SAMPLES

All tests were performed on prototype devices delivered by Xilinx in a 240 pin plastic flat package. The samples used for Heavy Ion were delidded by etching the plastic from the topside down to the chip. Chip marking is shown below. Test samples for Total Dose tests, SN#36-39, were delivered in the same batch.

	Chip Markings	**Device Marking**
SN #32	XILINX	Top and bottom side blank
SN #34	C-Logo 1998 M-Logo XNK06A (All markings not visible)	

Following information of process description is taken from a Total dose report presented by Xilinx at MAPLD2000 [2]:

Material:	<1-0-0> 20ohm-cm p-type epitaxial layer on highly doped substrate
Gate Oxide:	SiO_2, nominal 45/65A
Gate Width:	0.25/0.35µM defined
Isolation:	Shallow Trench 7,500A nom
Foundry:	UMC Group
Operating voltage:	2.5V

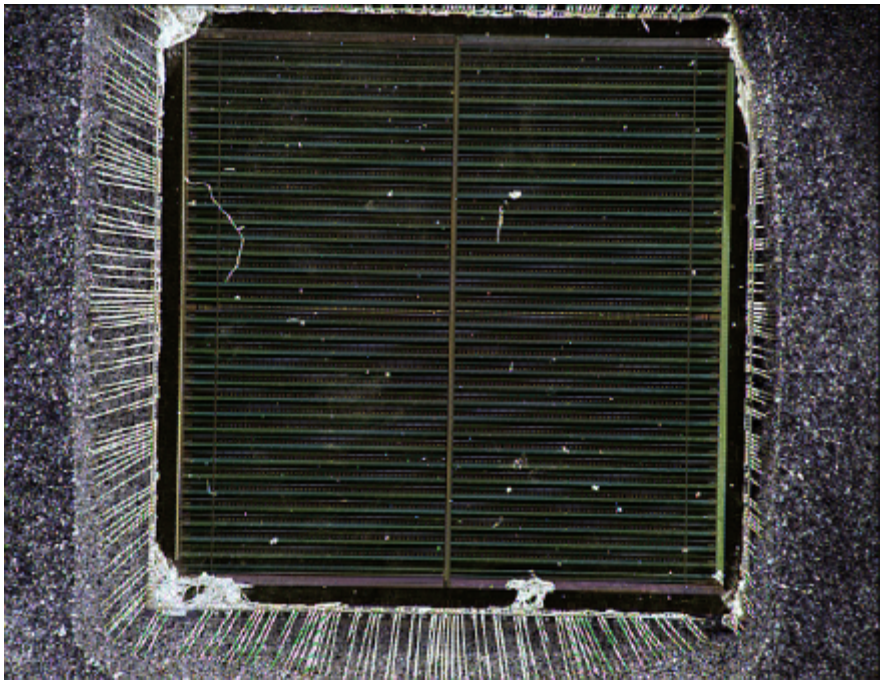

Figure 3.1 Overview of Virtex XQVR300 chip. Chip size is 11,2 x 11,2 mm.

3.1 DUT Design

Two different designs have been tested, named non-TMR and TMR. The non-TMR design was used for the total dose and the SEU test while the TMR design was used only for the SEU testing.

3.2 Non-TMR Design

For total dose tests a design was developed with two parts, one designed for functional test by the controller board and one designed for parameter measurements.

The part for functional test, shown in Fig. 3.2, implements into the Device Under Test (DUT) 14 pipelined shift register each 144 bit long and a small self-test circuit. Individual register bits are build up of a D-type CLB flip-flop modules [3]. All together, 32% of the available CLB flip-flop resources in the Virtex device have been used.

The principal of the self test circuit, shown in Fig. 3.3, is that data are compared with itself and any mismatch is reported to an output (Error flag). Data are a 6-bit word taking two different paths in the design before comparison. One path goes through 6 I/O modules of the device and then back to the comparator. The other path goes directly to the comparator. The data are generated by a feed back flip-flop register from an external clock signal. This give toggling data with half the frequency of the clock signal.

One small part of the device has been designed for parameter testing. Twelve binning circuits are connected from inputs to outputs of the device. They are of three different types, four of each. One type (BUF) has 50 buffer cells in-line between in- and outputs, one type (INV) has 50 inverter cells in-line between in- and outputs and one type (DIR) is direct connected.

All user I/Os was selected in the design as LVTTL.

The non-TMR design is a standard design practice without any redundancies or circuits for SEU mitigation.

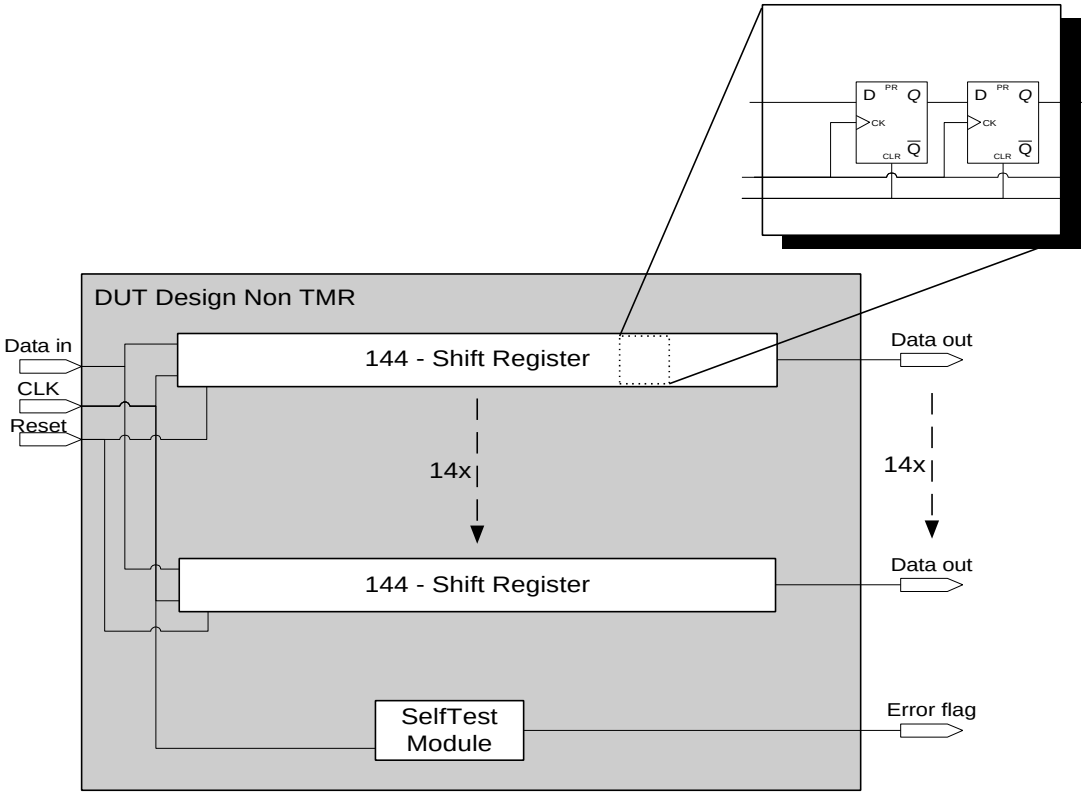

Figure 3.2 Principal Drawing of part used for functional test in the Non-TMR DUT Design.

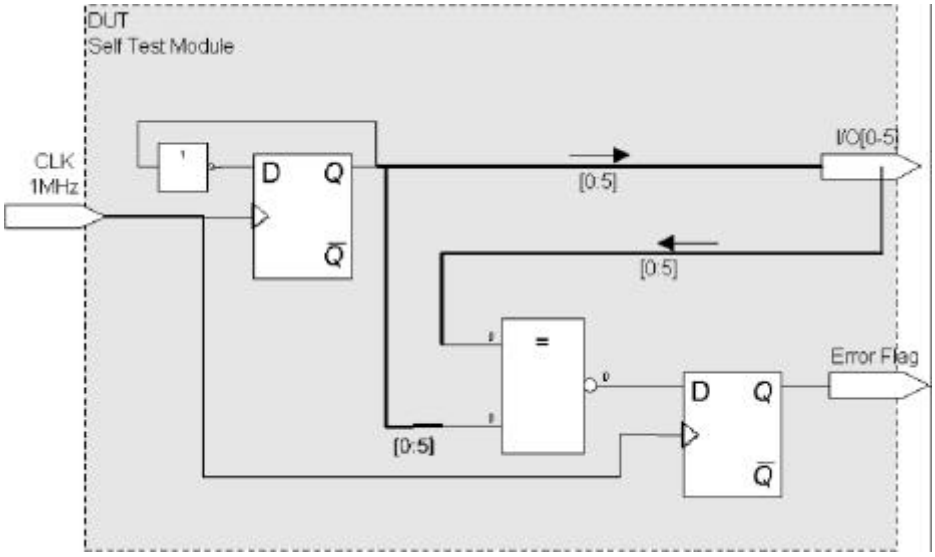

Figure 3.3 Principal Drawing of SelfTest Module

3.3 TMR Design

The TMR design, shown in Fig. 3.4, implements a functionally equivalent circuitry as the non-TMR design but with full internal triple redundancy. 95% of available FF-resources are used. The outputs of the TMR design use triple tri-state drivers to filter data errors from the output.

The TMR version uses the Triple Module Redundancy design techniques that Xilinx recommends for use with the Virtex FPGA. It use the same design rules as have been used in SEU tests performed at the Los Alamos National Laboratory [4].
The binning circuits in the non-TMR design are excluded since they fill no purpose for SEU testing.

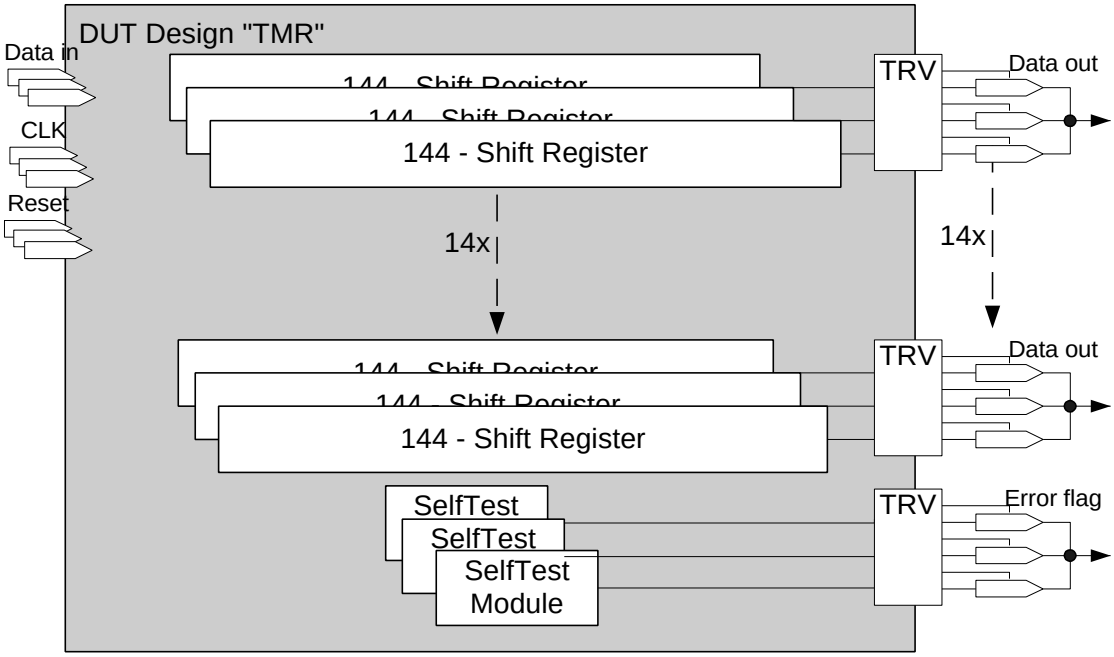

Figure 3.4 Principal Drawing of TMR DUT Design

4. TEST EQUIPMENT

At Saab Ericsson Space special test equipments have been developed for SEU- and Total Dose testing of FPGAs. In total dose tests, the DUTs are individually biased and supply current measurement and functional tests can be performed continuously.

4.1 General

The general concept is to load data into the DUT, pause for a pre-set time and thereafter read data and check for errors. New data are loaded into the DUT at the same time as old are read out. All this is repeated continuously during irradiation. With long pause time the DUT is tested in static condition and by setting the pause time to zero the DUT is tested in dynamic condition.

A flow chart of the test sequence is given in Fig. 4.1. Any detected errors will be stored in FIFOs, and the DUT will be loaded with new data again. The cycle will then be repeated. Failing read/write operations from/to the DUT will determine the functionality. The clock speed is variable up to 5 MHz. Error Data are serially transferred from the FIFO to a PC where data are analyzed. For each DUT, errors can be traced down to logic module, logic value and position.

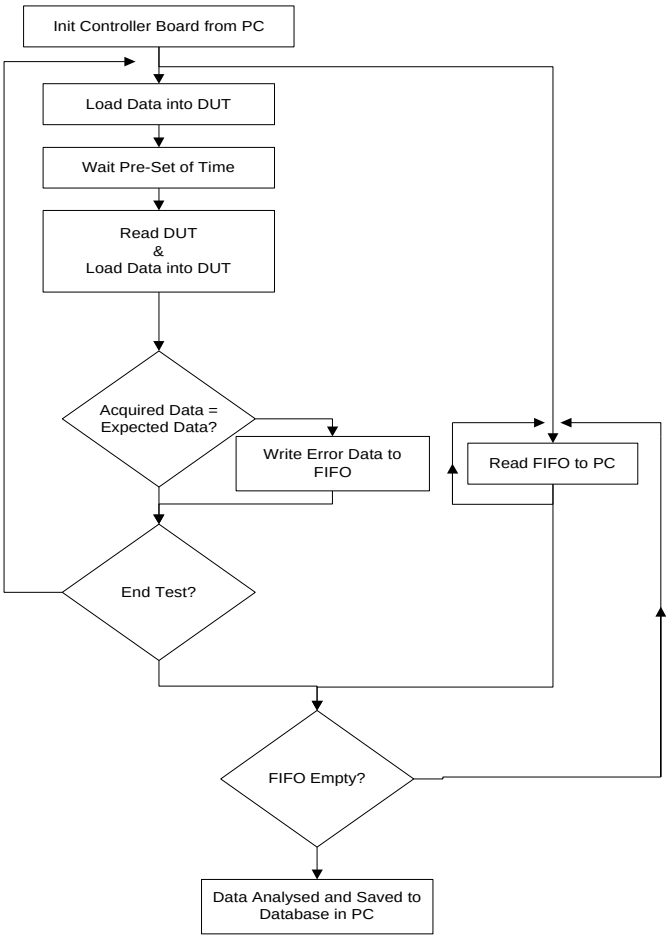

Figure 4.1 Flow chart of the test sequence.

4.2 Test Boards

The test system consist of two boards, one Controller board managing the test sequence and the serial interface to the PC and one DUT board housing two Devices Under Test (DUT). A principal drawing is given in Fig. 4.2.

The Controller board tests one DUT at a time using a "virtual golden chip" test method. The principal of the measuring technique is to compare each output from the DUT with the correct data stored in SRAM's. The general concept of the error detection and test sequence is shown in Fig. 4.1. The DUT is continually cycled while the outputs of selected ring counters are compared with the "golden chip". When an error is detected (when outputs do not match), the state of all outputs and position in cycle of the failing ring counter will be temporarily stored in FIFOs. Data in the FIFOs is continually send to a PC through a RS232 serial interface. After each test run the data are analyzed and stored in a database by the controlling PC.

The controller board also control the power supply for the DUTs by relays and send status signals to a Data Logger connected to the board.

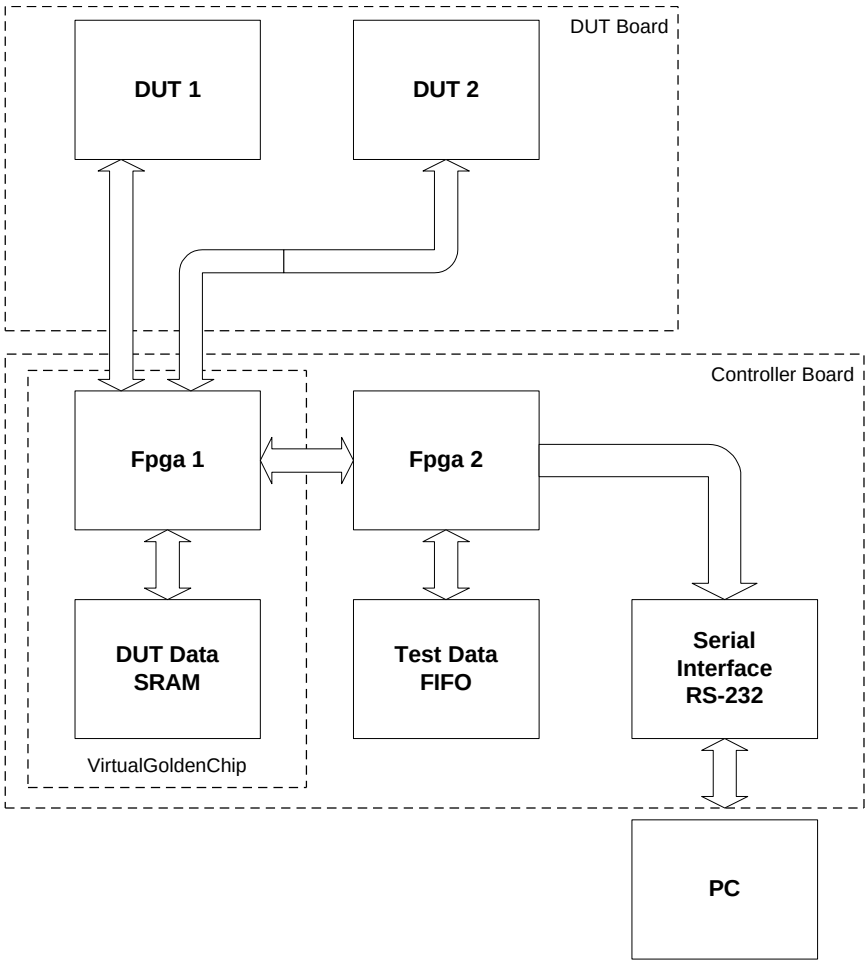

Figure 4.2 Principal drawing of DUT board and Controller Board

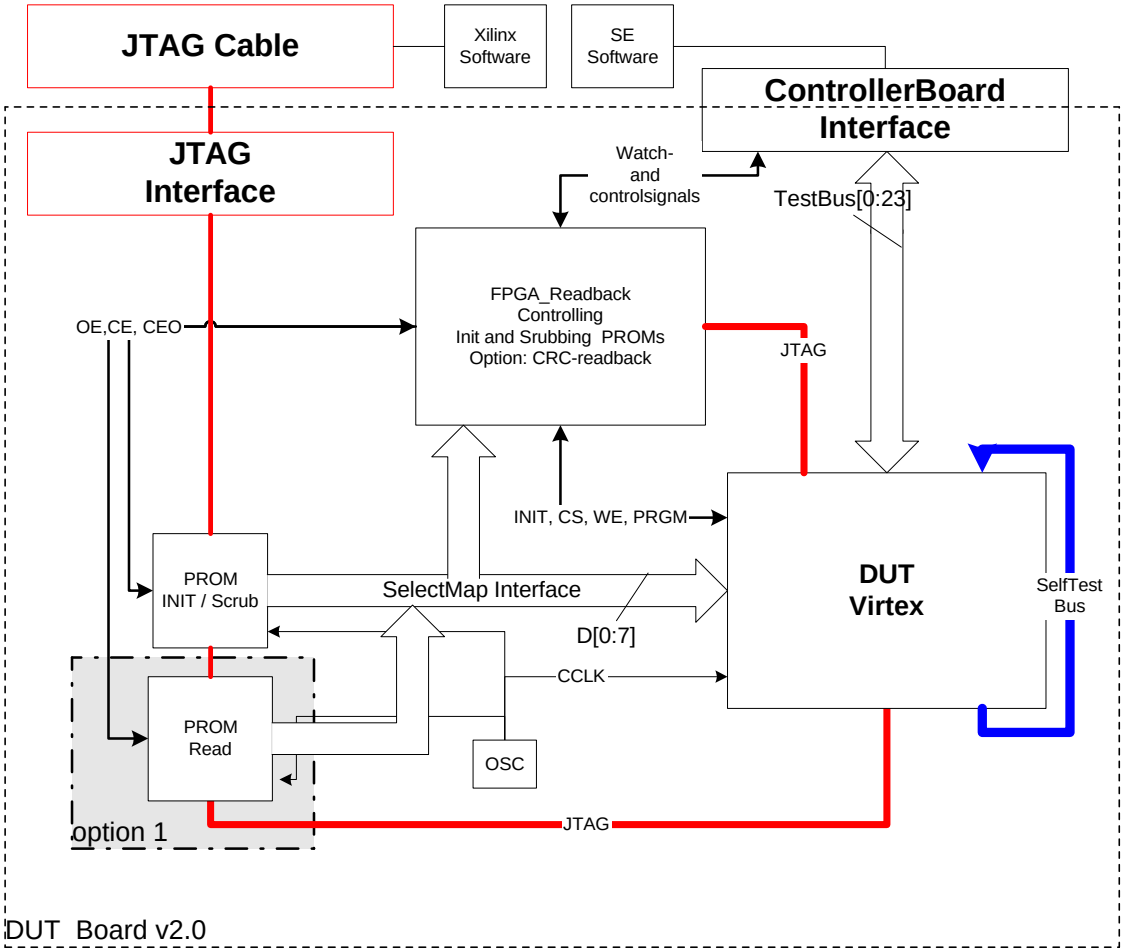

Figure 4.3 Schematic drawing of DUT board with configuration interface for the Virtex device.

The configuration controller chip on the DUT-board is controlling the PROM and configuration ports of the DUT. A program command can be sent to the DUT, which clears its configuration memory and starts an automatic re-configuration of the DUT from the PROM. During the test of the DUT the configuration controller is continuously scrubbing the DUT configuration memory with new configuration data from the PROM's.

All data from the PROM's to the DUT is transferred through the parallel SelectMAP interface, which supports the partial configuration feature making it possible to continuously scrub the device with new configuration data during operation.

The controller board also controls the power supply for the DUT by relays and sends status signals to a Data Logger connected to the board.

5. TOTAL DOSE TEST TECHNIQUES

Total dose tests have been performed on 4 samples programmed with the non-TMR design. Both static and dynamic operation modes have been tested in total dose tests. During irradiation all devices were separately biased with V_{CCO}=3.3V and V_{CCINT}=2.5V.

5.1 General

The total dose tests were performed at the hospital of Borås. Irradiation up to 150 krad(Si) at a dose rate of 1,1 krad(Si)/h have been performed in steps indicated in Table I. At each step parameter measurements have been performed on ~30 of all 208 available pins. In-situ measurements of function and standby current were performed.

TABLE I
RADIATION AND ANNEALING STEPS

Step	Irradiation	Annealing
0	Pre	
1	50 krad(Si)	
2	78 krad(Si)	
3	150 krad(Si)	
4		168h at Room Temperature
5		168h at 100°C

5.1.1 Static Test Conditions

Two samples were static biased without power cycling and functional testing during irradiation. Bias conditions of user I/Os are described in 5.2.1.

5.1.2 Dynamic Test Conditions

Two samples were tested in dynamic test conditions. The samples were clocked with checkerboard data at 1.25 MHz. The configuration data were continuously updated (scrubbing) from the configuration PROM. The samples were operated in a 1 hour test cycles

1 hour in dynamic operation
2 minutes in static mode for standby current measurement
Power cycling
Functional test on part of device

In the power cycling step the power to the device is turned off and on to test for start-up problems. During the Annealing all samples were operated in static mode and no power cycling or functionality tests were performed.

5.2 Parameter Measurements

Pre-, intermediate- and post-irradiation electrical measurements have been performed on the parameters listed in Table II. All measurements were performed with SE's component tester, SZ M3000.

TABLE II
ELECTRICAL PARAMETERS AND CONDITIONS

Parameter	Conditions	Low Limit	High Limit
I_{IL}	V_{IN} = GND V_{CCINT} = 2.5V+5% V_{CCO} = 3.3V+10%	-10µA	10µA
I_{IH}	V_{IN} = V_{CCI} V_{CCINT} = 2.5V-5% V_{CCO} = 3.3V-10%	-10µA	10µA
V_{OL}	I_{OL} = 24mA (LVTTL) V_{CCINT} = 2.5V+5% V_{CCO} = 3.3V+10%	-	0.4V
V_{OH}	I_{OH} = - 24mA (LVTTL) V_{CCINT} = 2.5V-5% V_{CCO} = 3.3V-10%	2.4V	V_{CCO}
I_{OZL}	V_{IN} = GND Output disabled V_{CCINT} = 2.5V+5% V_{CCO} = 3.3V+10%	-10µA	10µA
I_{OZH}	V_{IN} = V_{CCI} Output disabled V_{CCINT} = 2.5V-5% V_{CCO} = 3.3V-10%	-10µA	10µA
Propagation Delays	V_{CCINT} = 2.5V-5% V_{CCO} = 3.3V-10%		

After the first irradiation step it was discovered that the supply current of the component tester was too weak. Instead external power supplies were used with V_{CCINT}=2.5V and V_{CCO}=3.3V for all measured parameters.

Positive and negative propagation delays were measured from input to output of the binning circuits and DC parameter measurement was performed on all in- and outputs of the binning circuits and on the six data outputs from the Self test circuit.

5.2.1 Bias Conditions of I/Os During Irradiation

The inputs to the binning circuits can be in two different states during irradiation,

- 1 kOhm connected to Vcc=3,3V
- 1 kOhm connected to GND

All cells in the binning circuits were either static high or static low during irradiation.

Outputs of the binning circuits can be in two different states during irradiation,

- static high with 1kOhm load to GND
- static low with 1kOhm load to Vcc=3,3V

The data outputs from the Self-test circuit were not connected on the DUTboard. The outputs were toggled with half the clock frequency giving 0,5Mhz in the dynamic test condition and un-toggled in the static test condition.

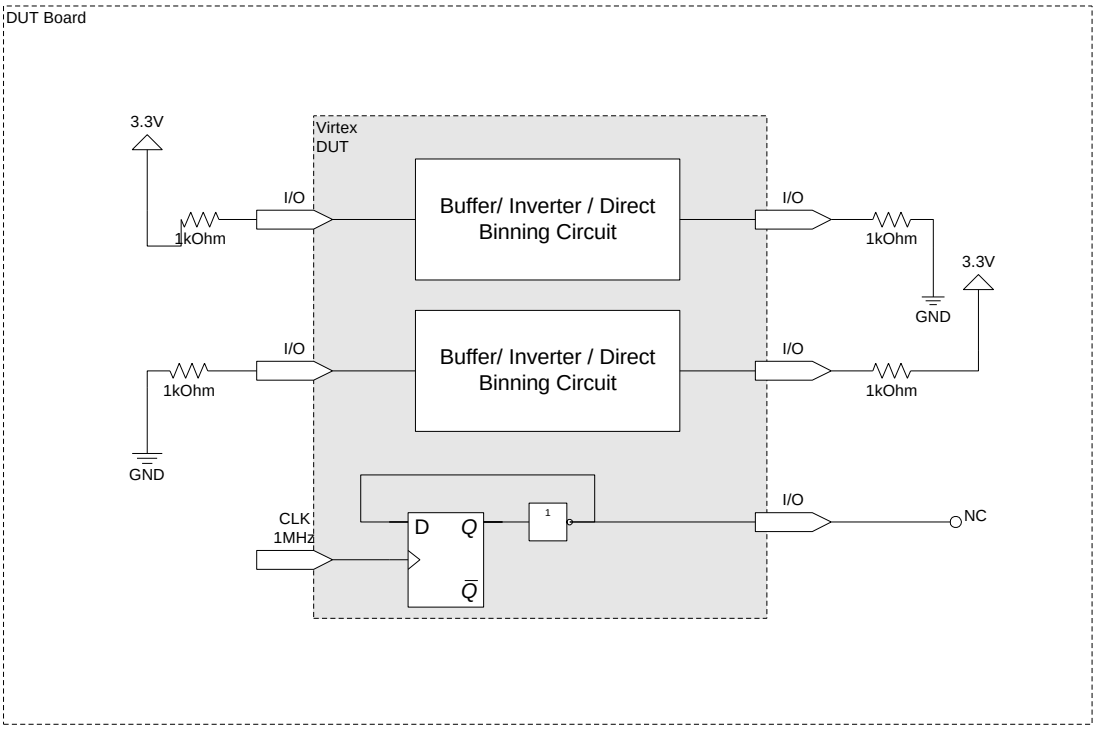

Figure 5.1 Principal drawing for configuration of I/Os during irradiation.

6. SEU TEST TECHNIQUES

Two design methods were tested for comparison, the TMR and non-TMR design, see paragraph 3.2 and 3.3. Both designs having the same basic functionality.

6.1 SEU Error Separation

Detected errors out from the DUT could originate from SEU in registers (user logic flip-flop) of the device, in the configuration data causing functional errors in parts of the device and in control registers of the device causing global functional errors. The analysed data errors are separated into three different domains, SEU in registers, SEU in configuration data, and SEU in device control registers.

6.1.1 Register Error Types

SEU in the user logic registers are corrected with new data loaded into the registers in connection with each read cycle. The data are analysed for single bit errors and categorised into the following error types:

FF(0-1) Read ‘1’ from flip-flop registers when ‘0’ is expected.

FF(1-0) Read ‘0’ from flip-flop registers when ‘1’ is expected.

FF Total sum of all FF errors (above) read from the shift registers.

DataSwap This error type showed up as two bit errors in registers next to each other. First a ‘0’ was read when ‘1’ was expected and in the next register a ‘1’ is read when a ‘0’ was expected. It is only observed in this order. The error was not persistent in the next test cycle. This error type stand for 25% of all user logic registor errors. No explanation has been found for this error type.

6.1.2 Configuration induced Error types

SEU in the configuration data will remain until the configuration data are corrected with new configuration data. Errors that are caused by SEU in the configuration are quantified by observing the following signatures in the test data:

Routing An SEU in the configuration logic (routing bits and lookup tables) may cause errors in the configured function of the operational device. This gives errors from the shift registers that are permanent until next time the device is scrubbed with new configuration data.

Persistent A persistent error is a permanent error that can not be corrected with new configuration data. The device needs to be reset and completely reinitialised. This is the result of SEU in “weak keeper” circuits used in the Virtex architecture when logical constants are implied in the configured design such as unused clock enable signals for registers.

SelfTest SelfTest errors are of the same type as the routing type, but instead of interrupting a shift register it interrupts the function of the SelfTest module.

6.1.3 SEU in Device Control Registers

SEFI type Function of the whole device is interrupted in one hit and all shift register data are lost. The device requires a reset and complete reconfiguration for correction. Xilinx believe this to be SEU in the POR register in the control registers of the architecture.

6.2 Other Test Considerations

The test system is optimised for SEU testing of the registers. Data are clocked in and out and then paused for a pre-set time, giving the radiation time to upset the registers before reading out the data. Every upset in the tested registers (*FF, DataSwap*) will be detected.

An SEU in configuration data causing a functional error is corrected when new configuration data are written to the DUT. To be able to detect all of these errors the DUT must be continuously tested. Since the DUT is paused in our tests we will not see all of these errors (*Routing, SelfTest*). Therefor we have estimated the fraction of errors detected. (*Detection factor*).

Two different pause times (time where DUT is not clocked between read/write of data) are used during the tests, 223ms and 4ms. Testing the non-TMR design mostly used the long pause time since the flow of error data otherwise became too high for the system to handle.

Selection of the scrub time between 10,38ms / 22,93ms and 166ms could be performed in the test system. The longer scrubbing rates were only used in the first test runs for calibration purposes.

7. TOTAL DOSE TEST RESULTS

The total dose test was planned out from the fact that this device type will be good for more than 100 krad(Si). Already at 45 krad(Si) problems with the start-up of one device was observed (Fig. 7.1). The supply current at the power up sequence increased remarkably. The device went into a state of unlimited current use where the device was not configured for operation.

The two devices tested with dynamic conditions were power cycled every hour during irradiation and at 45 krad(Si) sn#39 failed to initialise (Fig. 7.1). The two devices in static mode were only power cycled between the irradiation steps. After the first irradiation step at 50krad(Si) none of the two static mode devices succeeded to initialise (Fig. 7.3).

The test boards used a power-up rate faster than the Xilinx specification required (some few microseconds). The power-up of pre-irradiated devices worked perfectly. According to Xilinx specification requirements the devices shall be powered up at a rate of 2 to 50 milliseconds and use up to 2 Ampere of current. The test boards were reconstructed after the second irradiation step at 78 krad(Si) to fulfil these requirements. The problems with power up were, however, not solved with the new power solution.

All devices were irradiated up to 150 krad(Si) (120 krad(Si) for sn#37) but due to the power-up failure the bias conditions was out of control from 50krad(Si). In conclusion, the radiation test has not been successfully carried out to more than 50krad(Si).

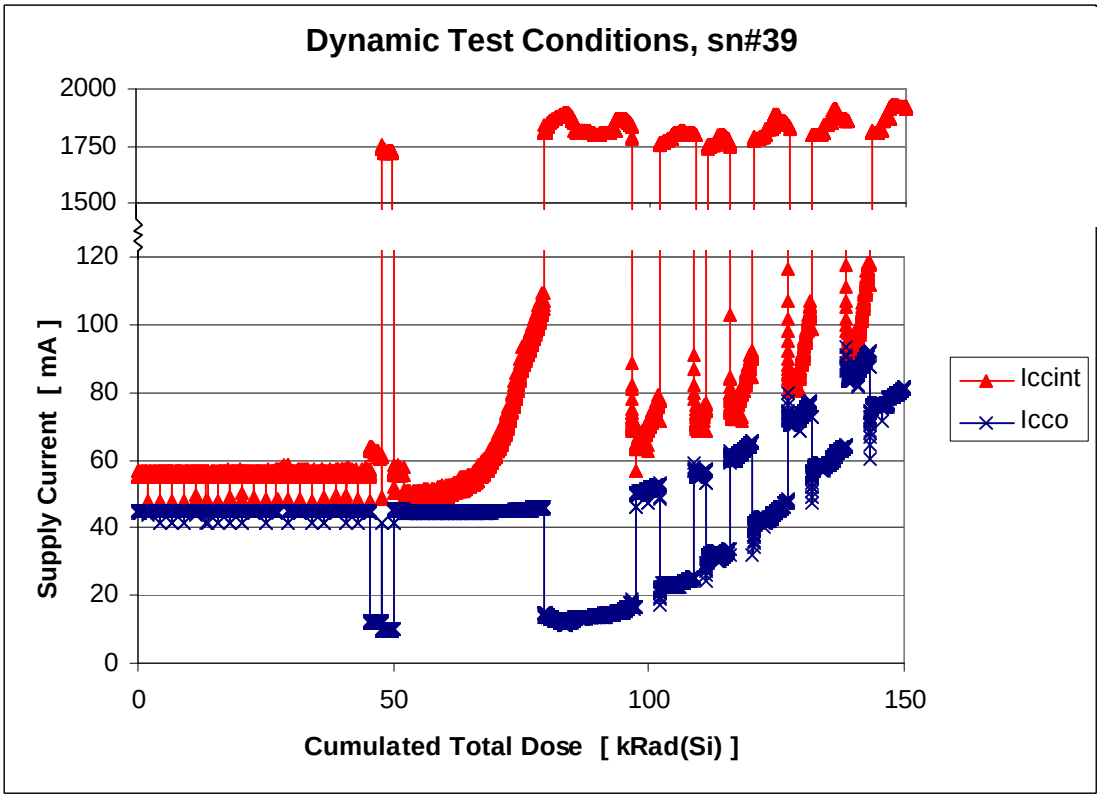

Figure 7.1 *Supply current values during irradiation for sn#39 irradiated under dynamic test conditions. The dips in the current during the first 50 krad(Si) are when the device is in static mode within each test cycle. At 45 krad(Si) the initialisation failed after a power cycling. The functional test proceeding the power cycling failed. The supply current for the I/O logic (I_{CCO}) was just 10 mA which indicated that the DUT wasn't configured. To avoid power-up failures the power cycling wasn't performed within the test cycle between 50 and 78 krad(Si). The second device in dynamic mode, Sn#38 showed similar current behaviour, but the first power-up failure occurred after parameter testing at 78krad(Si).*

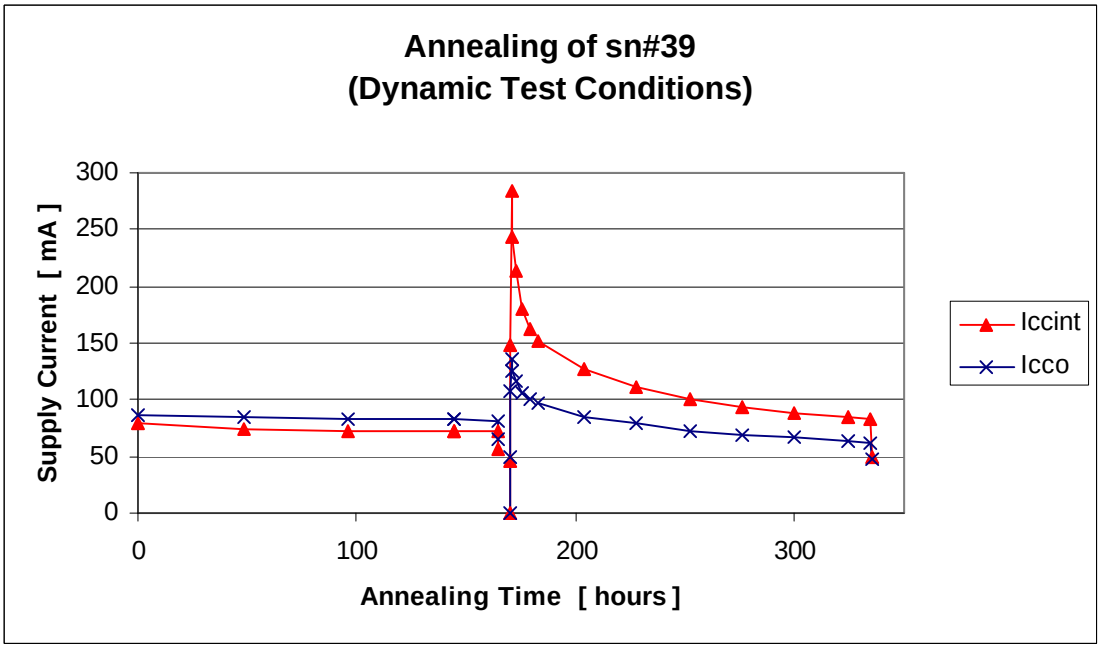

Figure 7.2 *Supply current values for sn#39 during 168h room temperature and 168h 100 degree annealing. The device was static biased during annealing and not power cycled. After high temperature annealing the last measuring point is performed at room temperature. It can be seen that both currents decreased to less than 50 mA which were the pre-irradiation values. The high temperature annealing indicate a special anneal effect on the induced radiation damages.*

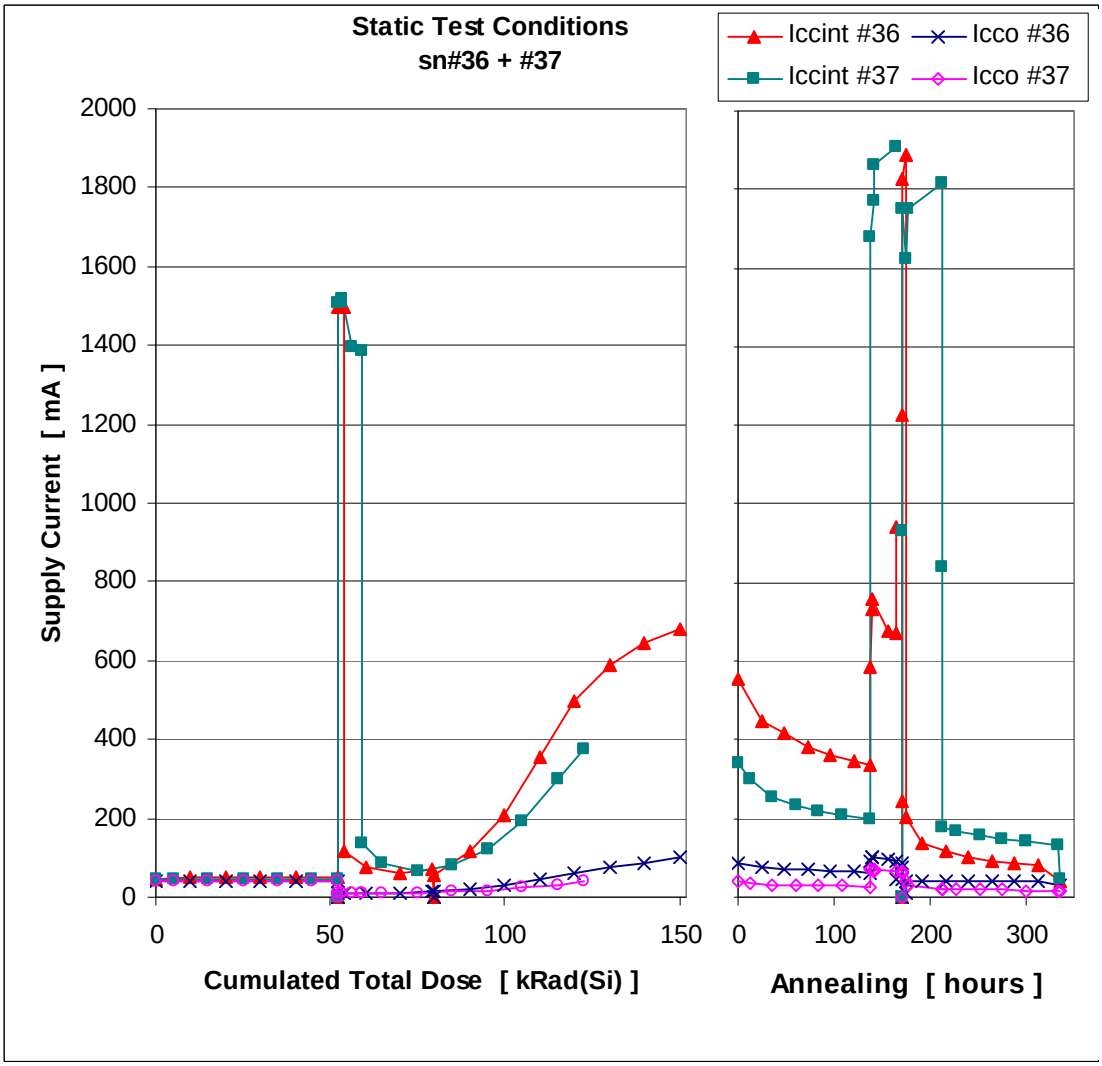

Figure 7.3 *Supply current values during irradiation and annealing for sn#36 and sn#37 that was irradiated in static test conditions. After 50 krad(Si) both DUTs failed to initialise. The supply current for the I/O logic was just 10mA which indicates that the DUT wasn't configured. Sn#37 was removed between the 50 krad(Si) and 78krad(Si) irradiation step and therefor only received a cumulated total dose of 122 krad(Si).*

7.1 Supply Leakage Current

No supply current increase was observed (except increase related to power-up failure) for any devices up to 50 krad(Si) (Fig. 7.1, 7.3). After 50 krad(Si) only sn#38 and sn#39 (dynamic conditions) initialised properly and after 65 krad(Si) the current started to increase. This is well in line with earlier performed total dose testing [2,4].

After the 78 krad(Si) step, samples sn#38 and sn#39 did not initialise and further analysis are therefore meaningless.

After temperature annealing all devices did return to pre-irradiated supply current values.

7.2 Details of Power-up Failure

The power up failure was studied in detail when doing parameter testing using a power supply with the current limited to 2A and a power-up rate within specification requirements. The power up was studied with a current probe and an oscilloscope. Figures 7.4-7.8 show the voltage (V_{CCINT}) and current (I_{CCINT}) during power-up. At 50krad(Si) the current at power-up had increased remarkable for all irradiated devices and one device (sn#37) wasn't possible to initialise.

After enhanced temperature annealing all devices returned to normal operation during the power-up.

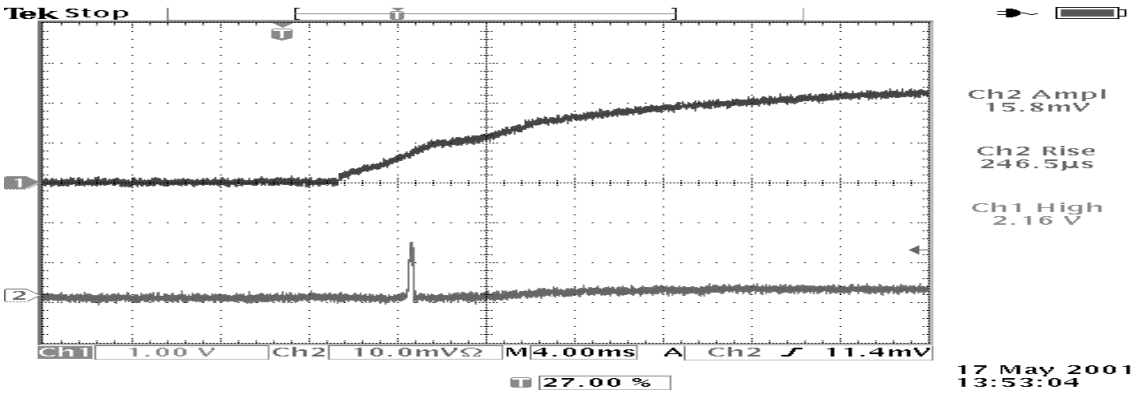

Figure 7.4 Oscilloscope image of V_{CCINT} (Ch1- 1V / div) and I_{CCINT} (Ch2- 0.2A / div) for the reference device, REF#33 (4ms / div). The current peak observed during the ramp-up of the voltage is according to specification [3].

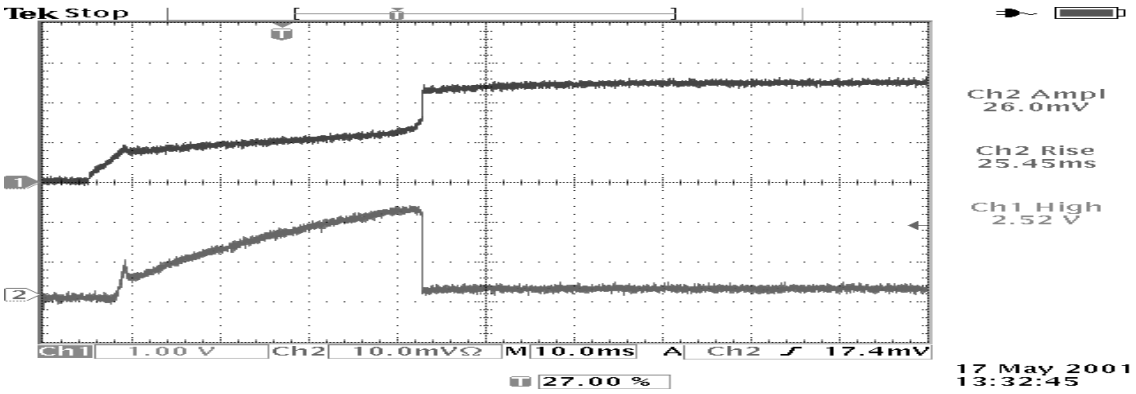

Figure 7.5 Oscilloscope image of V_{CCINT} (Ch1- 1V / div) and I_{CCINT} (Ch2- 0.5A / div) for sn#36 after 50 krad(Si) (10ms / div). The current peak observed in the pre-irradiation case is here followed by furhter increase in the current until the voltage has reached 1.2V.

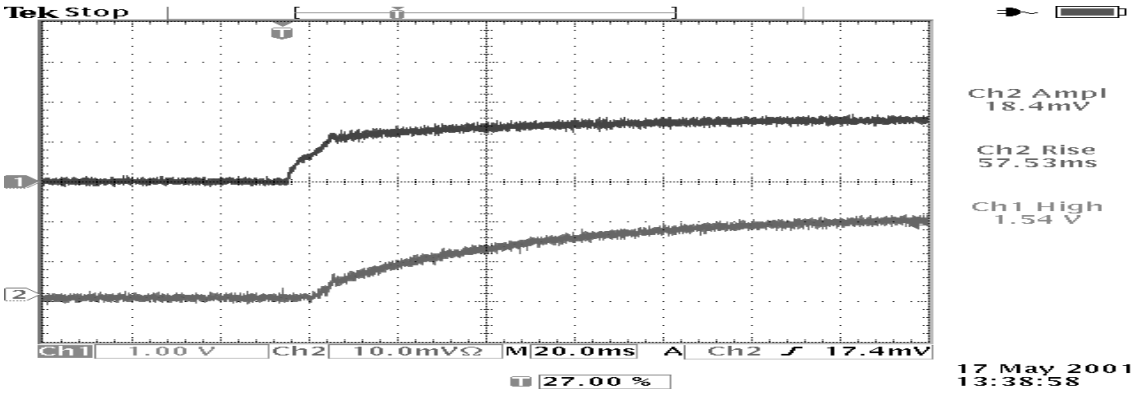

Figure 7.6 Oscilloscope image of V_{CCINT} (Ch1- 1V / div) and I_{CCINT} (Ch2- 1.0A / div) for sn#37 after 50krad(Si) (20ms / div). The device was never initialised likely because of the current limit at 2A on the power supply.

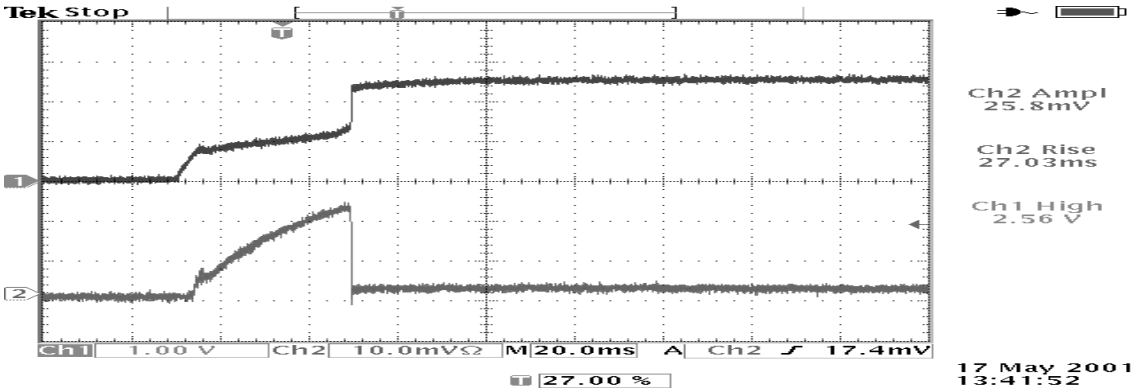

Figure 7.7 Oscilloscope image of V_{CCINT} (Ch1- 1V / div) and I_{CCINT} (Ch2- 0.5A / div) for sn#38 after 50krad(Si) (20ms / div). The current peak observed in the pre-irradiation case is here followed by furhter increase in the current until the voltage has reached 1.2V.

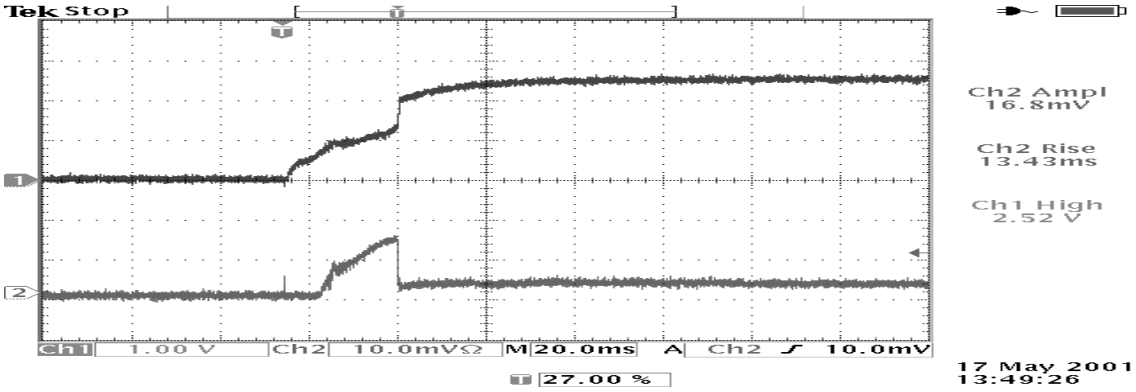

Figure 7.8 Oscilloscope image of V_{CCINT} (Ch1- 1V / div) and I_{CCINT} (Ch2- 0.5A / div) for sn#39 after 50krad(Si) (20ms / div). The current peak observed in the pre-irradiation case is here followed by furhter increase in the current until the voltage has reached 1.2V.

7.3 Parameter Measurement Results

At the parameter testing after the first irradiation step at 50krad(Si), the power source of the SZ test equipment (max 0,5A) wasn't able to power-up the devices. Instead an external power supply, giving 2A, was used. The new power supply full fills the specification requirements.
When changing to an external power supply, the test conditions were changed for most of the parameters from the pre-irradiation measurements (Table II). All tests were performed with V_{CCINT} at 2,5V and V_{CCO} at 3.3V.

The fact that devices have not always been initialised during irradiation makes the comparison between different samples meaningless. Table III shows an overview of tested devices. A summary of the results of the DC parameter measurement is presented in Table IV.

TABLE III
PERFORMED DC PARAMETER MEASUREMENTS ON IRRADIATED PARTS

sn#	Pre Irradiation Measurement	50 krad(Si) Measurement	78 krad(Si) Measurement	150 krad(Si) Measurement	Post RT Anneal Measurement	Post 100°C Anneal Measurement
#36	√	√	√	Not initialised	Broke down during measurement	√
#37	√	Not initialised	√	Not initialised	Not initialised	√
#38	√	√	Not initialised	√	Sent to Xilinx	Sent to Xilinx
#39	√	√	Not initialised	√	√	√

TABLE IV
SUMMARY OF DC PARAMETER MEASUREMENTS.

Parameter	**50 krad(Si) Measurement**	**78 krad(Si) Measurement**	**150 krad(Si) Measurement**	**Post RT Anneal Measurement**
I_{IH}	All parts OK	Drift within spec. on measured parts	All parts measured parts out of spec. Sn#38 <20uA Sn#39 up to 400uA	#39 out of spec. up to 250uA
I_{IL}	All parts OK	All measured parts OK	All measured parts Small drift	#39 Small drift
I_{OZH}	All parts Drift within spec.	Drift within spec. on measured parts	#38 Drift within spec. #39 out of spec. up to 400uA	#39 Small anneal
I_{OZL}	All parts Drift within spec.	Drift within spec. on measured parts	#38 OK #39 small drift	#39 Small anneal

At Post 100°C Anneal all parameters had returned to initial values. V_{OH} and V_{OL} showed no drifts in any measurement

7.3.1 I/O Damages

We have chosen to present DC parameter data to the first irradiation step at 50krad(Si). Data for Sn#37 are actually taken from the 78krad(Si)-measurement, but since it wasn't irradiated between 50 and 78krad(Si) it finally had a cumulated dose of 50krad(Si) and was measured one day after irradiation.

We have observed leakage current damages in all devices. The input low and output low leakage currents (I_{IL}, I_{OZL}) are negligible, while the results for the input high and output high leakage currents (I_{IH}, I_{OZH} in Fig. 7.9-10) are worse and out of specification at 50krad(Si).
The output Voltage parameters show no drifts or damages.

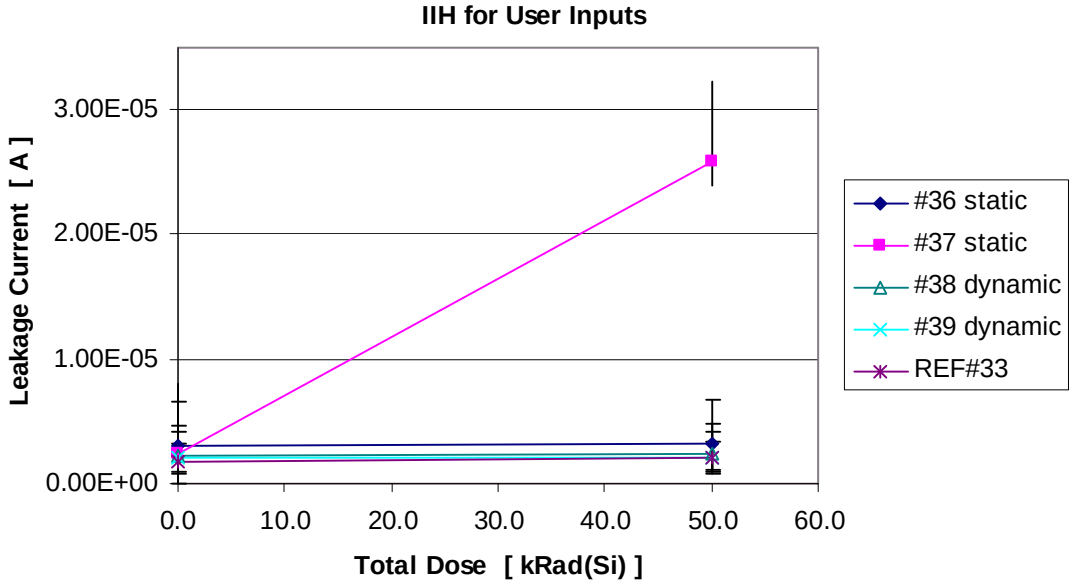

Figure 7.9 Average Input Leakage High Current for all measured user I/Os and devices up to 50krad(Si). Specification limit is 1×10^{-5} A. Error bars indicate max and min-measured value for each device.

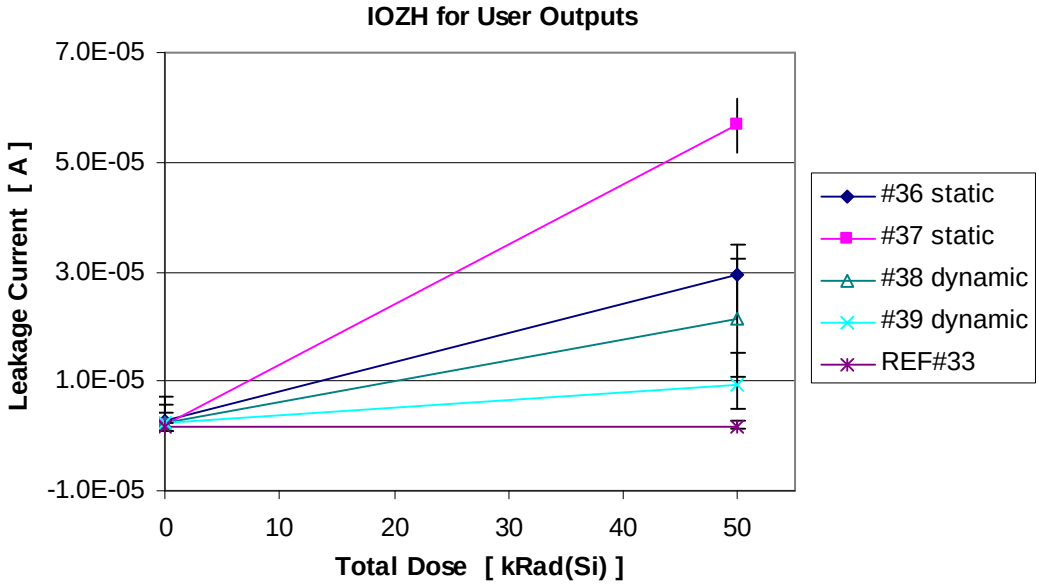

Figure 7.10 Average Output Leakage High Current for user I/Os and devices up to 50krad(Si). User outputs that were driven high during irradiation have been excluded. They had lower leakage than the outputs presented in this graph. Specification limit is 1×10^{-5} A. Error bars indicate max and min-measured value for each device.

7.3.2 Parameter Values for SN#39

Device sn#39 was the one that did survive this radiation test best from problems with power up failure. We have chosen to present all taken DC parameter data for the device. The measurement after 78 krad(Si) wasn't performed due to power up failure.

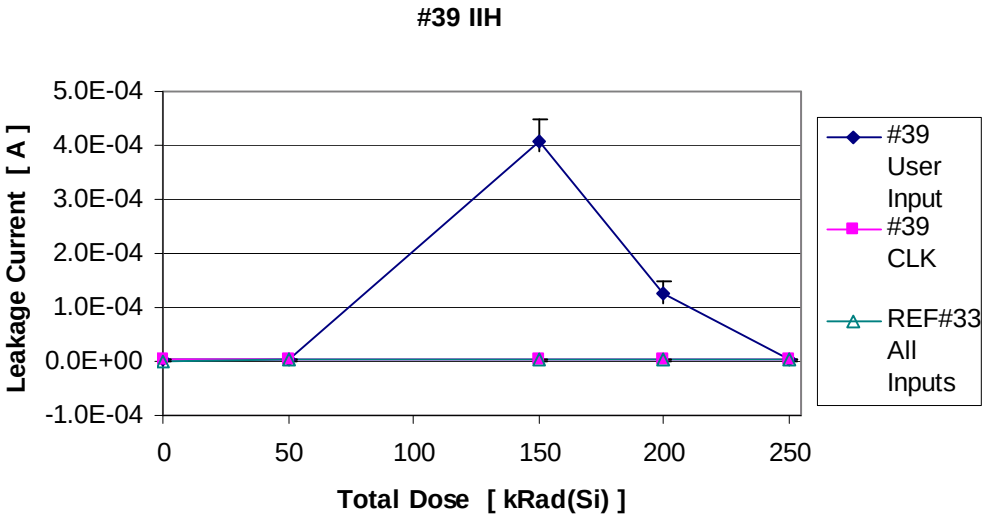

Figure 7.11 Average Input Leakage high Current for sn#39 for user I/Os and dedicated Clock. Measurement at 200 and 250 krad(Si) are the two annealing steps. All measurement over 1.2×10^{-4} A was made with another instrument. Error bars indicate max and min measured value for each device.

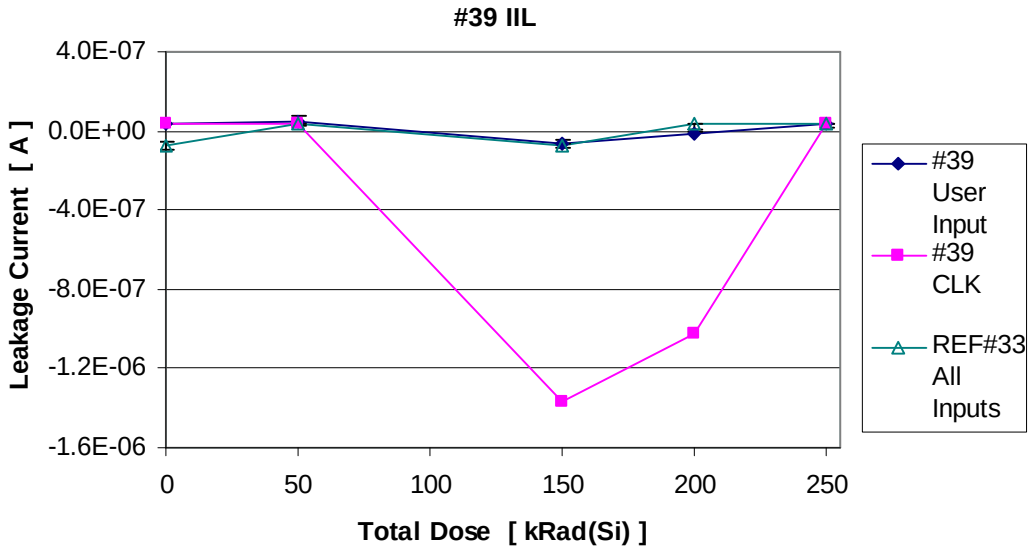

Figure 7.12 Average Input Leakage Low Current for sn#39 for user I/Os and dedicated Clock. Measurement at 200 and 250 krad(Si) are the two annealing steps. All measurements are well within specification limit of 1×10^{-5} A. Error bars indicate max and min measured value for each device.

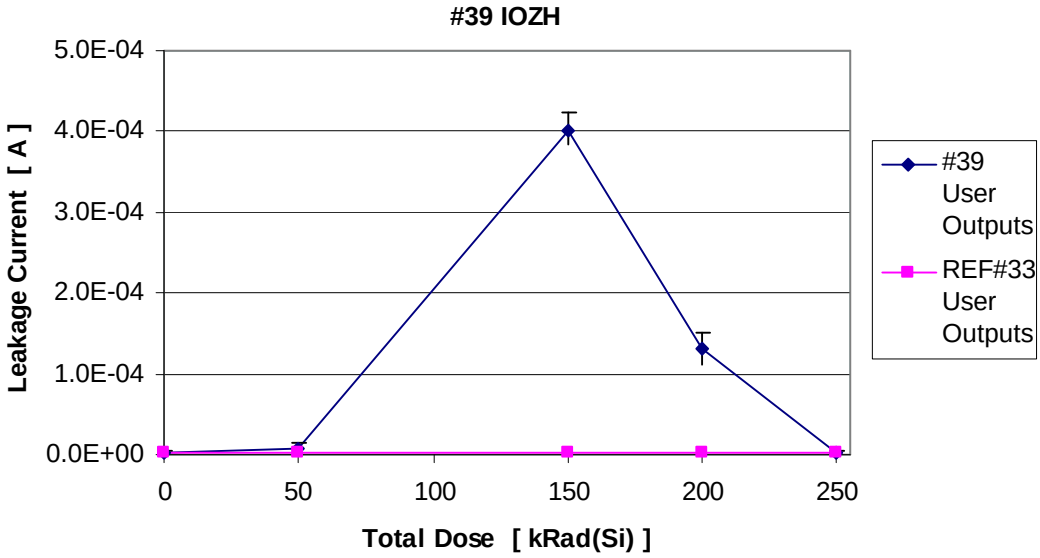

Figure 7.13 Average Output Leakage high Current for sn#39 for user I/Os. Measurement at 200 and 250 krad(Si) are the two annealing steps. All measurement over 1.2×10^{-4} A was made with another instrument. Error bars indicate max and min measured value for each device.

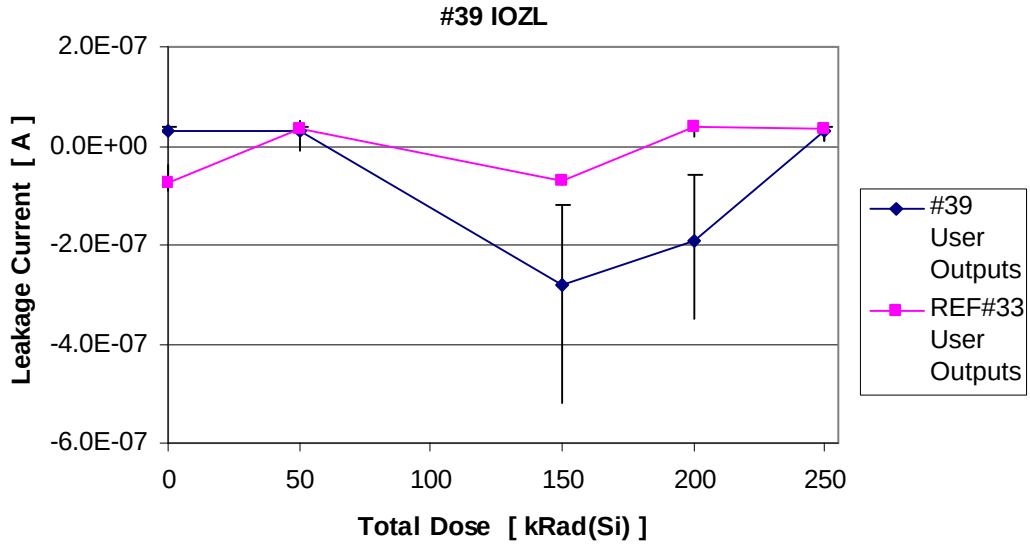

Figure 7.14 Average Output Leakage Low Current for sn#39 for user I/Os and dedicated Clock. Measurement at 200 and 250 krad(Si) are the two annealing steps. All measurements are well within specification limit of 1×10^{-5} A. Error bars indicate max and min measured value for each device.

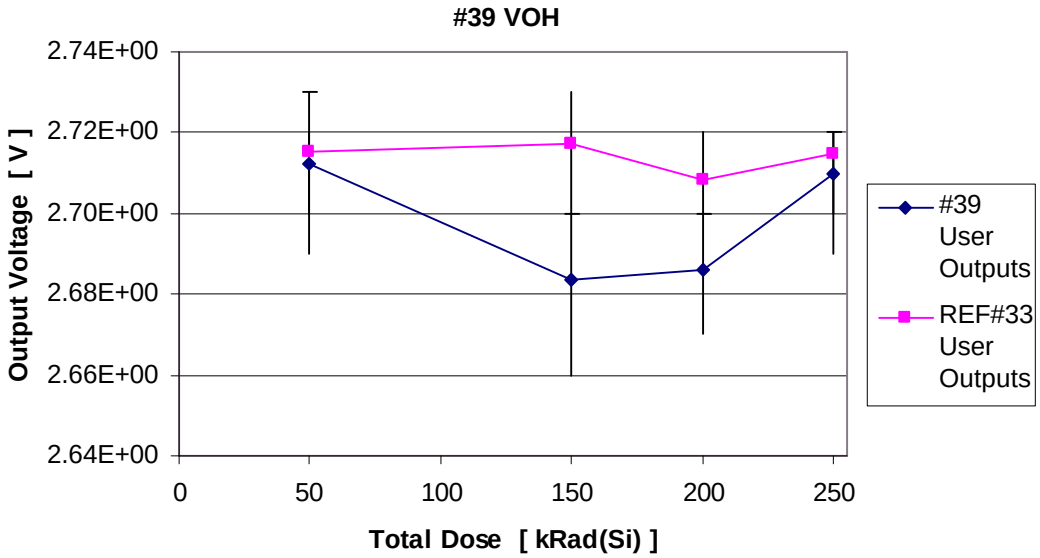

Figure 7.15 Average Output High Voltage for SN#39 for user I/Os. Specification limit is 2.4 Volts but the parameter is measured at nominal supply voltage conditions. Pre irradiation measurement was performed with specified these conditions and are not presented since it isn't valid for comparison. Measurement at 200 and 250 krad(Si) are the two annealing steps. Error bars indicate max and min measured value for each device.

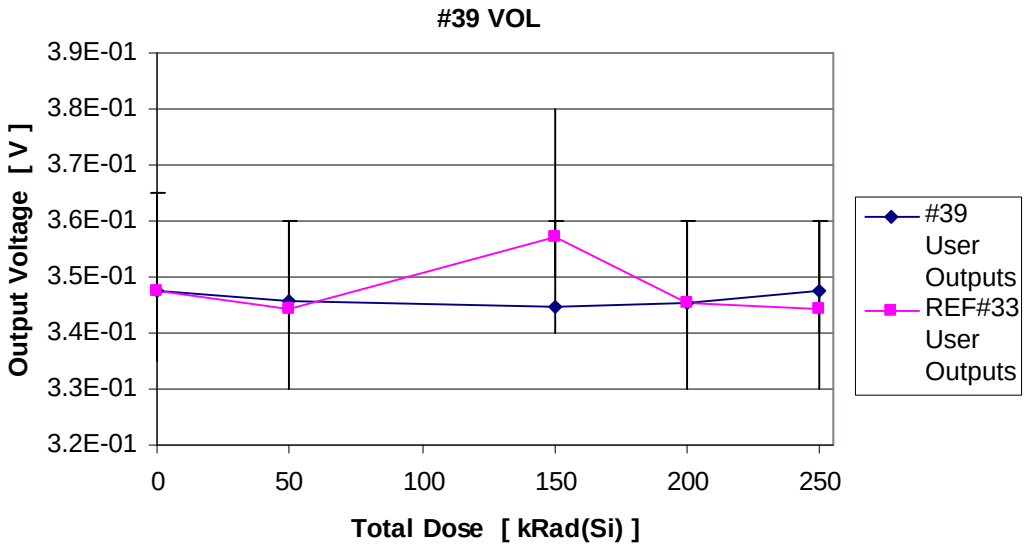

Figure 7.16 Average Output Low Voltage for SN#39 for user I/Os. Specification limit is 0.4 Volts but the parameter is measured at nominal supply voltage conditions. Pre-irradiation measurement was performed with specified these conditions and are not presented since it isn't valid for comparison. Error bars indicate max and min measured value for each device. Measurement at 200 and 250 krad(Si) are the two annealing steps.

7.4 Propagation Delays

Positive and negative pulse delays have been measured for the 12 binning circuits designed into the DUT. The resolution for positive pulses is 1 ns and negative pulses 5 ns.
No significant changes in timings have been observed.

TABLE V
AVERAGE OF POSITIVE TIME DELAYS

Part#	Binning	0 krad(Si)*	50 krad(Si)	78krad(Si)	150krad(Si)		post RT Anneal	post 100C Anneal
REF#33	DIR	12.25	11.75	11.5	11.75		11.75	11.5
	INV	67.75	65	64.75	65		64.875	64.75
	BUF	65.5	62.5	62.5	62.5		62.5	62.25
#38	DIR	12.5	11.5	Not testable	11		Sent to Xilinx	Sent to Xilinx
	INV	68.5	66	Not testable	65.75		Sent to Xilinx	Sent to Xilinx
	BUF	66.75	63.5	Not testable	63.75		Sent to Xilinx	Sent to Xilinx
#39	DIR	12.5	11.5	Not testable	11.75		11.5	11.5
	INV	69	66	Not testable	66		65.75	65.5
	BUF	66.75	63.5	Not testable	63.5		63.5	63.25

* *At all pre-irradiation measurements were the supply voltage set to minimum giving longer time delays.*

TABLE VI
AVERAGE OF NEGATIVE TIME DELAYS

Part#	Binning	0 krad(Si)*	50 krad(Si)	78krad(Si)	150krad(Si)		post RT Anneal	post 100C Anneal
REF#33	DIR	10	11.25	7.5	10		11.25	10
	INV	67.5	63.75	63.75	63.75		62.5	62.5
	BUF	63.75	62.5	61.25	62.5		62.5	62.5
#38	DIR	10	10	Not testable	7.5		Sent to Xilinx	Sent to Xilinx
	INV	67.5	66.25	Not testable	63.75		Sent to Xilinx	Sent to Xilinx
	BUF	63.75	62.5	Not testable	61.25		Sent to Xilinx	Sent to Xilinx
#39	DIR	8.75	10	Not testable	15		10	10
	INV	67.5	63.75	Not testable	70		65	62.5
	BUF	62.5	62.5	Not testable	70		62.5	62.5

* *At all pre-irradiation measurements were the supply voltage set to minimum giving longer time delays*

8. SEE TEST RESULTS

Each test was performed with a variety of atomic species up to a fluence of $1 \cdot 10^6$ ions/cm^2, or until all the shift registers was permanently disabled by the "Persistent" error or all 14 shift registers were eliminated by the "SEFI" error. With this error in a shift register no data came out and the registers couldn't be tested.

8.1 Non-TMR Design

8.1.1 Configuration Type Errors

Each configuration type error was observed and their cross-sections are plotted in Fig. 8.1.
The Cross section is specific for this design. To predict cross section for a 100% utilised device you must multiply these cross sections with the utilisation factor for this design (about 32% for the routing errors and maybe 5% for the SelfTest module).

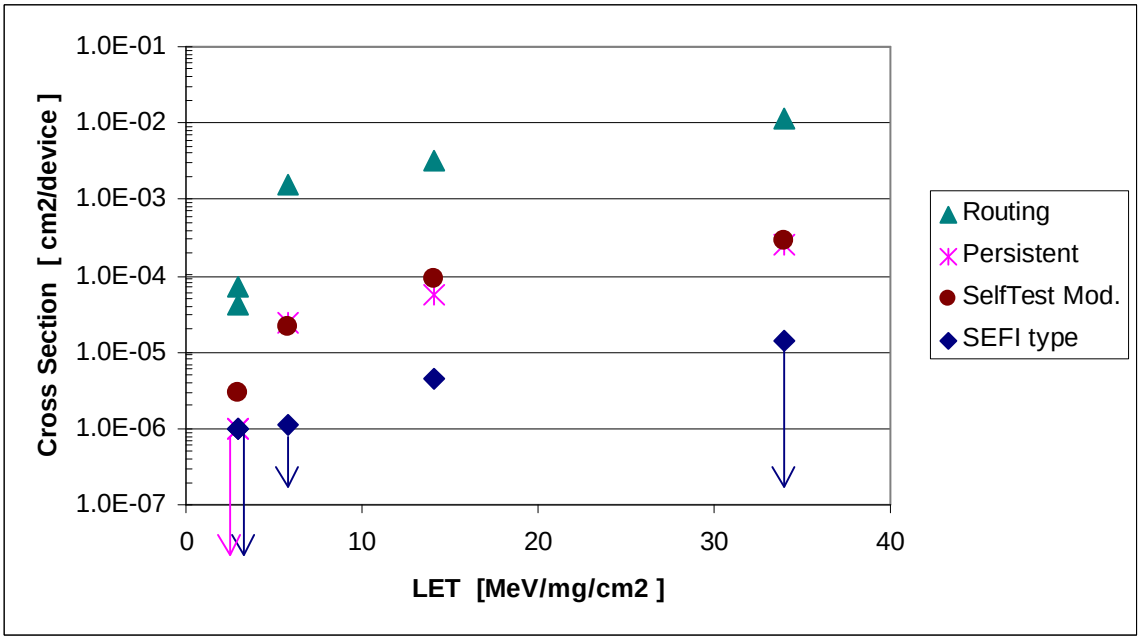

Figure 8.1 Configuration errors for non-TMR Design. Arrows indicate test without any upsets. The Cross sections are per device and are specific for this design. To predict cross section for a 100% utilised device you must multiply these cross sections (except SEFI type) with the utilisation factor for this design (about 32% for the routing and persistent errors and maybe 5% for the SelfTest module).

Run#	**Ion [LET]**	**Error type**	**# of Errors**	**Flux** Ions/cm^2/s	**Fluence** Ions/cm^2	**Detection ratio**	**Cross Section** cm^2/device
#16	Ar [14,1]			~700			
		Routing	25		1,6e+5	0,05	3,3e-3
		Persistent	9		1,6e+5	1	5,8e-5
		SelfTest	1		2,2e+5	0,05	9,3e-5
		SEFI type	1		2,2e+5	1	4,5e-6
#23	Ne [5,85]			~1000			
		Routing	37		5,0e+5	0,05	1,5e-3
		Persistent	12		5,0e+5	1	2,4e-5
		SelfTest	1		9,3e+5	0,05	2,2e-5
		SEFI type	0		9,3e+5	1	< 1,1e-6
#28	N [2,97]			~2000			
		Routing	2		1,0e+6	0,05	4,1e-5
		Persistent	0		1,0e+6	1	< 1,0e-6
		SelfTest	0		1,0e+6	0,05	(< 2,0e-5)
		SEFI type	0		1,0e+6	1	< 1,0e-6
#31*	N [2,97]			~2000			
		Routing	25		1,0e+6	0,66	3,8e-5
		Persistent	0		1,0e+6	1	< 1,0e-6
		SelfTest	1		1,0e+6	0,66	1,5e-6
		SEFI type	0		1,0e+6	1	< 1,0e-6
#35	Kr [34]			~300			
		Routing	24		4,3e+4	0,05	1,1e-2
		Persistent	11		4,3e+4	1	2,5e-4
		SelfTest	1		7,0e+4	0,05	2,9e-4
		SEFI type	0		7,0e+4	1	< 1,4e-5

* In this run was the pause time decreased down to 4ms which increase the amount of routing errors detected in the test (*detection ratio*).

8.1.2 Register Type Errors

FF errors were observed at a LET threshold of 3 MeV/mg/cm^2 with a saturation cross-section of ~10^{-6} cm^2. The results are plotted in Fig. 8.2.

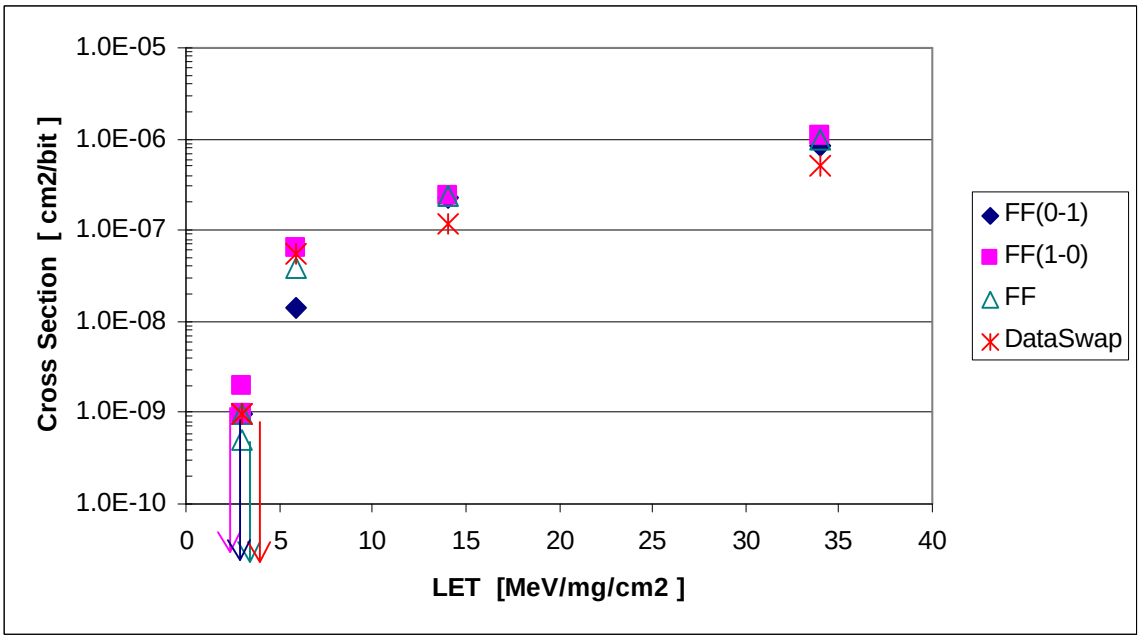

Figure 8.2 Register Errors for non-TMR Design. Arrows indicate test without any upsets.

Run#	Ion [LET]	Error type	# of Bits	# of Errors	Flux Ions/cm^2/s	Fluence Ions/cm^2	Detection ratio	Cross Section cm^2/bit
#16	Ar [14,1]				~700	1,6e+5	1	
		FF(0-1)	1008	36				2,3e-7
		FF(1-0)	1008	38				2,4e-7
		FF	2016	74				2,4e-7
		DataSwap	1008	18				1,1e-7
#23	Ne [5,85]				~1000	5,0e+5	1	
		FF(0-1)	1008	7				1,4e-8
		FF(1-0)	1008	32				6,3e-8
		FF	2016	39				3,9e-8
		DataSwap	1008	28				5,5e-8
#28	N [2,97]				~2000	1,0e+6	1	
		FF(0-1)	1008	0				< 1,0e-10
		FF(1-0)	1008	2				2,0e-10
		FF	2016	2				9,9e-10
		DataSwap	1008	0				< 1,0e-10
#31	N [2,97]				~2000	1,0e+6	1	
		FF(0-1)	1008	0				< 1,0e-10
		FF(1-0)	1008	0				< 1,0e-10
		FF	2016	0				< 5,0e-11
		DataSwap	1008	0				< 1,0e-10
#35	Kr [34]				~300	4,3e+4	1	
		FF(0-1)	1008	37				8,4e-7
		FF(1-0)	1008	47				1,1e-6
		FF	2016	84				9,6e-7
		DataSwap	1008	22				5,0e-7

8.2 TMR Design

8.2.1 Configuration Type Errors

With the exception of run#15, the SEFI type error was the only observable error. The Persistent error is not observed. The SEFI was observed at a LET of 5.85 MeV/mg/cm^2. This demonstrated that the TMR design method effectively eliminated all non-SEFI configuration induced errors.
The “SEFI type” error is believed to be an SEU in the POR control register, clearing the whole device from configuration data. All I/Os are 3-stated in this state and this was detected at the read out data, which slowly went from read high state to read low state after some test cycles.
In run#15 one “Routing” error was observed. The flux was ~1333 ions/cm^2/s and the device were scrubbed with new configuration data every 10,38ms. This gives a flux/scrub-cycle ratio of 13ions/cm^2/scrub. With a too high flux/scrub-cycle ratio we have an increased risk to have errors in two modules at the same time which could give error in the majority voting circuit. From the tests on the Non-TMR data we know the cross-section for a “Routing” error in one module and can calculate the mean number of errors/scrub-cycle for the test run. With the assumption that the errors are randomly spread in time, the Possion distribution may be used to predict the probability to have two “Routing” errors within the same scrub-cycle. The probability that these two errors in the TMR design shall occure in the same tripled shift register, is $1/14 * 2/3$. With this statistics, we would detect 1,8 errors in this specific test run, we detected one.
Therefore, the observed “routing” error is most likely an artifact of the flux/scrub-cycle ratio. With a 10 times lower flux/scrub-cycle ratio the same statistics predicts that 100 times less errors would be detected.

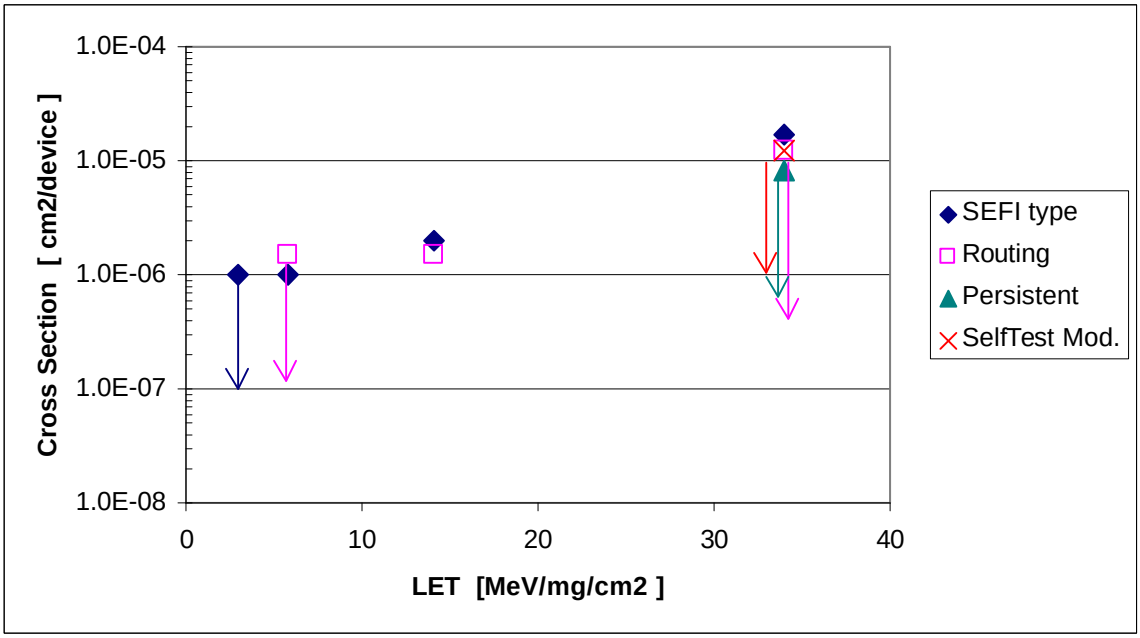

Figure 8.3 Configuration errors for TMR Design. Arrows indicate test without any upsets.

Run#	**Ion [LET]**	**Error type**	**# of Errors**	**Flux** Ions/cm^2/s	**Fluence** Ions/cm^2	**Detection ratio**	**Cross Section** cm^2/device
#15	Ar [14,1]			~1300	1,0e+6		
		SEFI(POR)	2			1	2,0e-6
		Routing	1			0,66	1,5e-6
		Persistent	0			1	<1,0e-6
		SelfTest	0			0,66	<1,5e-6
#24	Ne [5,85]			~1300	1,0e+6		
		SEFI(POR)	1			1	1,0e-6
		Routing	0			0,66	<1,5e-6
		Persistent	0			1	<1,0e-6
		SelfTest	0			0,66	<1,5e-6
#27	N [2,97]			~2000	1,0e+6		
		SEFI(POR)	0			1	< 1,0e-6
		Routing	0			0,66	<1,5e-6
		Persistent	0			1	<1,0e-6
		SelfTest	0			0,66	<1,5e-6
#36	Kr [34]			~400	1,2e+5		
		SEFI(POR)	2			1	1,7e-5
		Routing	0			0,66	<1,2e-5
		Persistent	0			1	<8,3e-6
		SelfTest	0			0,66	<1,2e-5

8.2.2 Register Type Errors

Only one FF error was observed at a LET 14.1 MeV/mg/cm^2 with an estimated cross-section of ~5·10^{-10} cm^2. No other FF errors were recorded in absence of a SEFI type error. It is considered that this error is the result of the flux/scrub-cycle ratio as previously mentioned.

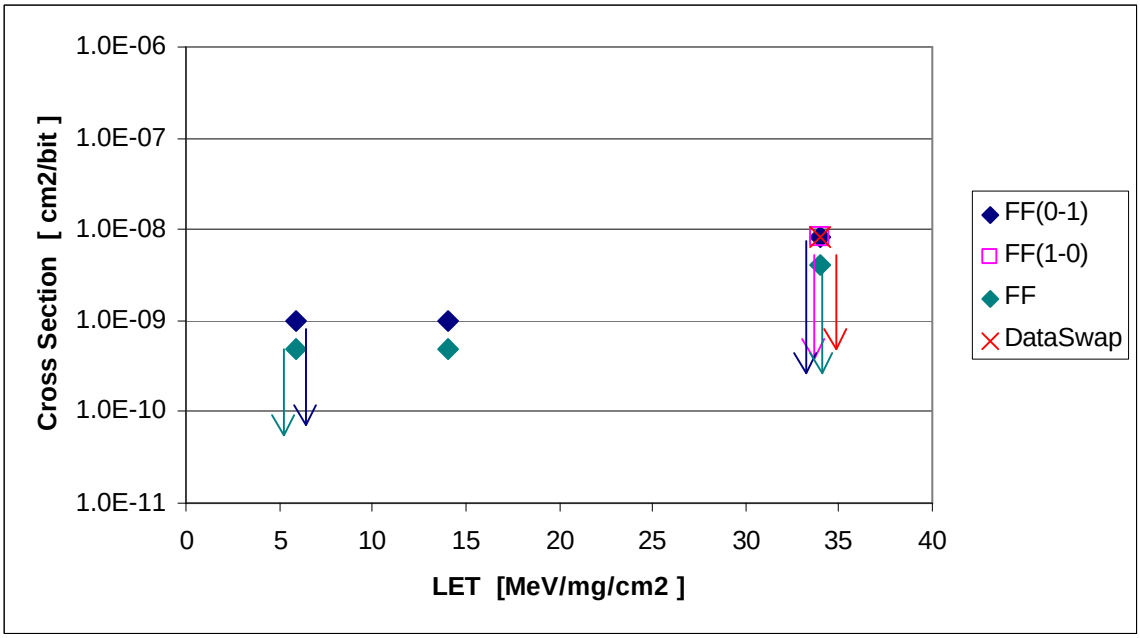

Figure 8.4 Register Errors of TMR Design. Arrows indicate test without any upsets.

Run#	**Ion [LET]**	**Error type**	**# of Bits tested**	**# of Errors**	**Flux** Ions/cm^2/s	**Fluence** Ions/cm^2	**Detection ratio**	**Cross Section** cm^2/bit
#15	Ar [14,1]				~1300	1,0e+6	1	
		FF(0-1)	1008	1				1,0e-9
		FF(1-0)	1008	0				<1,0e-9
		FF	2016	1				5,0e-10
		DataSwap	1008	0				<1,0e-9
#24	Ne [5,85]				~1300	1,0e+6	1	
		FF(0-1)	1008	0				<1,0e-9
		FF(1-0)	1008	0				<1,0e-9
		FF	2016	0				<5,0e-10
		DataSwap	1008	0				<1,0e-9
#27	N [2,97]				~2000	1,0e+6	1	
		FF(0-1)	1008	0				<1,0e-9
		FF(1-0)	1008	0				<1,0e-9
		FF	2016	0				<5,0e-10
		DataSwap	1008	0				<1,0e-9
#36	Kr [34]				~400	1,2e+5	1	
		FF(0-1)	1008	0				<8,3e-9
		FF(1-0)	1008	0				<8,3e-9
		FF	2016	0				<4,1e-9
		DataSwap	1008	0				<8,3e-9

9. CONCLUSION

9.1 Total Dose

Severe problems to initialise the devices were observed after 45 krad(Si) accumulated total dose. To overcome the problem, a slow power-up ramp was required with the possibility to deliver more current than specified (2-Ampere)

The results are in conflict with earlier total dose tests [2,4] that indicate total dose tolerance to about 100 krad(Si). However, no power cycling have been performed in earlier tests.
Parameter drift measurements indicated failures at about 80 krad(Si).

9.2 SEU

The SRAM based cells are sensitive for SEUs down to low LET values. With a Tipple Module Redundant Design in combination with fast correction of configuration data, the majority of all observed errors could be corrected. Errors in the control registers of the device cannot be corrected. The results from this test are shown in the figure below.

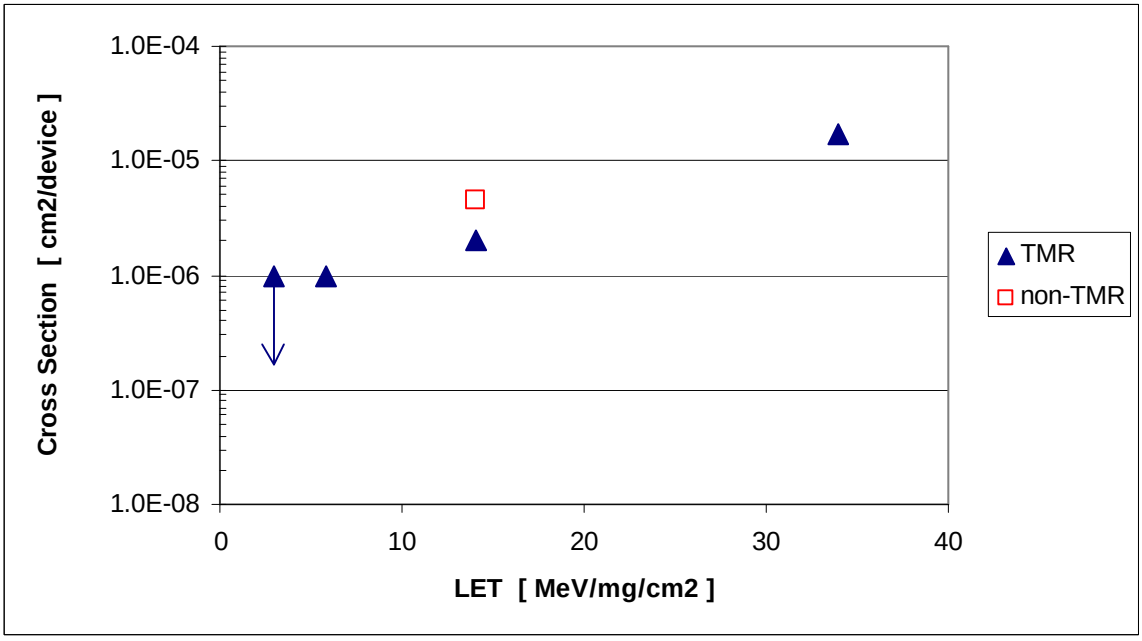

Figure 9.1 SEFI errors for non-TMR and TMR design. The non-TMR tests were performed to less fluence than the TMR, therefor less SEFI errors have been observed for non-TMR design. In principal the SEFI error cross section should be the same for the two designs. With the assumption the the control registers have the same heavy ion sensitivity as the user registers(Fig. 8.1), the number of fatal failure control bits of the device seem to be around ten. The LET threshold of the SEFI errors would with this assumption be around 5 MeV/mg/cm^2.

10. REFERENCES

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[2] Joe Fabula, Howard Bogrow, *Total Ionizing Dose Performance of SRAM-based FPGAs and supporting PROMs,* MAPLD 2000, October 2000.

[3] *Virtex™ 2.5 V Field Programmable Gate Arrays***,** Product Specification, DS003-2 (v2.6) July 19, 2001

[4] Earl Fuller, Michael Caffrey, Anthony Salazar, Carl Carmichael, Joe Fabula, *Radiation Characterization, and SEU Mitigation, of the Virtex FPGA for Space based Reconfigurable Computing,* NSREC 2000, October 2000.

[5] Carl Carmichael, Earl Fuller, Phil Blain, Michael Caffrey, *SEU Mitigation Techniques for Virtex FPGAs in Space Applications*. MAPLD 1999 Proceedings, September 1999.