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TITLE
Radiation Evaluation of Power-up Behaviour of Xilinx FPGA XQVR300

EUROPEAN SPACE AGENCY
CONTRACT REPORT

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SUMMARY

This total dose test on Xilinx Virtex XQVR300 has been performed to verify results observed in an earlier total dose test of this device type [1]. In that test an unexpected failure mode was observed, where the current use at power-up increased remarkably at a relatively low total dose level. The increased current use prevented the device to reach a power level high enough to initialise. After the test had been performed it was concluded that the power-up circuit didn't fulfil the specification for the device. The rise time of the power-up circuit was too fast.

In this test the power supplies have been reconstructed to fulfil the specification. The power-up ramp goes from 0 Volt to 2.5 Volt in 2-4 ms and it may deliver up to 2.5 Ampere. The aim of the present test was to confirm whether the results from last test were induced by the test method or not.

The power-up behaviour is studied for two devices in a number of total dose irradiation steps up to 95 krad(Si). The results are well in line with the earlier performed test. After a cumulated total dose of 45 krad(Si) both devices failed to power-up using a power-up ramp rate of 2 ms. By using a power-up ramp of 4 ms a cumulated dose of 55 krad(Si) was reached before first failure.

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TABLE OF CONTENTS		PAGE
1.	ABSTRACT	4
2.	INTRODUCTION	4
3.	<i>Vertex</i> XQVR300 DETAILS.....	5
3.1	TEST SAMPLES	5
4.	TEST EQUIPMENT.....	6
4.1	Test Boards.....	6
4.2	Power Supplies.....	7
5.	TOTAL DOSE TEST TECHNIQUES	9
5.1	Irradiation Steps	9
5.1.1	Test Conditions	9
5.2	DUT Design	10
5.2.1	Design for Functional Test.....	10
5.2.2	Design for Parameter Measurements.....	11
5.3	Parameter Measurements	12
6.	RESULTS	13
6.1	Supply Leakage Current.....	14
6.2	Details of Power-up Behaviour	15
6.3	Parameter Measurement Results	21
6.3.1	DC Parameters	21
6.3.2	Propagation Delays	22
7.	CONCLUSION.....	23
8.	REFERENCES	23



1. ABSTRACT

This total dose test on Xilinx Virtex XQVR300 has been performed to verify results observed in an earlier total dose test of this device type [1]. In that test an unexpected failure mode was observed, where the current use at power-up increased remarkably at a relatively low total dose level. The increased current use prevented the device to reach a power level high enough to initialise. In the earlier test this was first observed at 45 krad(Si) cumulated dose. After the test had been performed it was concluded that the power-up circuit didn't fulfil the specification for the device. The rise time of the power-up circuit was too fast.

In the present test the power supplies have been reconstructed to fulfil the specification. The power-up ramp goes from 0 Volt to 2.5 Volt in 2-4 ms and it may deliver up to 2.5 Ampere. The aim of the present test was to confirm whether the results from last test were induced by the test method or not.

The power-up behaviour is studied for two devices in a number of total dose irradiation steps up to 95 krad(Si). The results are well in line with the earlier performed test. After a cumulated total dose of 45 krad(Si) both devices failed to power-up using a power-up ramp rate of 2 ms. By using a power-up ramp of 4 ms a cumulated dose of 55 krad(Si) was reached before first failure.

2. INTRODUCTION

The Virtex FPGA is a very large and complex device. The power distribution to this kind of IC's may be a critical parameter for total dose radiation. In the data sheet [3] Xilinx have specified the power supply requirements to insure a successive initialisation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device from 0 V. The current is highest at the fastest suggested ramp rate, 2 ms (0 V to nominal voltage) and is lowest at the slowest allowed ramp rate, 50 ms. An industrial graded component requires 2 A on power-up.

In the earlier total dose test [1] a strong increase of current use during power-up was observed. This prevented the device to properly initialise. Such a total dose effect has not been reported in tests performed by Xilinx [2], [4]. The tests performed by Xilinx were not performed on programmed devices and the power was never cycled during irradiation.

In this new total dose test the power supply is constructed to fulfill Xilinx specification requirements.



3. Virtex XQVR300 DETAILS

The Virtex FPGA is an SRAM based device fabricated on thin-epitaxial silicon wafers using the commercial mask set and the Xilinx 0.22 μ CMOS process with 5 metal layers. Promising proton and heavy ion testing have been performed on the Virtex device and with mitigation techniques it may be a candidate for use in space applications.

3.1 TEST SAMPLES

The total dose test was performed on prototype devices delivered by Xilinx in a 240 pin plastic flat package. They origin from the same prototype LOT as earlier performed total dose test [1], [2], [4].

Two samples was tested, SN#41 and SN#42. A third device was used as a reference sample, REF#43.

Device Marking:

XILINX®
XQVR300™
PQ240AFT0125
DE11632/D3R2:01

The devices used in the previous total dose didn't have any device marking. The devices for the present test were delivered in a later shipment and the batch was marked after the first shipment.

The following information of process description is taken from a Total dose report presented by Xilinx at MAPLD2000 [2]:

Material: <1-0-0> 20ohm-cm p-type epitaxial layer on highly doped substrate
Gate Oxide: SiO₂, nominal 45/65A
Gate Width: 0.25/0.35 μ M defined
Isolation: Shallow Trench 7,500A nom
Foundry: UMC Group
Operating voltage: 2.5V

The configuration controller FPGA on the DUT board is controlling the PROMs and configuration ports of the DUTs. A program command can be sent to the DUT, which clears its configuration memory and starts an automatic re-configuration of the DUT from the PROM. During test the controlling FPGA can continuously scrub the DUT with new configuration data from the PROMs.

All data from the PROMs to the DUTs are transferred through the parallel SelectMAP interface, which supports the partial configuration feature making it possible to continuously scrub the device with new configuration data during operation.

4.2 Power Supplies

The power sources have been reconstructed to fulfil the requirements specified for the Virtex device (2-50ms rise time and 2A current). The power supply has an over current protection. If the current exceed $\sim 2,5A$ the power is turned off. After 20 ms the power is turned on again.

Two different setups were used for the power-up (Fig. 4.2). During irradiation a 15mF capacitor was connected to V_{CCINT} to give a rise time of about 4ms. Since the current is measured before the capacitor in the circuit, also the charge of the capacitor is added to the measured current at power-up (Fig. 4.3). In the measurements between the irradiation steps the capacitor were disconnected to test the worst case, 2ms-rise time.

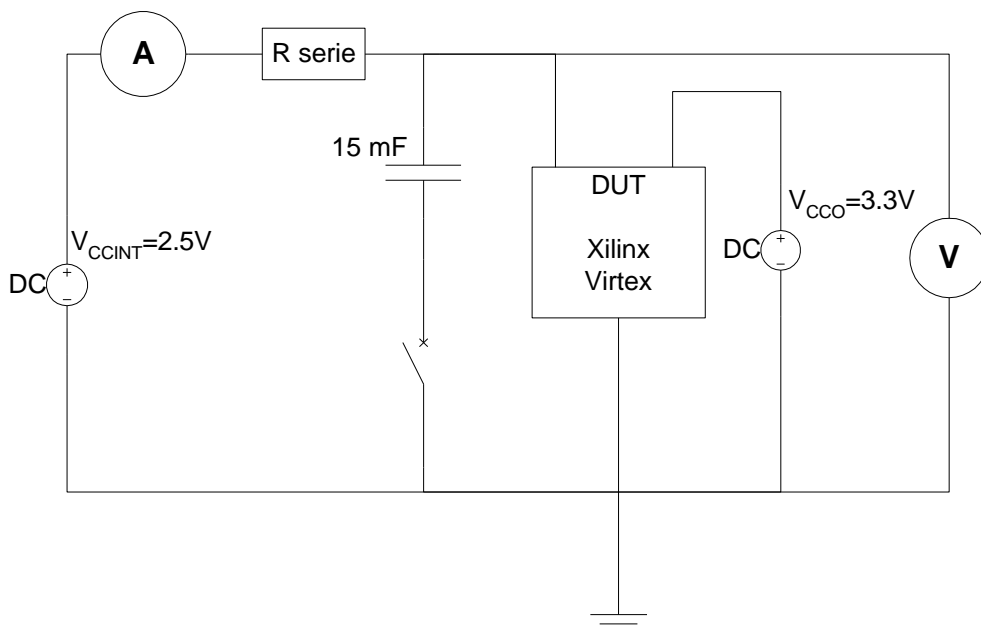


Figure 4.2 Principal drawing for power connection to the device under test (DUT). By connection the 15mF capacitor the power-up rise time increase from 2 to 4 ms.

By monitor the DONE signal from the Virtex device a successful power-up may be concluded. The Virtex device drains the pull-up DONE signal while it reads the configuration data from the configuration PROM. It release the DONE signal after the device is initialised and goes into operational mode. The configuration from the PROM takes about 10 ms. The DONE signal is monitored in the oscilloscope images in Fig. 4.3.

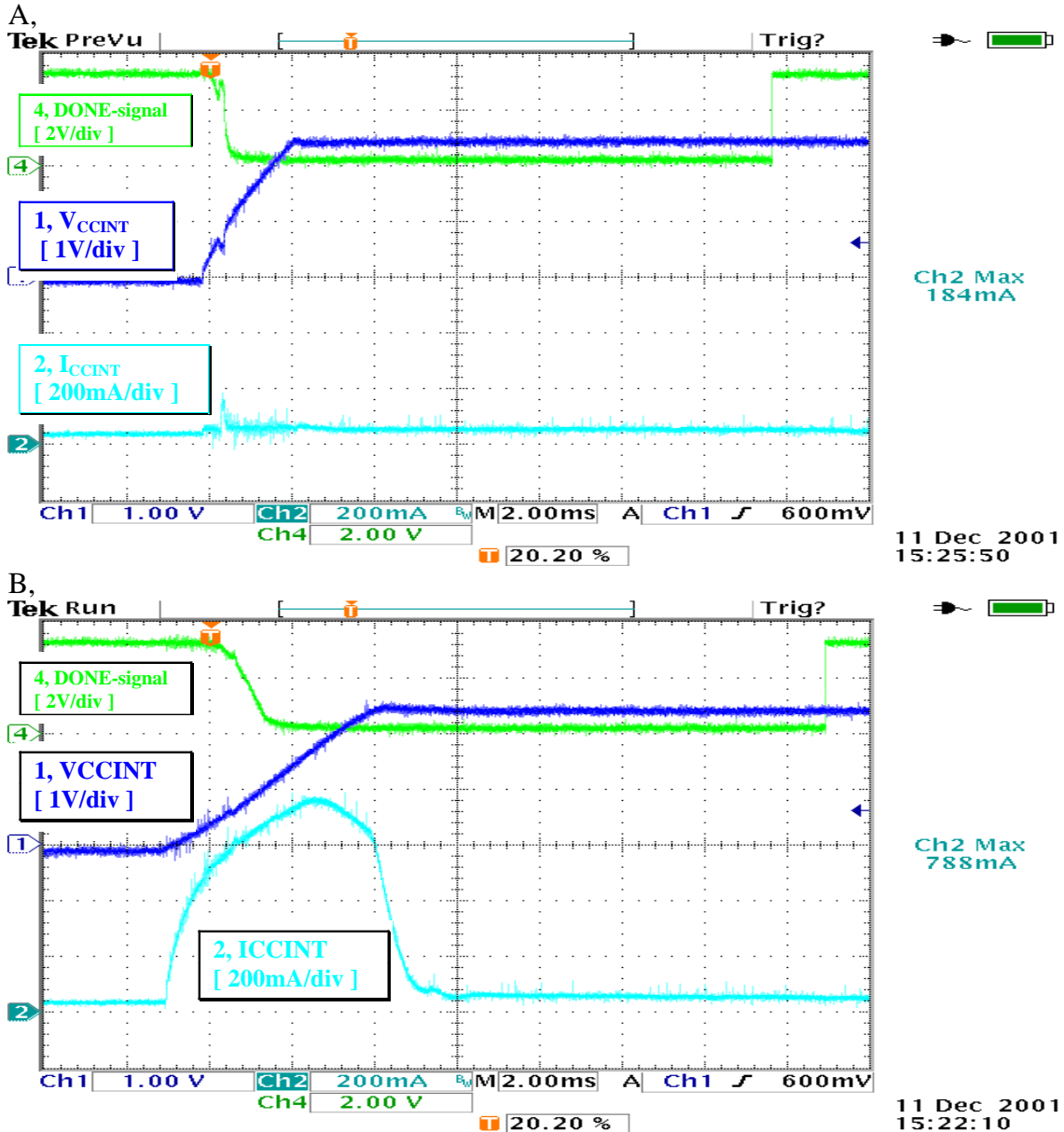


Figure 4.3 Pre Irradiation measurement of Power-up for SN#41 with (B) and without (A) the 15mF capacitor. The current (Ch2) is measured before the capacitor in the circuit.



5. TOTAL DOSE TEST TECHNIQUES

Total dose tests have been performed on 2 samples programmed with the *non-TMR* design described earlier [1]. During irradiation all devices were separately biased with $V_{CCO}=3.3V$ and $V_{CCINT}=2.5V$.

5.1 Irradiation Steps

The total dose tests were performed at the hospital of Borås. Irradiation up to 95 krad(Si) using a dose rate of 0,735 krad(Si)/h was performed in steps indicated in Table I. After each irradiation step the power-up behaviour were measured with oscilloscope. Both the 2 ms and the 4 ms power-up ramp were tested in each step. Before and after irradiation parameter measurements were performed on ~30 of all 208 available I/O pins. In-situ measurements of standby current were performed.

TABLE I
IRRADIATION STEPS

Step	Irradiation
0	Pre
1	25 krad(Si)
2	45 krad(Si)
3	75 krad(Si)
4	95 krad(Si)

5.1.1 Test Conditions

Two samples were static biased with power cycling and standby current measurement during irradiation. In the power cycling step the power to the device is turned off and on to test for the power-up problems. Bias conditions of user I/Os are described in 5.3.1. The configuration data were continuously updated (scrubbing) from the configuration PROM.

The samples were operated in a 1 hour test cycles

- One hour in static operation
- Power Cycling
 - Turn off V_{CCO} .
 - Wait 200 ms
 - Turn off V_{CCINT} .
 - Wait 10 s
 - Turn on V_{CCO} .
 - Wait 200 ms
 - Turn on V_{CCINT} with 4 ms ramp.

5.2 DUT Design

The DUT design is the same that we used in the earlier test [1] (denoted “Non-TMR”). It is made up of two parts, one part for functional test by the controller board and one part for parameter measurements.

5.2.1 Design for Functional Test

The part for functional test, shown in Fig. 5.2.1, implements 14 pipelined shift register each 144 bit long and a small self-test circuit. Individual register bits are build up of a D-type CLB flip-flop modules [3]. All together, 32% of the available CLB flip-flop resources in the Virtex device have been used.

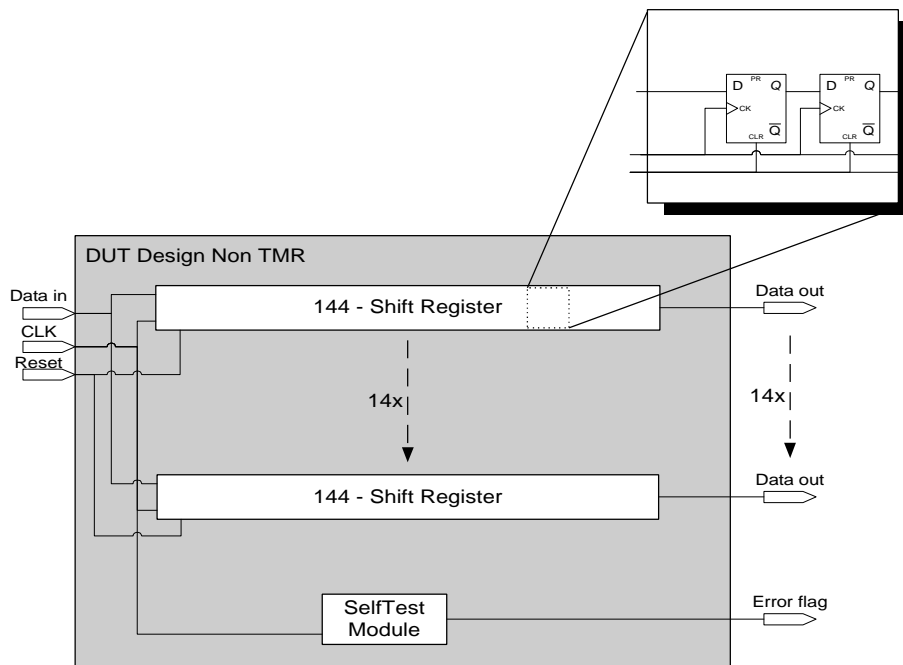


Figure 5.2.1 Principal Drawing of part used for functional test in the Non-TMR DUT Design.

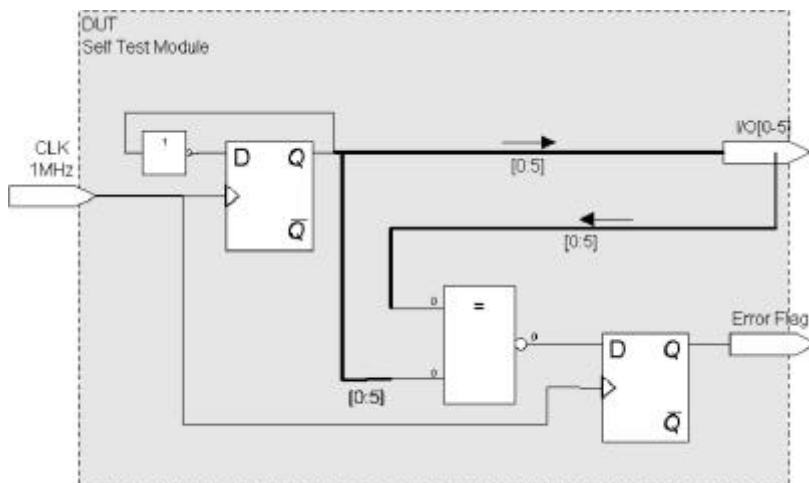


Figure 5.2.2 Principal Drawing of SelfTest Module



The principal of the self test circuit, shown in Fig. 5.2.2, is that data are compared with itself and any mismatch is reported to an output (Error flag). Data are a 6-bit word taking two different paths in the design before comparison. One path goes through 6 I/O modules of the device and then back to the comparator. The other path goes directly to the comparator. A feed back flip-flop register with the external clock signal generates the data. This give toggling data with half the frequency of the clock signal.

5.2.2 Design for Parameter Measurements

One small part of the device has been designed for parameter testing. Twelve binning circuits are connected from inputs to outputs of the device. They are of three different types, four of each. One type (BUF) has 50 buffer cells in-line between in- and outputs, one type (INV) has 50 inverter cells in-line between in- and outputs and one type (DIR) is direct connected. All user I/Os was selected in the design as LVTTTL.

The inputs to the binning circuits can be in two different states during irradiation,

- 1 kΩ connected to Vcc=3,3V
- 1 kΩ connected to GND

All cells in the binning circuits were either static high or static low during irradiation.

Outputs of the binning circuits can be in two different states during irradiation,

- static high with 1kΩ load to GND
- static low with 1kΩ load to Vcc=3,3V

The data outputs from the Self-test circuit were not connected on the DUT board and was not toggled during irradiation.

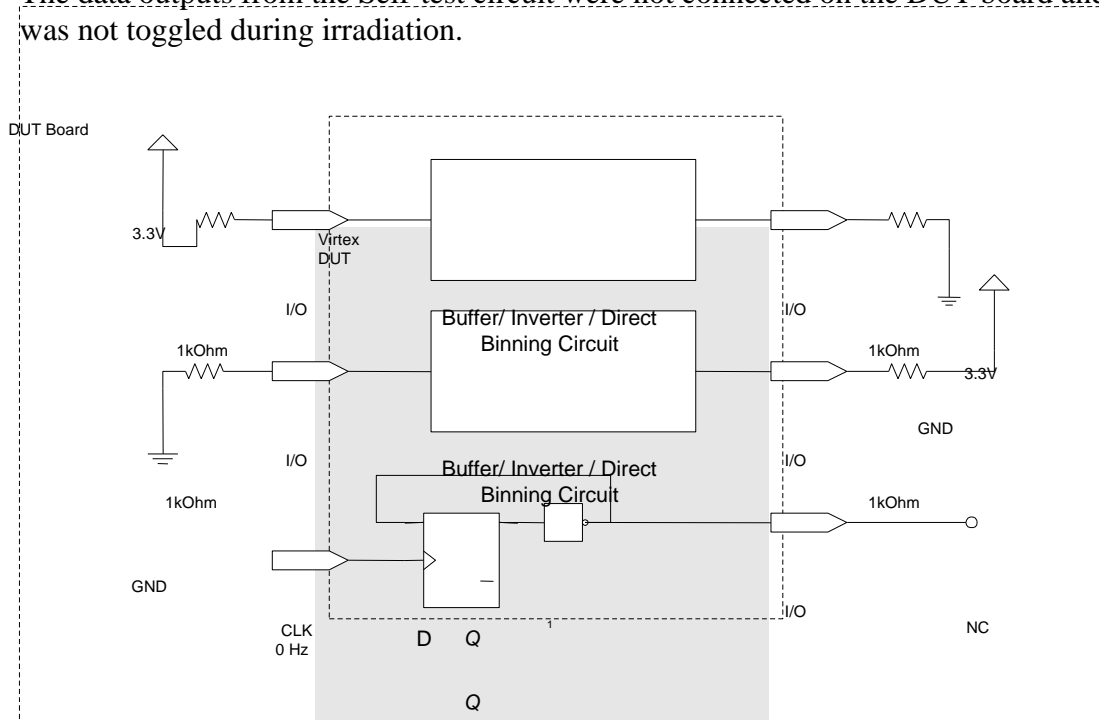




Figure 5.2.1 Principal drawing for configuration of I/Os during irradiation.

5.3 Parameter Measurements

Pre- and post-irradiation electrical measurements have been performed on the parameters listed in Table II using normal bias condition with $V_{CCINT}=2.5V$ and $V_{CCO}=3.3V$. All measurements were performed with SE's component tester, SZ M3000.

TABLE II
ELECTRICAL PARAMETERS AND CONDITIONS

Parameter	Conditions	Low Limit*	High Limit*
I_{IL}	$V_{IN} = GND$ $V_{CCINT} = 2.5V$ $V_{CCO} = 3.3V$	-10 μA	10 μA
I_{IH}	$V_{IN} = V_{CCI}$ $V_{CCINT} = 2.5V$ $V_{CCO} = 3.3V$	-10 μA	10 μA
V_{OL}	$I_{OL} = 24mA$ (LVTTL) $V_{CCINT} = 2.5V$ $V_{CCO} = 3.3V$	-	0.4V
V_{OH}	$I_{OH} = - 24mA$ (LVTTL) $V_{CCINT} = 2.5V$ $V_{CCO} = 3.3V$	2.4V	V_{CCO}
I_{OZL}	$V_{IN} = GND$ Output disabled $V_{CCINT} = 2.5V$ $V_{CCO} = 3.3V$	-10 μA	10 μA
I_{OZH}	$V_{IN} = V_{CCI}$ Output disabled $V_{CCINT} = 2.5V$ $V_{CCO} = 3.3V$	-10 μA	10 μA
Propagation Delays	$V_{CCINT} = 2.5V$ $V_{CCO} = 3.3V$		

* The limits are specified by Xilinx for worst case bias conditions.

Positive and negative propagation delays were measured from input to output of the binning circuits. DC parameter measurement was performed on all in- and outputs of the binning circuits and on the six data outputs from the Self test circuit.



6. RESULTS

The total dose test performed normal up the 2nd irradiation step (45 krad). At this point the 2 ms power-up ramp failed to initialise both devices. Normal initialisation was achieved for the 4 ms power-up ramp.

The first initialisation failure of the 4 ms power-up ramp was observed in power cycling steps during irradiation after 55 krad(Si) for SN#42 and after 65 krad(Si) for SN#41.

In the power cycling step when the power was turned on, the over current protection circuit was activated. The power was turned off and a new try to turn on the power was automatically performed. This was repeated until the power-up succeeded without activating the over current protection circuit. The time to have a successful power-up after each power cycling varied between a few minutes up to the time for the next power cycle (one hour).

All devices were irradiated up to 95 krad(Si) cumulated dose. The bias conditions were normal up to 55 krad(Si) for SN#42 and 65 krad(Si) for SN#41. Thereafter, SN#41 was in normal bias condition for 30% of the time, un-biased for 45% of the time and in power-up phase for 25% of the time. SN#42 was biased normally 50% of the time, un-biased 33% of the time and during power-up 17% of the time.

Before the power-up problems started both devices were in normal biased conditions 99% of the time during irradiation.



6.1 Supply Leakage Current

No supply current increase was observed (except increase related to power-up failure) for any devices up to 60 krad(Si). This is well in line with earlier performed total dose testing [1], [2], [4].

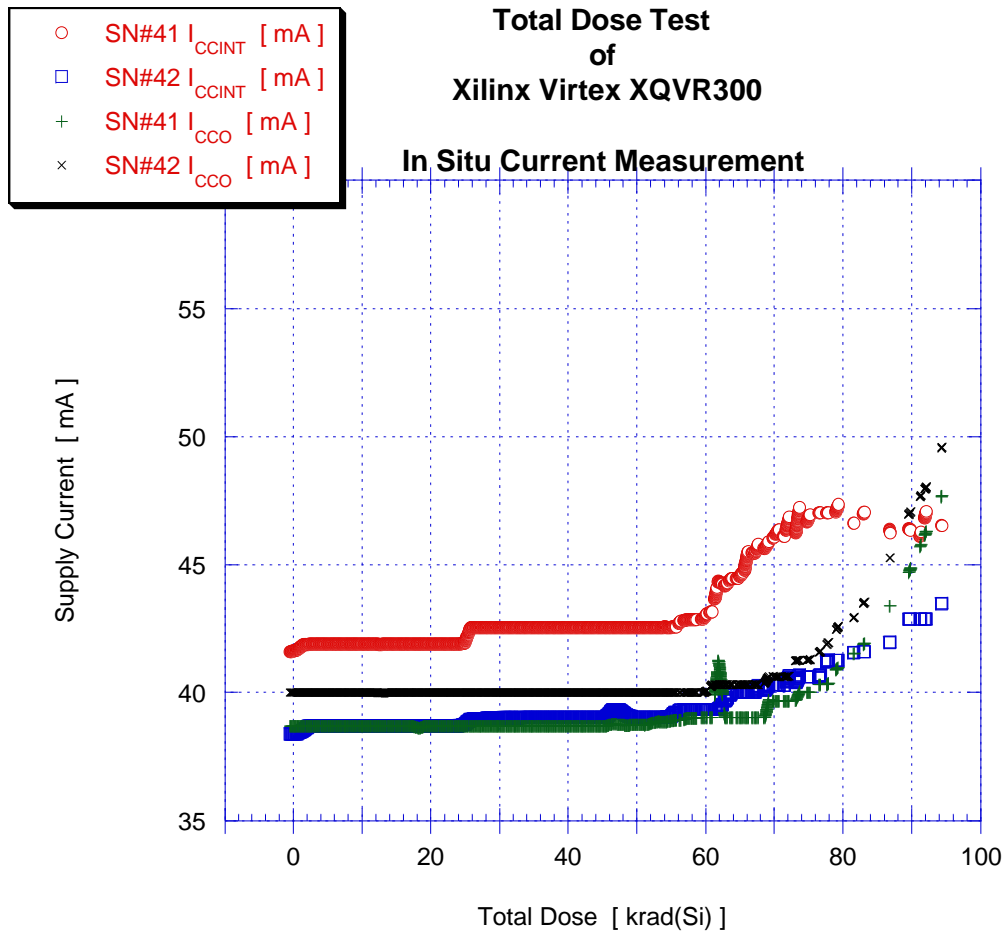


Figure 6.1 Supply current values during irradiation for SN #41 and #42. I_{CCO} is the supply current for the I/Os with $V_{CCO}=3.3V$. I_{CCINT} is the supply current for the internal logic with $V_{CCINT}=2.5V$. Measurements were taken every 10^{th} second. After start of power-up problem, 55 krad(Si) and 65 krad(Si), all abnormal measurement values have been excluded until the devices were back at normal power after each power cycling. The supply current starts to increase after about 60 krad(Si) for both devices.

6.2 Details of Power-up Behaviour

Figures 6.4-6.12 show the voltage (V_{CCINT}) and current (I_{CCINT}) during power-up for all irradiation steps. After the 1st irradiation step (25 krad) the current use in the power-up phase had slightly decreased. After the 2nd irradiation step (45krad) the current at power-up had increased remarkably for both irradiated devices. The current peak increased both in amplitude and width. With 2 ms rise time both devices failed to power-up, but with 4 ms rise time both succeeded. After the 3rd and the last irradiation step (75 and 95 krad) none of the devices succeeded to power-up, neither with 2 or 4 ms rise time.

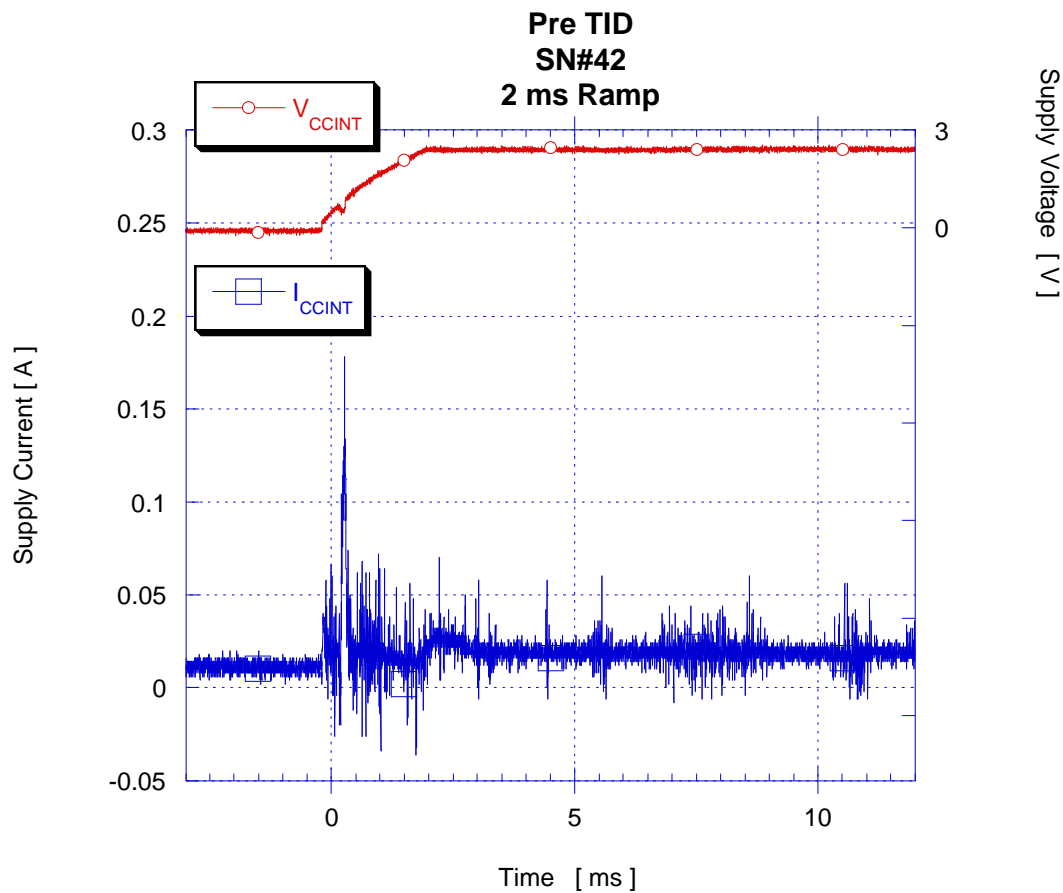


Figure 6.2 Voltage and current measurement for SN#42 before irradiation. The measurement is taken with oscilloscope during power-up with the 2 ms-ramp. The current peak observed during the ramp-up of the voltage is according to specification [3].

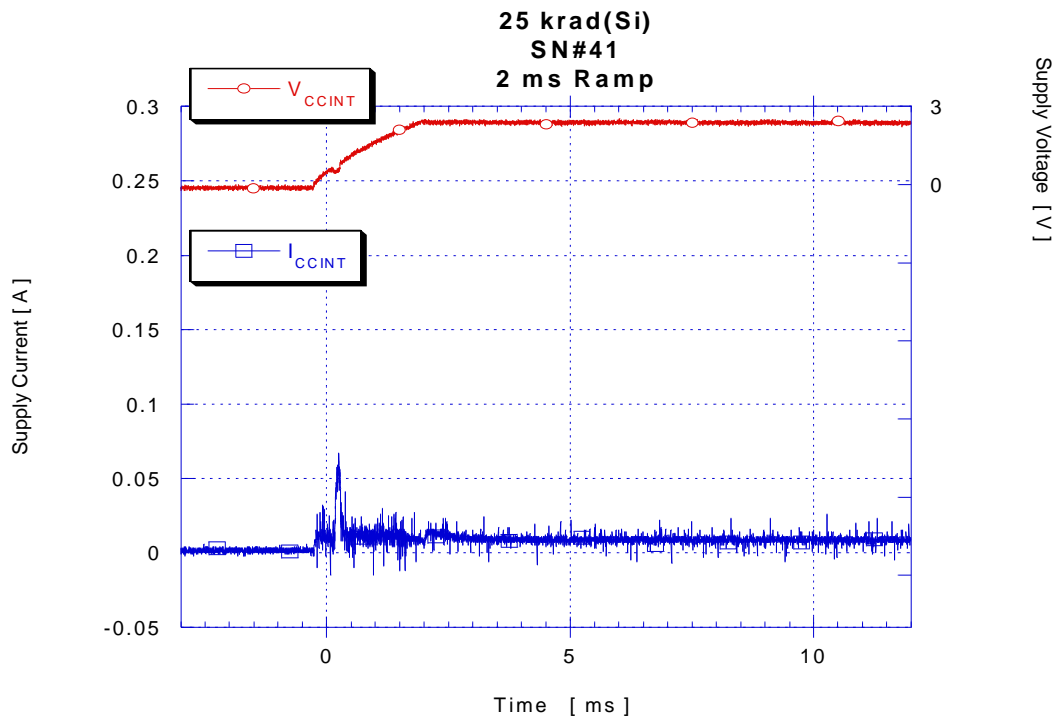


Figure 6.3 Voltage and current measurement for SN#41 after the 1st irradiation step (25 krad). The measurement is taken with oscilloscope during power-up with the 2 ms-ramp. The current peak has decreased from the pre-irradiation measurement.

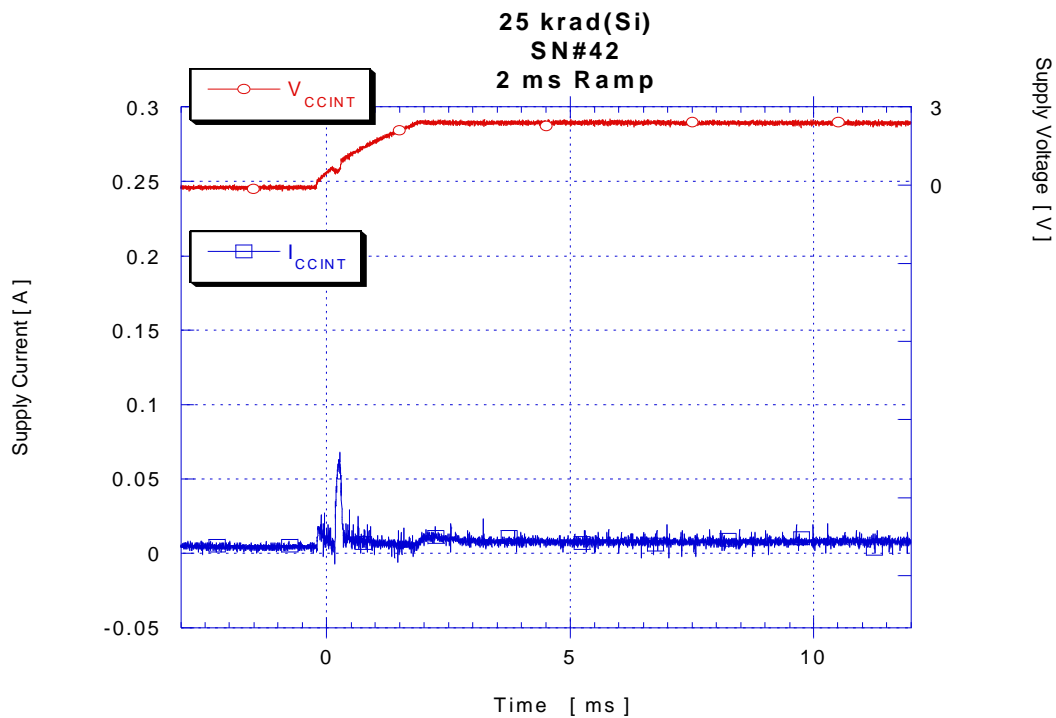
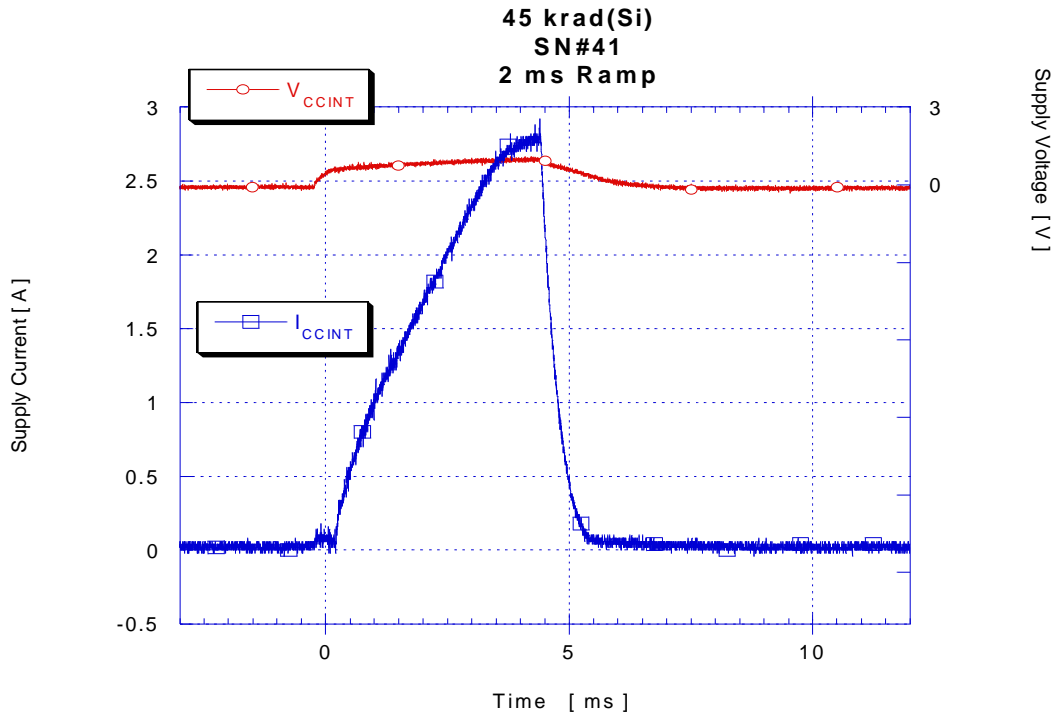


Figure 6.4 Voltage and current measurement for SN#42 after the 1st irradiation step (25 krad). The measurement is taken with oscilloscope during power-up with the 2 ms-ramp. The current peak has decreased from the pre-irradiation measurement.

A,



B,

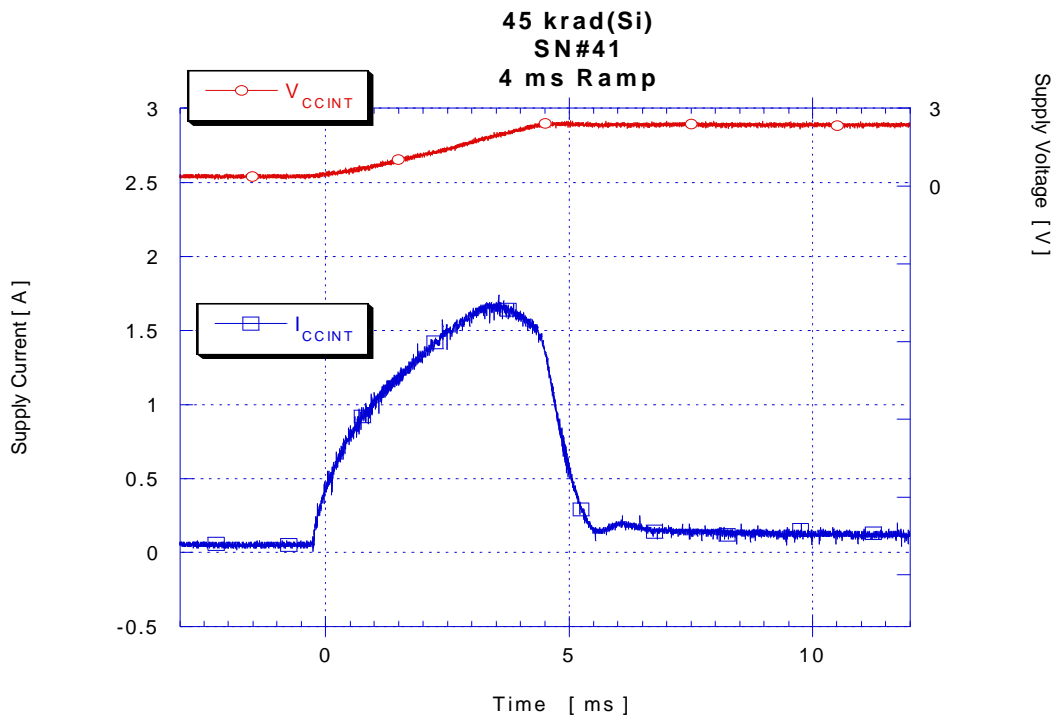
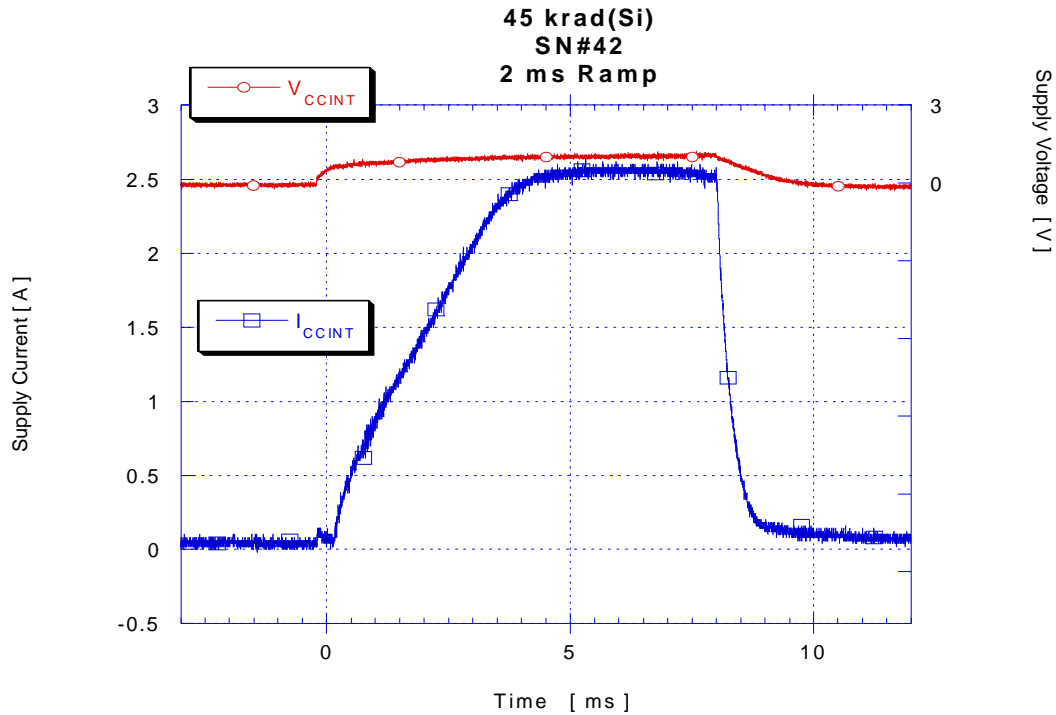


Figure 6.5 Voltage and current measurement for SN#41 after the 2nd irradiation step (45 krad). The measurements are taken with oscilloscope during power-up with the 2 ms-ramp (A) and the 4 ms-ramp (B). The over current protection circuit turns off the power (A). By increasing the rise time (B) the device used less current in the power-up phase and the power-up succeeded.

A,



B,

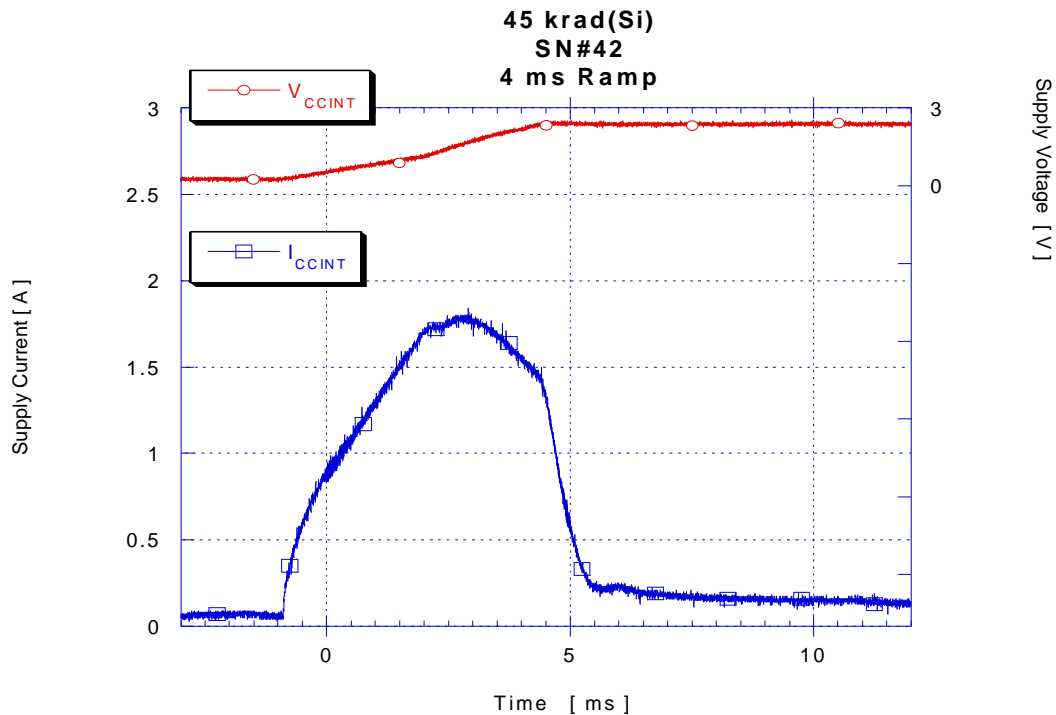


Figure 6.6 Voltage and current measurement for SN#42 after the 2nd irradiation step (45 krad). The measurements are taken with oscilloscope during power-up with the 2 ms-ramp (A) and the 4 ms-ramp (B). The over current protection circuit turns off the power (A). By increasing the rise time (B) the device used less current in the power-up phase and the power-up succeeded. The over current protection circuit for SN#41 is slightly slower than for SN#41. When reaching the maximum current (2.5 A) it takes some microseconds before the power is turned off.

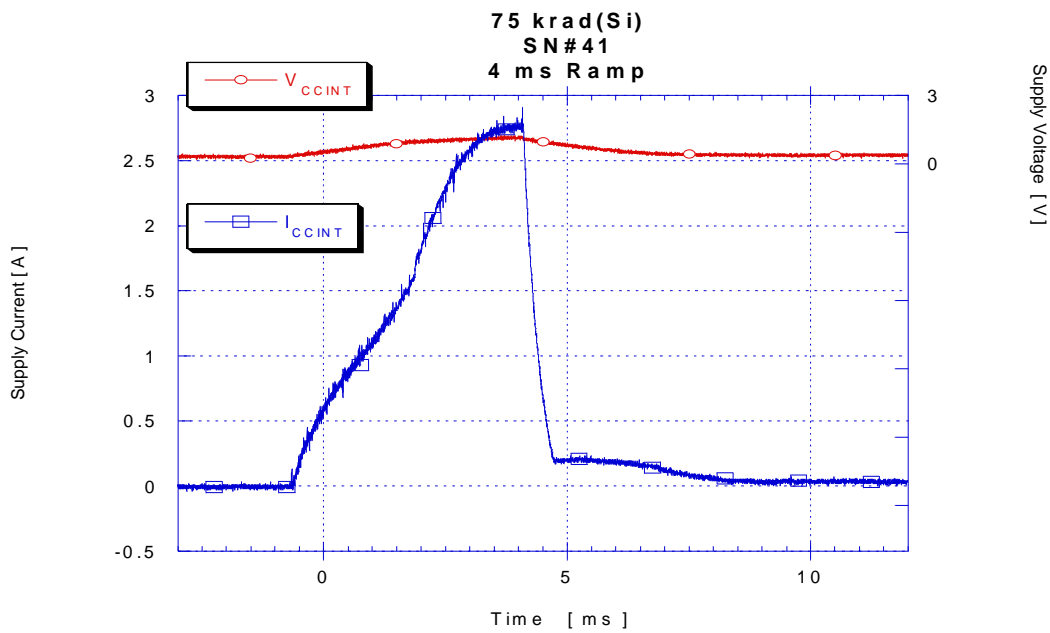


Figure 6.7 Voltage and current measurement for SN#41 after the 3rd irradiation step (75 krad). The measurement is taken with oscilloscope during power-up with the 4 ms-ramp. Both with the 2 ms- and 4 ms ramp the power-up failed.

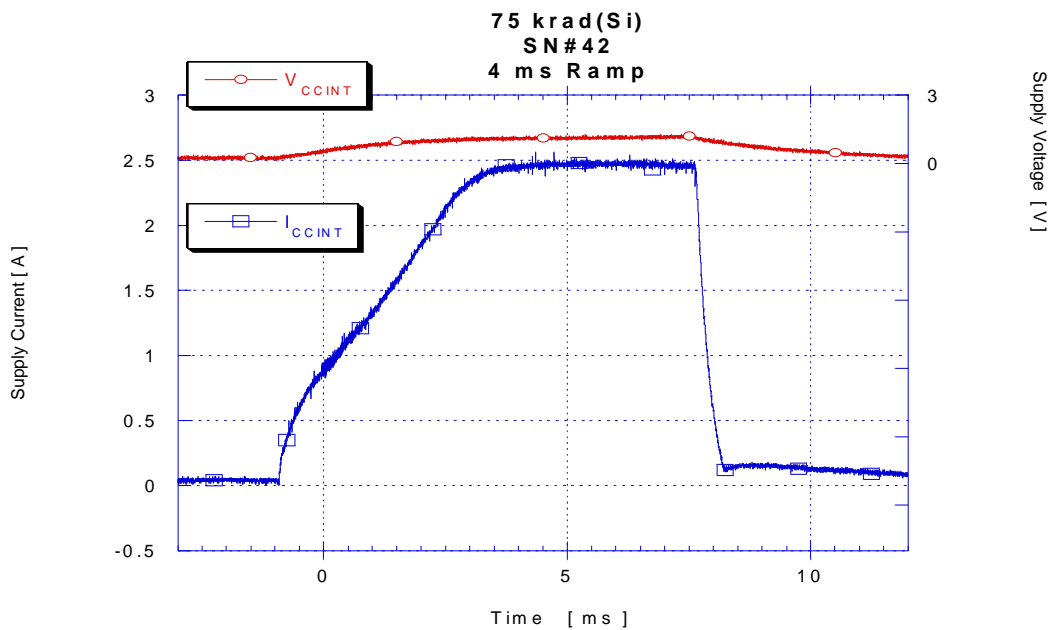


Figure 6.8 Voltage and current measurement for SN#42 after the 3rd irradiation step (75 krad). The measurement is taken with oscilloscope during power-up with the 4 ms-ramp. Both with the 2 ms- and 4 ms ramp the power-up failed. The over current protection circuit for SN#42 is slightly slower than for SN#41. When reaching the maximum current (2.5 A) it takes some microseconds before the power is turned off.

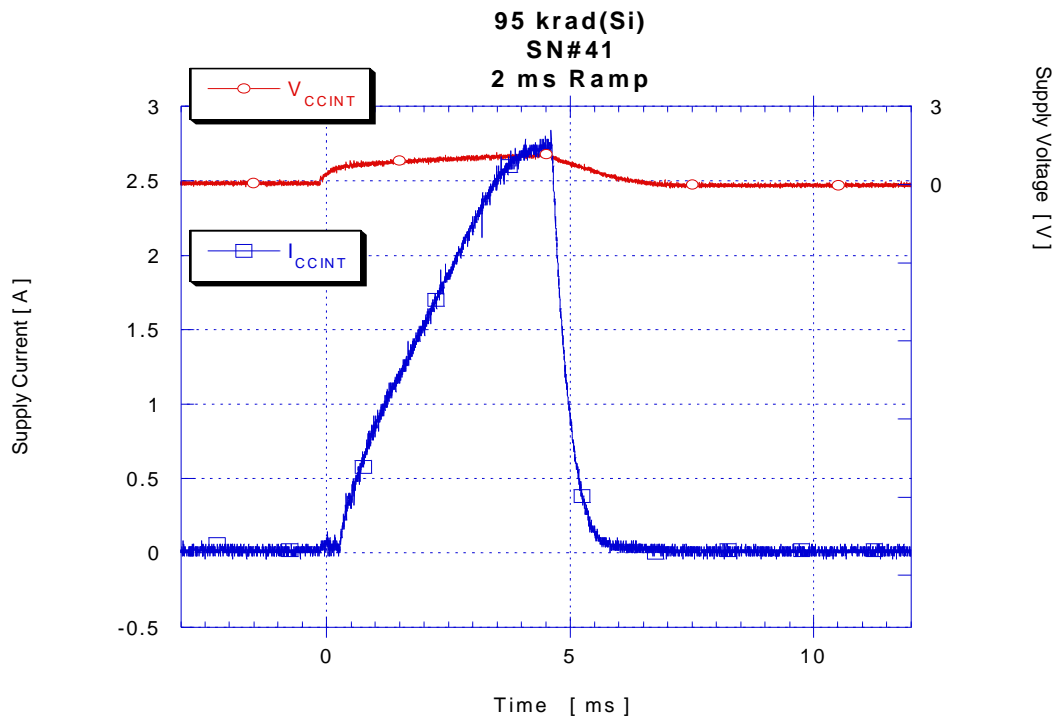


Figure 6.9 Voltage and current measurement for SN#41 after the last irradiation step (95 krad). The measurement is taken with oscilloscope during power-up with the 2 ms-ramp. Both with the 2 ms- and 4 ms ramp the power-up failed.

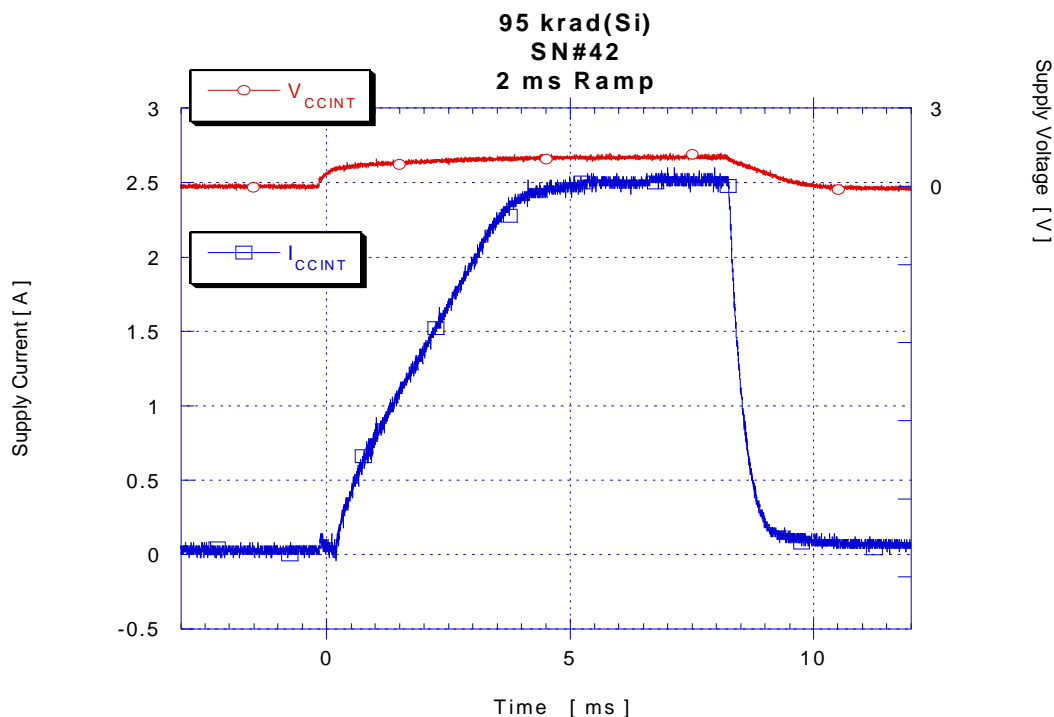


Figure 6.10 Voltage and current measurement for SN#42 after the last irradiation step (95 krad). The measurement is taken with oscilloscope during power-up with the 2 ms-ramp. Both with the 2 ms- and 4 ms ramp the power-up failed. The over current protection circuit for SN#42 is slightly slower than for SN#41. When reaching the maximum current (2.5 A) it takes some microseconds before the power is turned off.



6.3 Parameter Measurement Results

Pre- and post -parameter measurements were performed. In the in-situ supply current measurements (Fig. 6.1) it can be seen that the change in bias conditions after 55 and 65 krad(Si) affect the total dose response of the devices. Therefore, it is likely to believe that a total dose test with the devices in normal biased condition 100% of the time would have resulted in larger degradation of the parameter values than those presented below.

6.3.1 DC Parameters

A summary of the results of the DC parameter measurement is presented in Table III. The only parameter that shows any significant damage after irradiation is the output high leakage current. A graph is presented in Fig. 6.11.

TABLE III
SUMMARY OF DC PARAMETER MEASUREMENTS.

DC Parameter	Device	Pre Irradiation Measurement [mA]	Post Irradiation Measurement [mA]	Specification Limit
I _{IH}	SN#41	1.90	4.44	10 μA
	SN#42	2.11	4.12	
	REF#43	2.20	2.00	
I _{IL}	SN#41	0.0413	-0.0206	10 μA
	SN#42	0.0431	-0.0156	
	REF#43	0.0438	0.0356	
I _{OZH}	SN#41	1.48	21.5	10 μA
	SN#42	2.13	20.0	
	REF#43	1.7	1.7	
I _{OZL}	SN#41	0.0447	0.0276	10 μA
	SN#42	0.0424	0.0176	
	REF#43	0.0441	0.0294	
V _{OH}	SN#41	2.74	2.72	2.4 V
	SN#42	2.73	2.73	
	REF#43	2.72	2.73	
V _{OL}	SN#41	0.374	0.371	0.4 V
	SN#42	0.372	0.370	
	REF#43	0.368	0.374	

All data are mean values over all measured I/Os for each device.

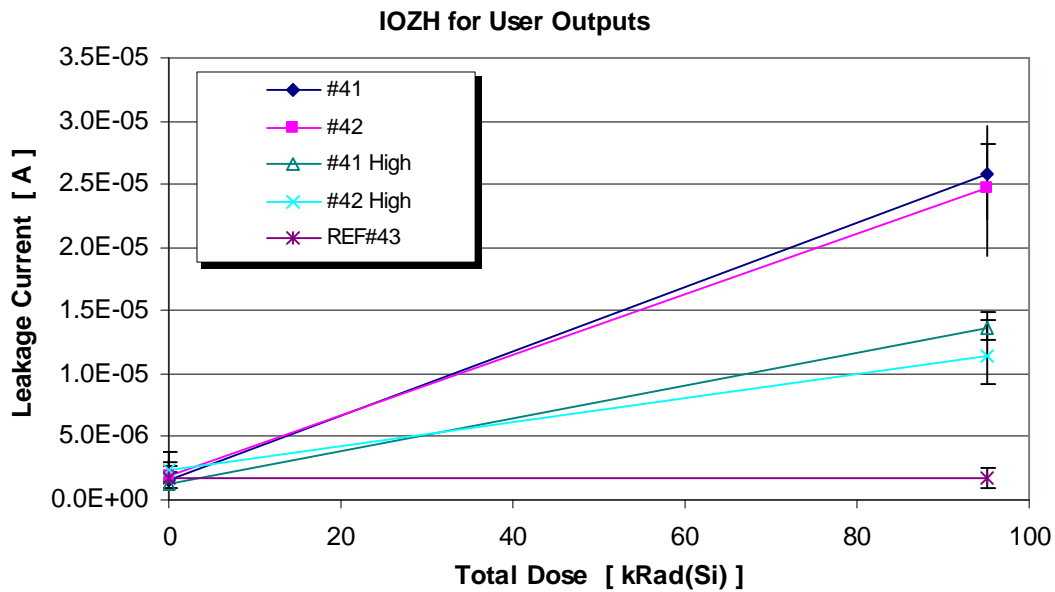


Figure 6.11 Pre- and post irradiation measurements of the output leakage high current for user I/Os. User outputs that were driven high during irradiation are presented as separate data points. Specification limit is 1×10^{-5} A. The data points are mean values for measured I/O's and the error bars indicate min- and max measured values.

6.3.2 Propagation Delays

Positive and negative pulse delays have been measured for the 12 binning circuits designed into the DUT. The resolution for positive pulses is 1 ns and negative pulses 5 ns. No significant changes in timings have been observed.

TABLE IV
AVERAGE OF POSITIVE TIME DELAYS

Binning *	Part#	0 krad(Si) [ns]	95 krad(Si) [ns]
DIR	#41	11.5	10.75
	#42	11.75	11.25
	REF#43	11.75	11.5
INV	#41	65.75	65.75
	#42	67.5	66.75
	REF#43	67.75	68
BUF	#41	63.5	63
	#42	65.25	64.5
	REF#43	65.5	65.5

Table V
AVERAGE OF NEGATIVE TIME DELAYS

Binning *	Part#	0 krad(Si) [ns]	95 krad(Si) [ns]
DIR	#41	11.25	11.25
	#42	12.5	11.25
	REF#43	12.5	10
INV	#41	65	65
	#42	67.5	67.5
	REF#43	67.5	66.25
BUF	#41	63.75	61.25
	#42	66.25	65
	REF#43	66.25	65

* See paragraph 5.2.2 for a description of the binning circuits.



7. CONCLUSION

Parameter drift, supply leakage current and time delay measurements indicate small drifts after irradiation. The critical parameter is the current peak at power-up.

After 45 krad(Si) accumulated total dose severe problems to initialise the devices were indicated. It was observed that the current peak in the power-up phase strongly increased in width and amplitude with cumulated total dose. The results are well in line with what was observed in the earlier performed total dose test [1]. The two tested power-up ramps indicate that a higher total dose tolerance could be achieved with a slower power-up ramp. Xilinx allow up to 50 ms power-up ramp.

The present results are in conflict with earlier total dose tests performed by Xilinx [2,4] where total dose tolerance to about 100 krad(Si) have been reported. These tests have, however, been performed on blank devices with no power cycling during irradiations.

8. REFERENCES

- [1] "Radiation Pre-Evaluation of FPGA Xilinx Virtex XQVR300," ESA contract report, ref. ESA_QCA0109TS_C, Aug. 2001.
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- [3] Xilinx Product Specification, *Virtex™ 2.5 V field programmable gate arrays*, DS003-2 (v2.6) Jul. 2001
- [4] Earl Fuller, Michael Caffrey, Anthony Salazar, Carl Carmichael and Joe Fabula, "Radiation characterization, and SEU mitigation, of the Virtex FPGA for space based reconfigurable computing," NSREC 2000, Oct. 2000.