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TRANSISTORS, MOSFET, POWER, P-CHANNEL,

BASED ON TYPES IRFY9120, IRFY9130,

IRFY9140 AND IRFY9240

ESA/SCC Detail Specification No. 5206/005

space components
coordination group

Issue/Rev.	Date	Approved by	
		SCCG Chairman	ESA Director General or his Deputy
Issue 1	November 1994		

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference	CHANGE Item	Approved DCR No.

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APPENDICES (Applicable to specific Manufacturers only)

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for Transistors, MOSFET, Power, P-Channel, based on Types IRFY9120, IRFY9130, IRFY9140 and IRFY9240. It shall be read in conjunction with ESA/SCC Generic Specification No. 5000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type transistors specified herein, which are also covered by this specification, are listed in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the transistors specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The parameter derating information applicable to the transistors specified herein is shown in Figure 1(a).

The safe operating area information applicable to the transistors specified herein is shown in Figure 1(b).

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the transistors specified herein are shown in Figure 2.

1.6 FUNCTIONAL DIAGRAM

The functional diagram, showing lead identification, of the transistors specified herein, is shown in Figure 3.

1.7 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be taken for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1, with a Minimum Critical Path Failure Voltage of 1000Volts.

TABLE 1(a) - TYPE VARIANTS

VARIANT	(1) LEAD MATERIAL AND FINISH	(2) BASED ON TYPE	(3) V_{DS} (MAX.) (V)	(4) I_D (MAX.) (NOTE 1) (A)	(5) I_D (MAX.) (NOTE 2) (A)	(6) I_S (NOTE 1) (A)	(7) V_{DS} (80%) (V)	(8) I_{DM} (MAX.) (Apk)	(9) V_{DG} (V)	(10) P_{tot} (NOTE 1) (W)	(11) $R_{TH(J-C)}$ (°C/W)	(12) E_{AS} (mJ)
01	H4	IRFY9120	−100	−5.3	−3.4	−5.3	−80	−21.2	−100	30	4.1	22.5
02	H4	IRFY9130	−100	−9.3	−5.8	−9.3	−80	−37.2	−100	45	2.8	26.5
03	H4	IRFY9140	−100	−13	−8.2	−13	−80	−52	−100	60	2.1	100.2
04	H4	IRFY9240	−200	−7.7	−4.8	−7.7	−160	−30.8	−200	60	2.1	300

NOTES
1. At T_{case} = +25°C.
2. At T_{case} = +100°C.

TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Drain Source Voltage	V_{DS}	Table 1(a) Column 3	V	
2	Gate Source Voltage	V_{GS}	±20	V	
3	Drain Gate Voltage	V_{DG}	Table 1(a) Column 9	V	
4	Drain Current (Continuous)	I_D	Table 1(a) Column 4	A	At T_{case} = +25°C Note 1
5	Drain Current (Continuous)	I_D	Table 1(a) Column 5	A	At T_{case} = +100°C Note 1
6	Source Current (Continuous)	I_S	Table 1(a) Column 6	A	At T_{case} = +25°C Note 1
7	Drain Current Pulsed (Peak)	I_{DM}	Table 1(a) Column 8	Apk	
8	Total Power Dissipation	P_{tot}	Table 1(a) Column 10	W	Note 2
9	Operating Temperature Range	T_{op}	−55 to +150	°C	T_{amb}
10	Storage Temperature Range	T_{stg}	−55 to +150	°C	
11	Soldering Temperature	T_{sol}	+300	°C	Note 3
12	Thermal Resistance (Junction to Case)	$R_{TH(J-C)}$	Table 1(a) Column 11	°C/W	
13	Avalanche Energy	E_{AS}	Table 1(a) Column 12	mJ	

NOTES

1. For T_{case} > +25°C, derate as follows:-

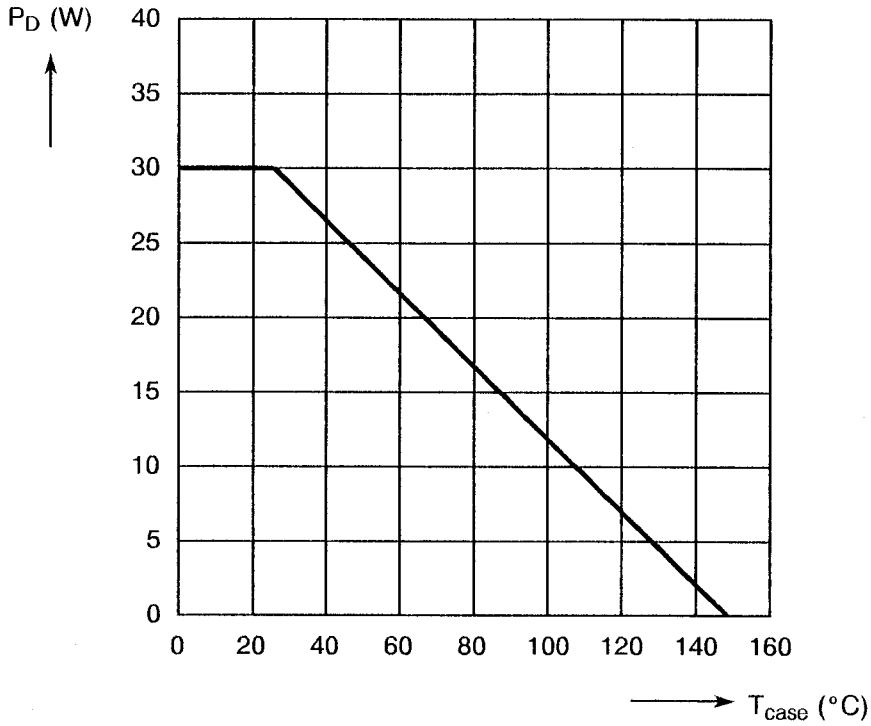
   $I_D = \sqrt{\frac{P(rated)}{K}}$ where: $P(rated) = P_{tot} - (T_{case} - 25)P_{tot}/125$.
   K = rated $r_{DS(ON)}$ at T_J = +150°C.

2. At $T_{case} \leq$ +25°C. For derating at T_{case} > +25°C, see Figure 1(a).

3. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

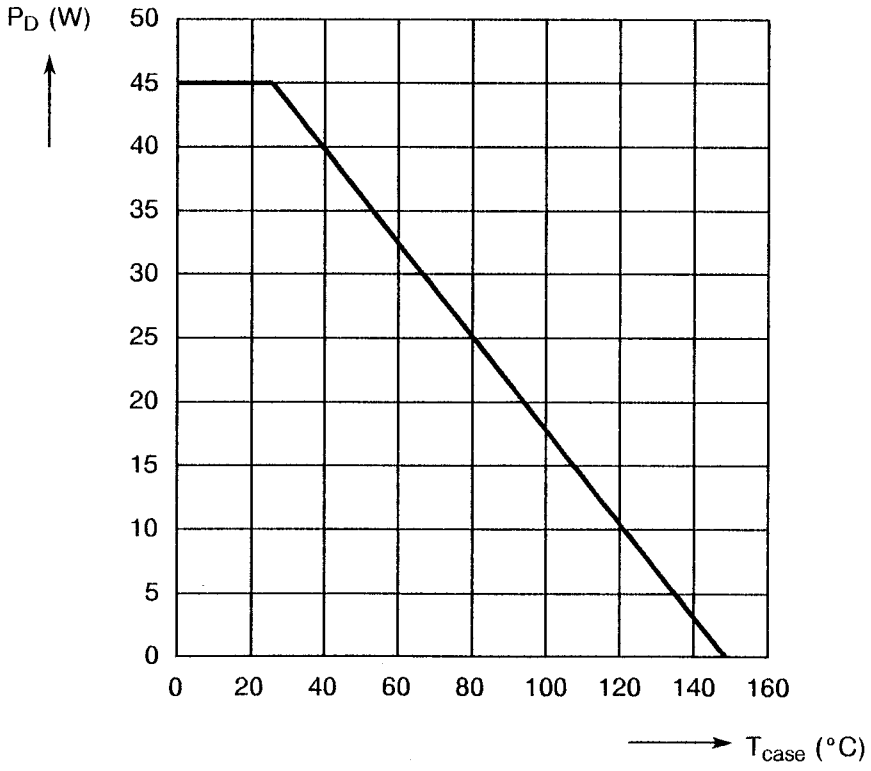
FIGURE 1(a) - PARAMETER DERATING INFORMATION

VARIANT 01



Power Dissipation versus Temperature

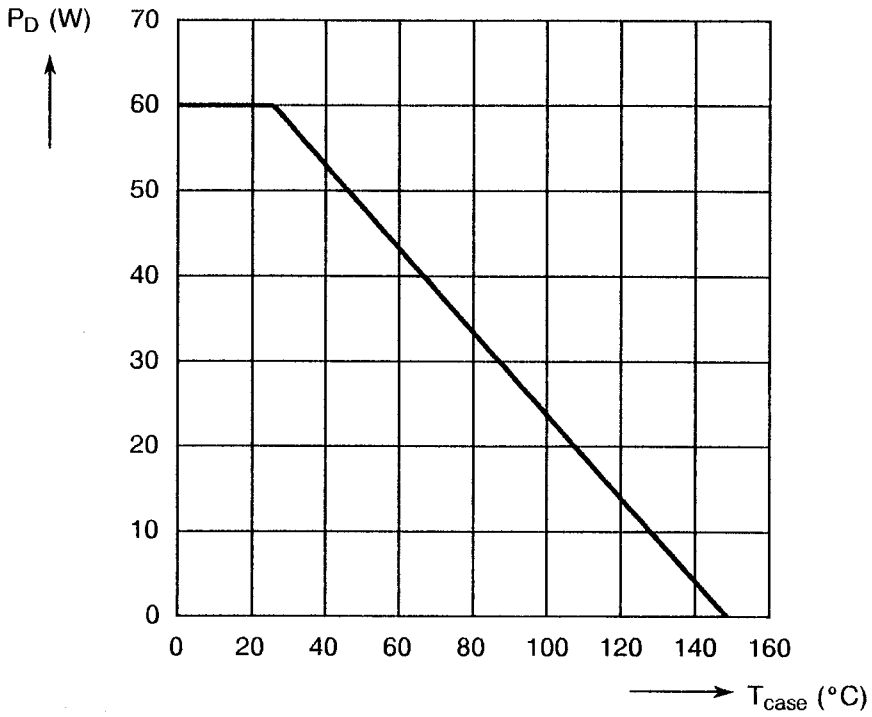
VARIANT 02



Power Dissipation versus Temperature

FIGURE 1(a) - PARAMETER DERATING INFORMATION (CONTINUED)

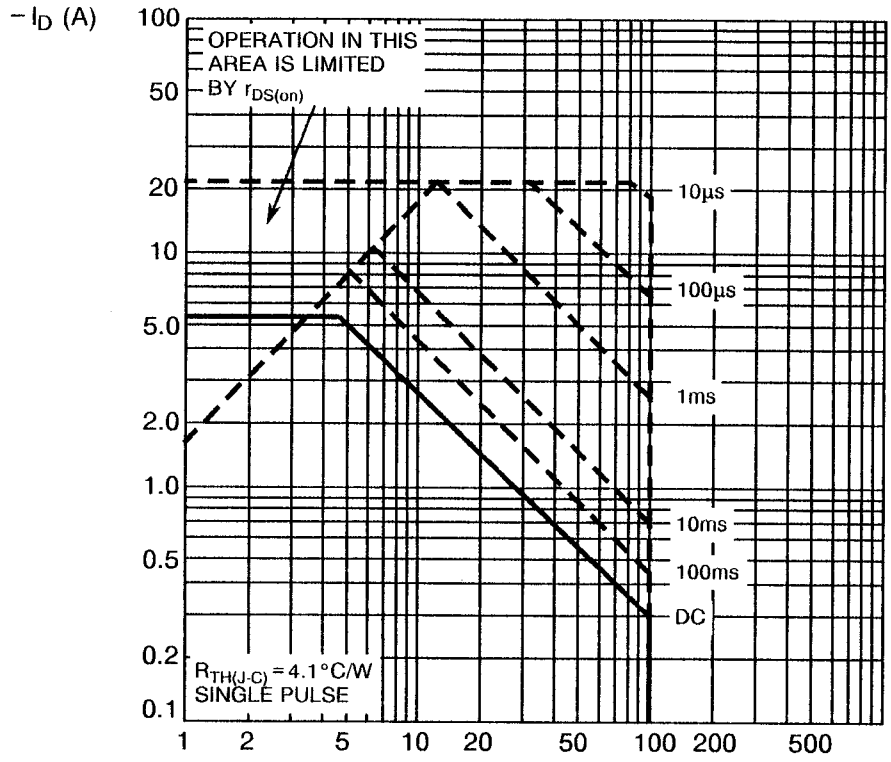
VARIANTS 03, 04



Power Dissipation versus Temperature

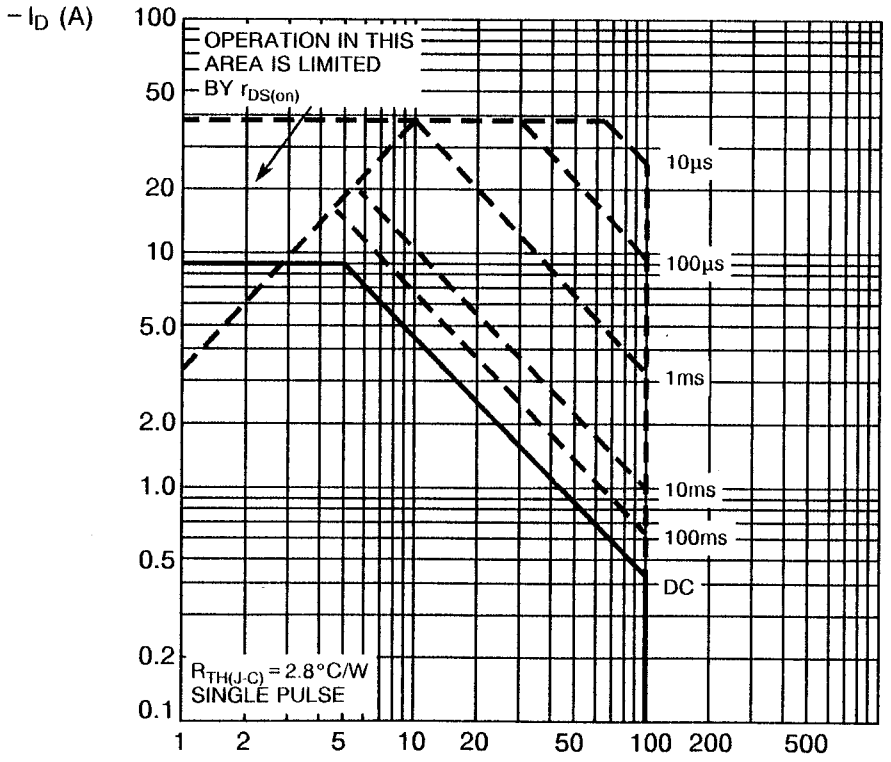
FIGURE 1(b) - MAXIMUM SAFE OPERATING AREA

VARIANT 01



NOTES 1. See Para. 4.7.6.

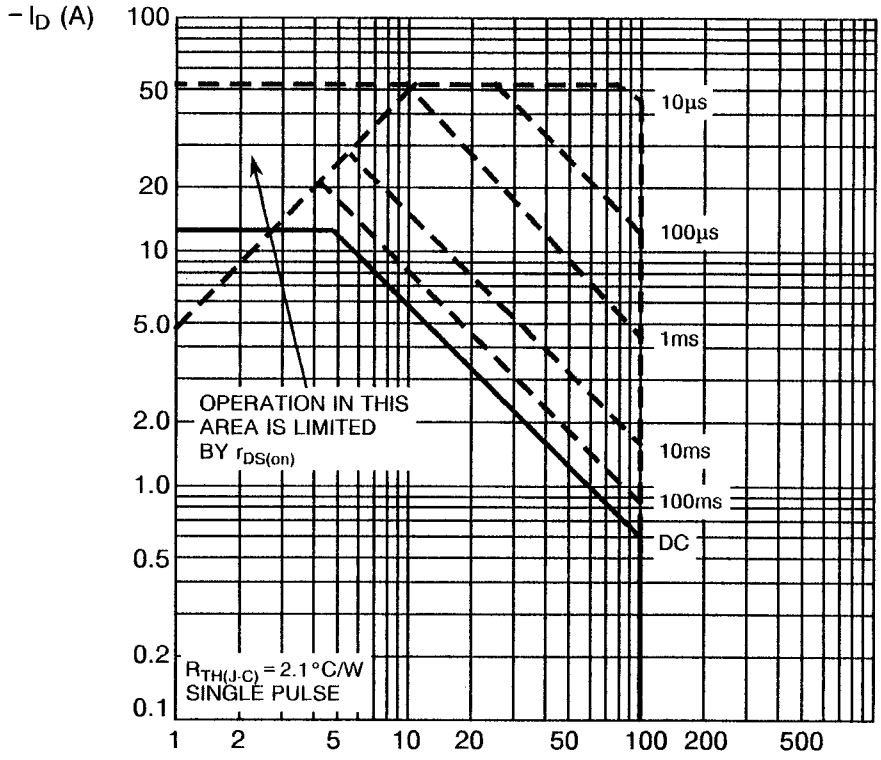
VARIANT 02



NOTES 1. See Para. 4.7.6.

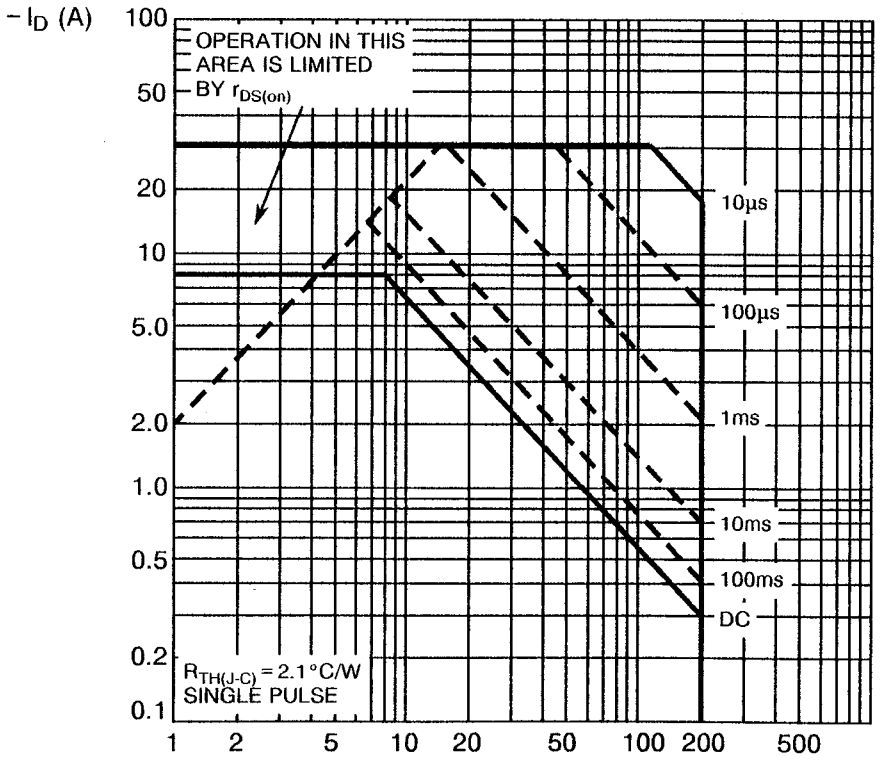
FIGURE 1(b) - MAXIMUM SAFE OPERATING AREA (CONTINUED)

VARIANT 03



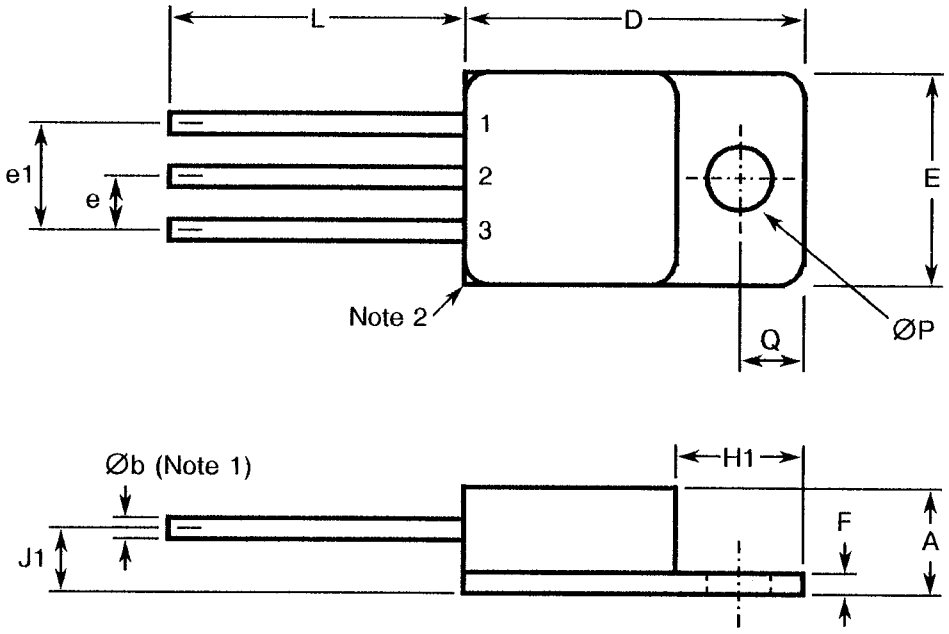
NOTES 1. See Para. 4.7.6.

VARIANT 04



NOTES 1. See Para. 4.7.6.

FIGURE 2 - PHYSICAL DIMENSIONS

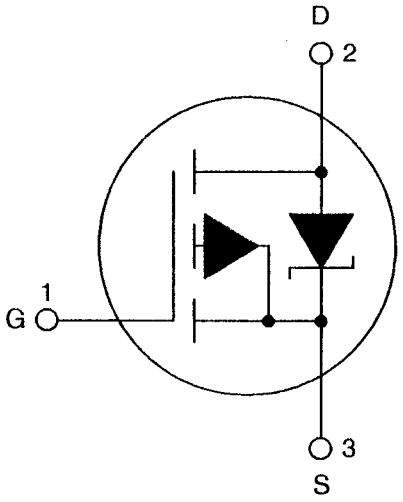


SYMBOL	MILLIMETRES	
	MIN.	MAX.
A	4.45	4.95
Øb	0.90	1.10
D	16.30	16.70
E	10.40	10.80
e	2.34	2.74
e1	4.88	5.28
F	0.60	1.00
H1	5.70	6.10
J1	2.45	2.95
L	12.70	14.70
ØP	3.40	3.80
Q	2.80	3.20

NOTES

1. All 3 leads.
2. Corner radii (6 places) are uncontrolled.

FIGURE 3 - FUNCTIONAL DIAGRAM



TERMINAL	VARIANTS 01 TO 04
1	Gate
2	Drain
3	Source

NOTES

1. The drain is electrically isolated from the case.

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 5000 for Discrete Semiconductor Components.

(b) ESA/SCC Basic Specification No. 21400, Scanning Electron Microscope (SEM) Inspection of Semiconductor Dice.

(c) MIL-STD-202, Test Methods for Electronic and Electrical Component Parts.

(d) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

I_{GSS} = Gate to Source Leakage Current.
B_{VGSS} = Gate to Source Breakdown Voltage.
$V_{GS(th)}$ = Gate Threshold Voltage.
V_{GS} = Gate to Source Voltage.
V_{DG} = Drain to Gate Voltage.
V_{DS} = Drain to Source Voltage.
V_{SD} = Source to Drain Diode Forward Voltage.
gfs = Forward Transfer Conductance.
C_{iss} = Common Source Input Capacitance.
C_{oss} = Common Source Output Capacitance.
C_{rss} = Common Source Reverse Transfer Capacitance.
I_S = Source Current.
I_D = Drain Current.
Ri = Insulation Resistance, Pins to Case.
E_{AS} = Avalanche Energy.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 5000 for Discrete Semiconductor Components. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

(a) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during qualification and maintenance of qualification.

(b) Para. 5.2.2, Total Dose Irradiation Testing: If specified in a Purchase Order, shall be performed during procurement on a lot acceptance basis at the total dose irradiation level specified in the Purchase Order.

(c) For testing levels 'B' and 'C', a Scanning Electron Microscope (SEM) inspection shall be performed on samples from each metallisation lot in accordance with ESA/SCC Basic Specification No. 21400. The SEM inspection shall include the gate finger area plus 3 randomly selected transistor cells, magnification ×2000 viewed from above and with the die tilted about 60°.

4.2.2 Deviations from Final Production Tests (Chart II)

(a) Para. 9.5.1, "Thermal Shock": Shall be performed using the following test conditions for 5 cycles:-

Low temperature = −55(+5−0)°C.
High temperature = +150(+0−5)°C.

(b) An Inductive Avalanche test is to be performed on a 100% basis. The energy pulse to be applied is shown in Table 1(a) column 12 of this specification. The circuit for this test is shown in Figure 4(d) of this specification.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

(a) Para. 7.1.1(b), "Power Burn-in": The duration shall be 240 hours. Parameter drift measurements shall be performed at 0 hours and 240 ± 24 hours.

(b) Para. 9.12, "Radiographic Inspection": Shall be performed in Configuration G, View 1 only.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the transistors specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the transistors specified herein shall be 4.2 grammes.

4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000. The test conditions shall be as follows:-

Test Condition : 'E' (Lead Fatigue).
Applied Force : 10 Newtons, 3 bends at 45°.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the transistors specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

Metal case, hermetically sealed, similar to JEDEC TO-257.

4.4.2 Lead Material and Finish

The lead material shall be Type 'H' with Type '4' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500.

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700 and the following paragraphs. When the component is too small to accommodate all of the marking specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence, shall be as follows:-

(a) Lead Identification.

(b) The SCC Component Number.

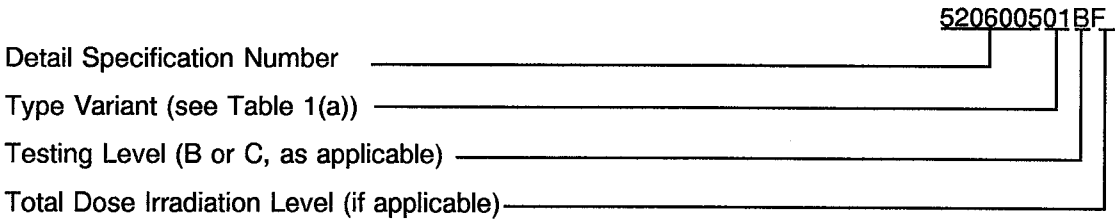
(c) Traceability Information.

4.5.2 Lead Identification

Lead identification shall be as shown in Figures 2 and 3.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



The Total Dose Irradiation level designation shall be added for those devices for which a sample has been successfully tested to the level in question. For these devices, a code letter shall be added in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-in

The requirements for H.T.R.B. burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 5000. The conditions for H.T.R.B. burn-in shall be as specified in Table 5(a) of this specification.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for High Temperature Reverse Bias Burn-in

A circuit for use in performing the H.T.R.B. burn-in test is shown in Figure 5(a) of this specification.

4.7.5 Electrical Circuits for Power Burn-in

A circuit for use in performing the power burn-in test is shown in Figure 5(b) of this specification.

4.7.6 Verification of Safe Operating Area

The requirements for verification of safe operating area testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000.

The test shall be performed twice in accordance with MIL-STD-750, Method 3474 and Figures 1(b) and 4(a) of this specification, at $T_{case} = +25 \pm 10$°C and $T_j = +150$°C maximum..

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	MIL-STD 750 TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
1	Breakdown Voltage Drain to Source	B_{VDSS}	3407 Bias Cond. 'C'	$I_D = -0.25mA$ $V_{GS} = 0V$ Variants 01, 02, 03 Variant 04	 −100 −200	 - -	V
2	Gate Threshold Voltage	$V_{GS(th)}$	3403	$V_{DS} \geq V_{GS}$ $I_D = -1.0mA$	−2.0	−4.0	V
3 to 4	Gate to Source Leakage Current	I_{GSS}	3411 Bias Cond. 'C'	$V_{DS} = 0V$, $V_{GS} = -20V$ $V_{GS} = 20V$	- -	−100 100	nA
5	Drain Current	I_{DSS}	3413 Bias Cond. 'C'	V_{DS} = Note 2 $V_{GS} = 0V$	-	−0.25	mA
6	Drain Source On Resistance	$r_{DS(ON)}$	3421	$V_{GS} = -10V$ Variant 01: $I_D = -3.5A$ Variant 02: $I_D = -6.5A$ Variant 03: $I_D = -10A$ Variant 04: $I_D = -6.0A$ Notes 1 and 4	 - - - -	 0.60 0.31 0.21 0.50	Ω
7	Drain Source On Voltage	$V_{DS(ON)}$	3405	$V_{GS} = -10V$ Variant 01: $I_D = -3.5A$ Variant 02: $I_D = -6.5A$ Variant 03: $I_D = -10A$ Variant 04: $I_D = -6.0A$ Notes 1 and 4	 - - - -	 −2.10 −2.02 −2.10 −3.00	V
8	Source to Drain Diode Forward Voltage	V_{SD}	4011	Variant 01: $I_S = -5.3A$ Variant 02: $I_S = -9.3A$ Variant 03: $I_S = -13A$ Variant 04: $I_S = -7.7A$ Note 1	- - - -	−5.4 −5.3 −4.2 −4.2	V
9	Insulation Resistance	Ri	MIL-STD-202 Method 302 Condition 'C'	Note 5	100	-	MΩ

NOTES

1. Pulsed Measurement: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.
2. See Column 3 of Table 1(a).
3. See Column 7 of Table 1(a).
4. Measured within 2.0mm of case.
5. Between linked pins and case, electrification time ≥ 40μsec.
6. Measurements to be performed on a sample basis, LTPD7.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	MIL-STD 750 TEST METHOD	TEST FIG.	TEST CONDITIONS (NOTE 6)	LIMITS MIN	LIMITS MAX	UNIT
10	Forward Transconductance	gfs	3455	-	$V_{DS} = -10V$ Variant 01: $I_D = -3.5A$ Variant 02: $I_D = -6.5A$ Variant 03: $I_D = -10A$ Variant 04: $I_D = -6.0A$ Note 1	 0.9 2.0 5.0 4.0	 - - - -	S
11	Turn-on Delay Time	$t_{d(ON)}$	3472	4(b)	$R_G = 4.7\Omega$ Variant 01: $I_D = -3.5A$, $V_{DD} = -50V$ Variant 02: $I_D = -6.5A$, $V_{DD} = -50V$ Variant 03: $I_D = -10A$, $V_{DD} = -50V$ Variant 04: $I_D = -6.0A$, $V_{DD} = -100V$	-	30	ns
12	Rise Time	t_r	3472	4(b)	$R_G = 4.7\Omega$ Variant 01: $I_D = -3.5A$, $V_{DD} = -50V$ Variant 02: $I_D = -6.5A$, $V_{DD} = -50V$ Variant 03: $I_D = -10A$, $V_{DD} = -50V$ Variant 04: $I_D = -6.0A$, $V_{DD} = -100V$	 - - - -	 50 100 100 60	ns
13	Turn-off Delay Time	$t_{d(OFF)}$	3472	4(b)	$R_G = 4.7\Omega$ Variant 01: $I_D = -3.5A$, $V_{DD} = -50V$ Variant 02: $I_D = -6.5A$, $V_{DD} = -50V$ Variant 03: $I_D = -10A$, $V_{DD} = -50V$ Variant 04: $I_D = -6.0A$, $V_{DD} = -100V$	 - - - -	 50 80 80 100	ns
14	Fall Time	t_f	3472	4(b)	$R_G = 4.7\Omega$ Variant 01: $I_D = -3.5A$, $V_{DD} = -50V$ Variant 02: $I_D = -6.5A$, $V_{DD} = -50V$ Variant 03: $I_D = -10A$, $V_{DD} = -50V$ Variant 04: $I_D = -6.0A$, $V_{DD} = -100V$	 - - - -	 50 80 50 50	ns

NOTES: See Page 18.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 750 TEST METHOD	TEST FIG.	TEST CONDITIONS (NOTE 6)	LIMITS		UNIT
						MIN	MAX	
15	Common Source Input Capacitance	C_{iss}	3431	-	V_{DS} = −25V V_{GS} = 0V, f = 1.0MHz Variant 01 Variant 02 Variant 03 Variant 04	 200 500 1000 800	 500 950 1700 1500	pF
16	Common Source Output Capacitance	C_{oss}	3453	4(c)	V_{DS} = −25V V_{GS} = 0V, f = 1.0MHz Variant 01 Variant 02 Variant 03 Variant 04	 100 200 350 200	 350 450 700 450	pF
17	Common Source Reverse Transfer Capacitance	C_{rss}	3433	-	V_{DS} = −25V V_{GS} = 0V, f = 1.0MHz Variant 01 Variant 02 Variant 03 Variant 04	 20 40 50 50	 100 150 200 200	pF

NOTES: See Page 18.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE

No.	CHARACTERISTICS	SYMBOL	MIL-STD 750 TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
2	Gate Threshold Voltage	$V_{GS(th)}$	3403	$V_{DS} \geq V_{GS}$ $I_D = -1.0mA$	-1.0	-	V
3 to 4	Gate to Source Leakage Current	I_{GSS}	3411 Bias Cond. 'C'	$V_{DS} = 0V$, $V_{GS} = -20V$ $V_{GS} = 20V$	- -	-200 200	nA
5	Drain Current	I_{DSS}	3413 Bias Cond. 'C'	V_{DS} = Note 3 $V_{GS} = 0V$	-	-1.0	mA
6	Drain Source On Resistance	$r_{DS(ON)}$	3421	$V_{GS} = -10V$ Variant 01: $I_D = -3.5A$ Variant 02: $I_D = -6.5A$ Variant 03: $I_D = -10A$ Variant 04: $I_D = -6.0A$ Notes 1 and 4	 - - - -	 0.99 0.51 0.34 0.88	Ω

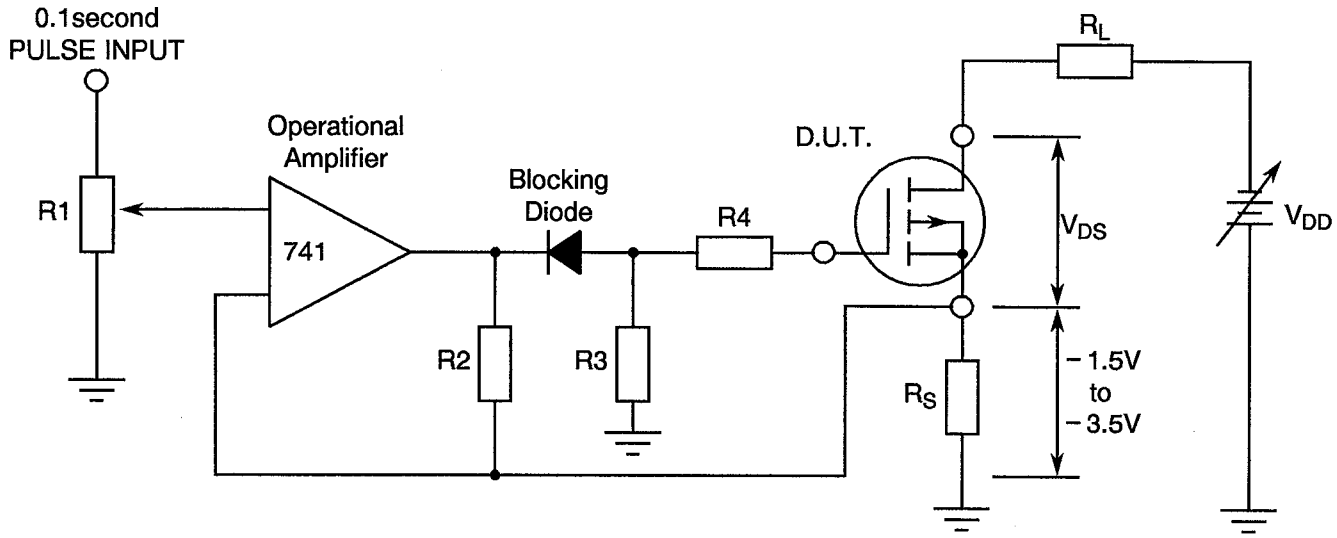
NOTES: See Page 18.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE

No.	CHARACTERISTICS	SYMBOL	MIL-STD 750 TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
2	Gate Threshold Voltage	$V_{GS(th)}$	3403	$V_{DS} \geq V_{GS}$ $I_D = -1.0mA$	-	-5.0	V

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - SAFE OPERATING AREA TEST CIRCUIT



R1 = Variable resistor.
R2 = 20kΩ.
R3 = 20kΩ.
R4 = 47Ω.

Variant 01	Test 1	Test 2
01	$V_{DS} = -80V$, $I_D = -370mA$	$V_{DS} = -6.0V$, $I_D = -5.0A$
02	$V_{DS} = -80V$, $I_D = -560mA$	$V_{DS} = -5.0V$, $I_D = -9.0A$
03	$V_{DS} = -80V$, $I_D = -750mA$	$V_{DS} = -5.0V$, $I_D = -12A$
04	$V_{DS} = -160V$, $I_D = -370mA$	$V_{DS} = -6.0V$, $I_D = -10A$

R_S is non inductive and selected such that $I_D \times R_S$ gives the specified voltage −1.5V to −3.5V.

Test Method for Both Tests

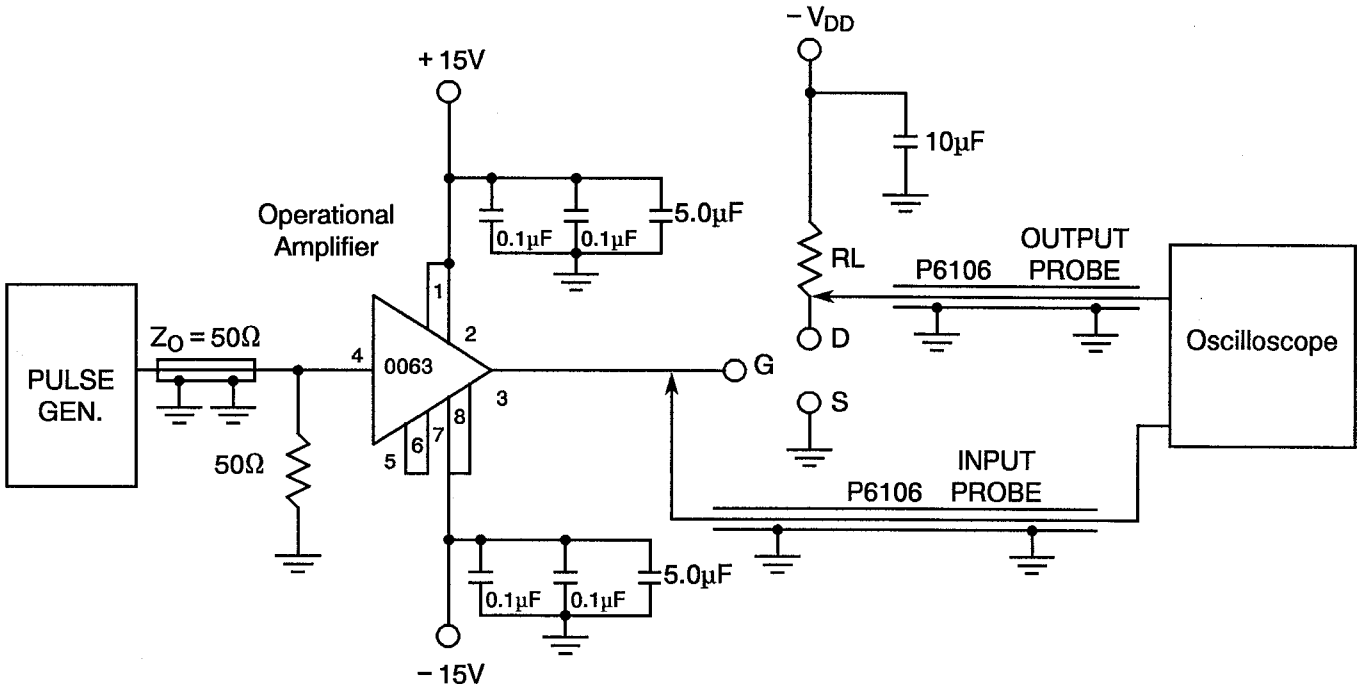
Using a 0.1 second pulse width with a minimum of 1 minute between pulses, increase V_{GS} and the Drain Supply Voltage until the specified value of I_D and V_{DS} are obtained. A load resistor, R_L, shall be used and shall be selected such that $I_D \times R_L = 2.5 \pm 1.0V$.

Electrical Measurements

After performing both tests, electrical measurements Nos. 1 to 8 inclusive of Table 2 shall be repeated.

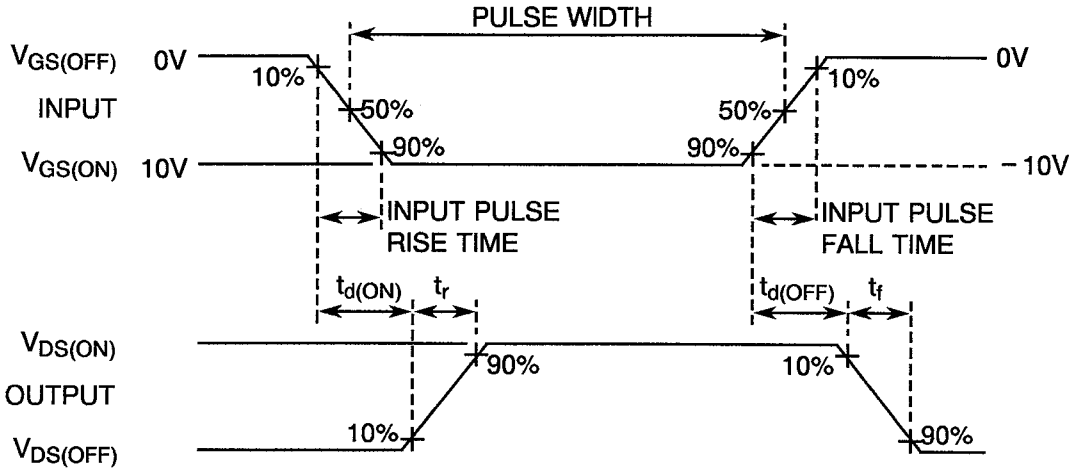
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(b) - SWITCHING TIMES TEST CIRCUIT



NOTES

1. 0063 case grounded.
2. Grounded connections common to ground plane on board.
3. Pulse width ≤3.0s, Period ≤1.0ms, Amplitude = 0V to −10V.

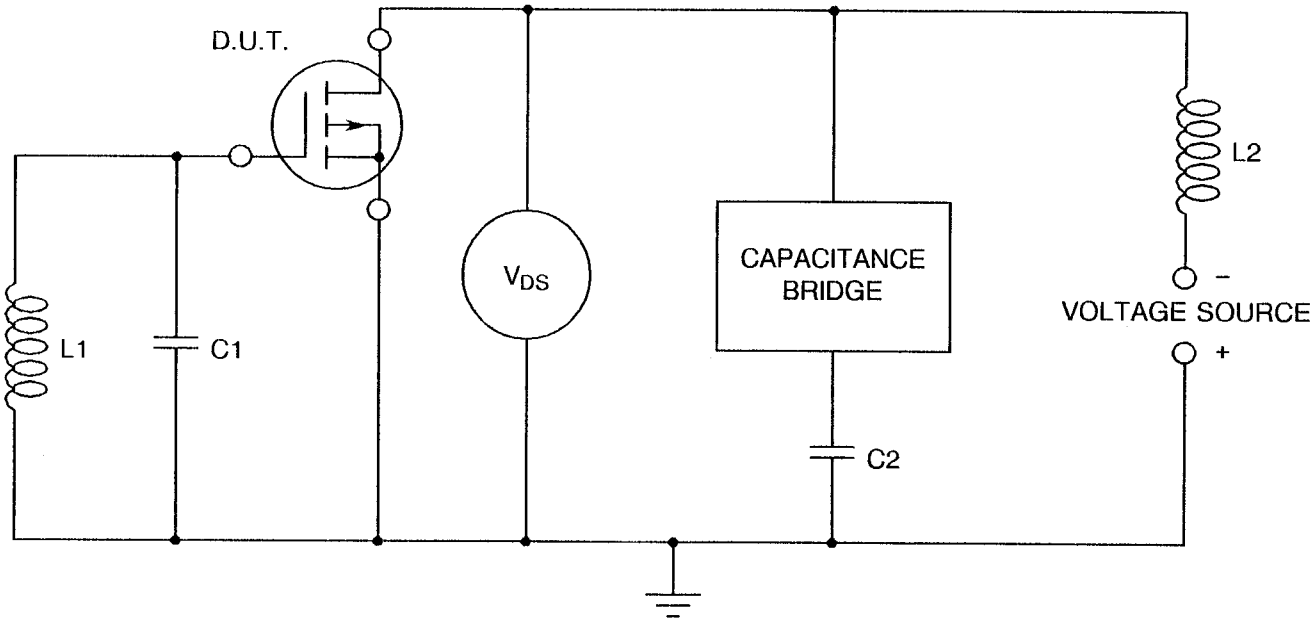


NOTES

1. When measuring rise time, $V_{GS(ON)}$ shall be as specified on the input waveform.
2. When measuring fall time, $V_{GS(OFF)}$ shall be as specified on the input waveform.
3. The input transition and drain voltage response detector shall have rise and fall response times such that doubling these responses will not affect the results greater than the precision of measurement.
4. The current shall be sufficiently small so that doubling it does not affect test results greater than the precision of measurement.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(c) - COMMON SOURCE OUTPUT CAPACITANCE

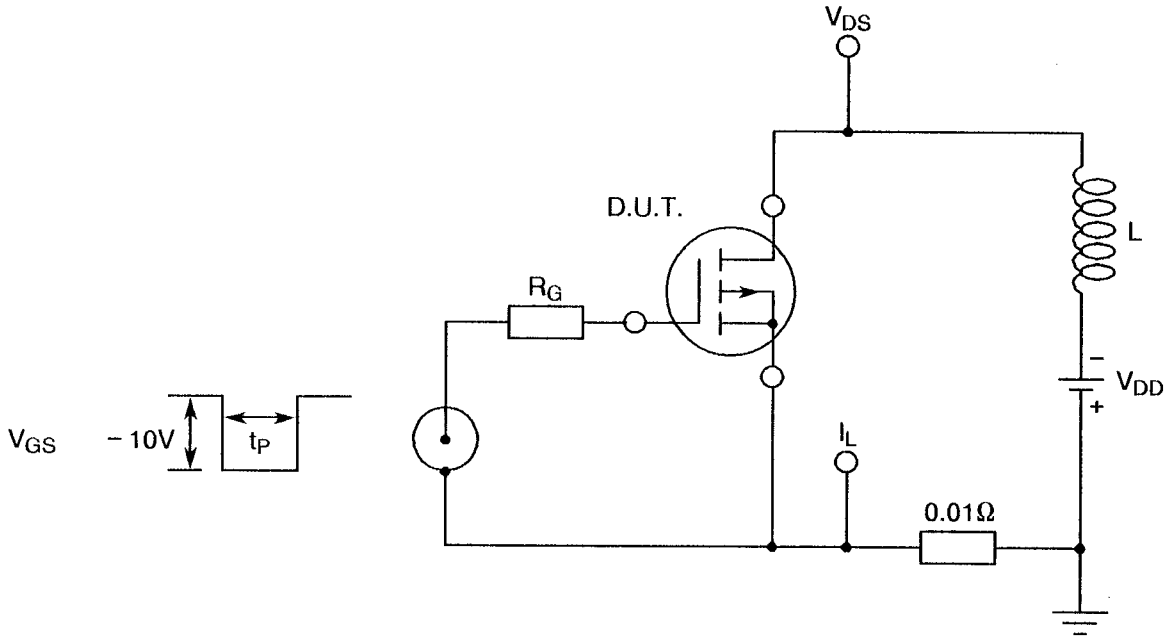


PROCEDURE

The capacitors C1 and C2 shall present apparent short circuits at the test frequency. L1 and L2 shall present a high a.c. impedance at the test frequency for isolation. The bridge shall have low d.c. resistance between its output terminals and should be capable of carrying the test current without affecting the desired accuracy of measurement.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(d) - UNCLAMPED INDUCTIVE AVALANCHE TEST CIRCUIT



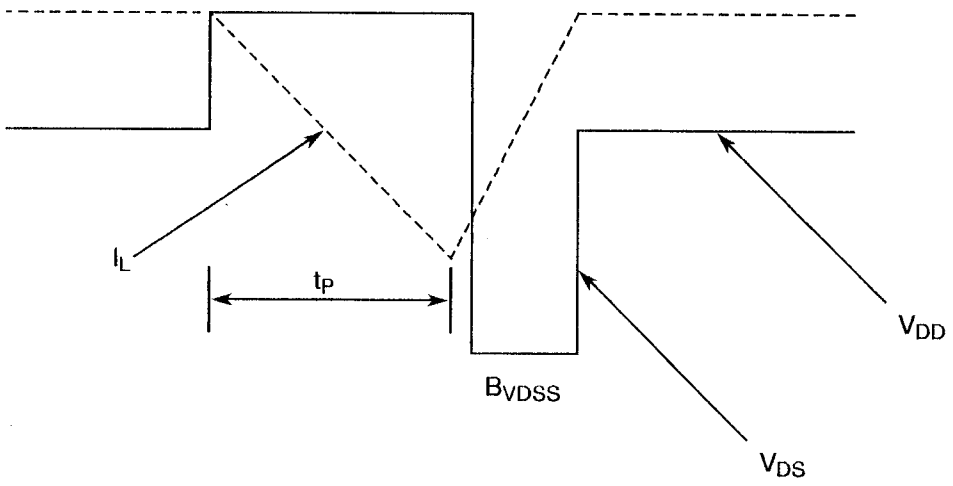


TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
2	Gate Threshold Voltage	$V_{GS(th)}$	As per Table 2	As per Table 2	±20	%
3 to 4	Gate to Source Leakage Current	I_{GSS}	As per Table 2	As per Table 2	±20 or (1) ±100	nA %
5	Drain Current	I_{DSS}	As per Table 2	As per Table 2	±25 or (1) ±100	µA %
6	Drain-Source On Resistance	$r_{DS(ON)}$	As per Table 2	As per Table 2	±20	%

NOTES

1. Whichever is greater referred to the initial value.

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+150(+0−5)	°C
2	Drain Source Voltage	V_{DS}	Variant 01, 02, 03: −80 Variant 04: −160	V
3	Gate Source Voltage	V_{GS}	0	V
4	Duration	t	72	Hrs

TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Junction Temperature	T_J	140 ± 10 (1)	°C
2	Minimum Drain Source Voltage	V_{DS}	−10	V
3	Gate Source Voltage	V_{GS}	−1.0 to −16	V

NOTES

1. Using the circuit shown in Figure 5(b), power shall be applied to the device to achieve the specified junction temperature. The junction temperature (T_J) should be determined as follows:-

   T_J = $(P_T) \times (R_{TH(J-C)}) + T_{case}$.

   P_T = $(V_{DS}) \times (I_D)$.

   $R_{TH(J-C)}$ = See column 11 of Table 1(a).

   T_{case} = Measured value at the hottest point on the case.

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

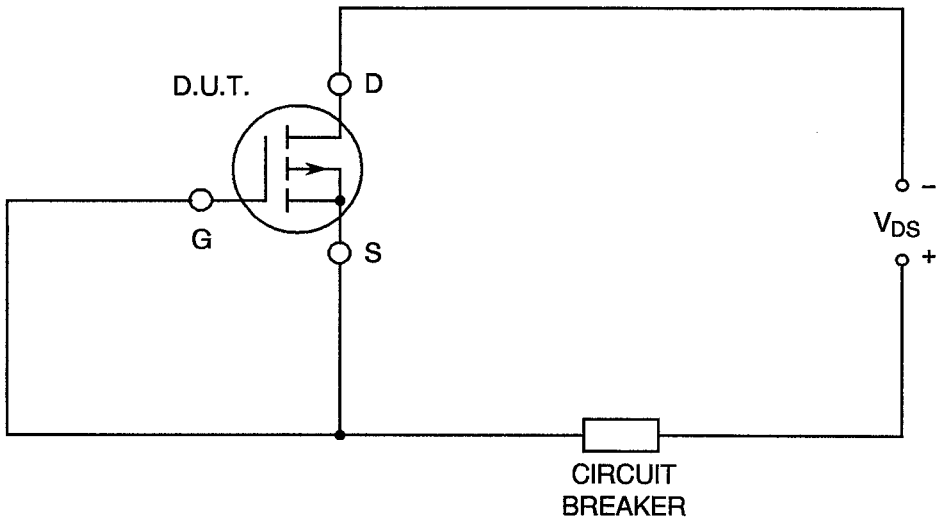
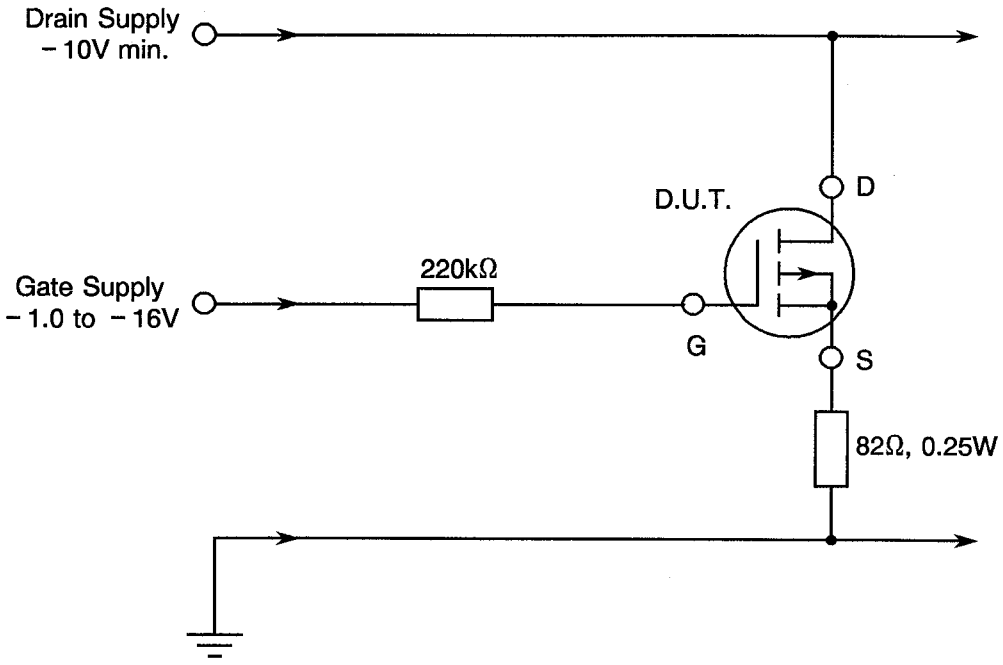


FIGURE 5(b) - ELECTRICAL CIRCUIT FOR BURN-IN AND OPERATING LIFE TESTS



4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 5000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 2 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests

The parameters to be measured at intermediate points and on completion of endurance tests are scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Conditions for Operation Life Tests (Part of Endurance Testing)

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000. The conditions for operating life testing shall be the same as specified in Table 5(b) for the burn-in test.

4.8.4 Electrical Circuits for Operating Life Tests

The circuit to be used for performance of the operating life tests shall be the same as shown in Figure 5(b) for the burn-in test.

4.8.5 Conditions for High Temperature Storage Test (Part of Endurance Testing)

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 5000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

4.9 TOTAL DOSE IRRADIATION TESTING

4.9.1 Application

If specified in Para. 4.2.1 of this specification, total dose irradiation testing shall be performed in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.9.2 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6 of this specification.

4.9.3 Electrical Measurements

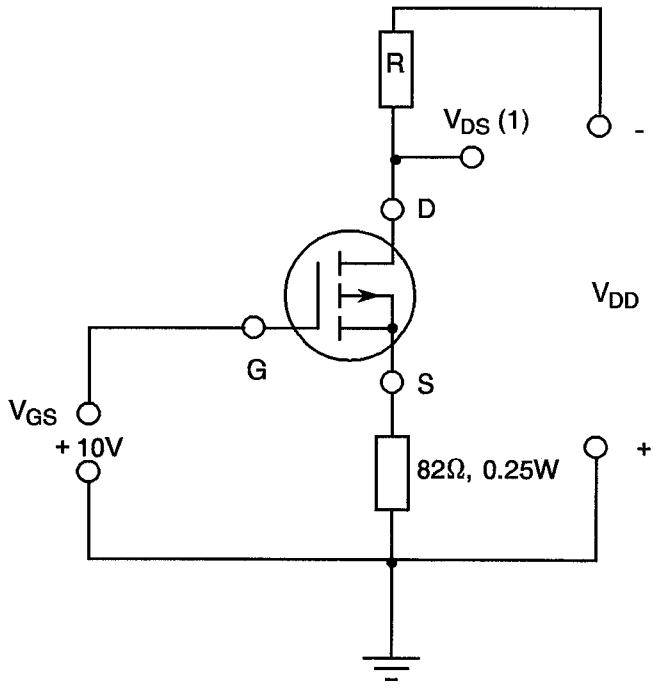
The parameters to be measured prior to irradiation exposure are scheduled in Table 2 of this specification. Only devices which meet the requirements of Table 2 shall be included in the test sample.

The parameters to be measured during and on completion of irradiation testing are scheduled in Table 7 of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
2	Gate Threshold Voltage	$V_{GS(th)}$	As per Table 2	As per Table 2	−2.0	−4.0	V
3 to 4	Gate to Source Leakage Current	I_{GSS}	As per Table 2	As per Table 2	- -	−100 100	nA
5	Drain Current	I_{DSS}	As per Table 2	As per Table 2	-	−0.25	mA

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING



NOTES

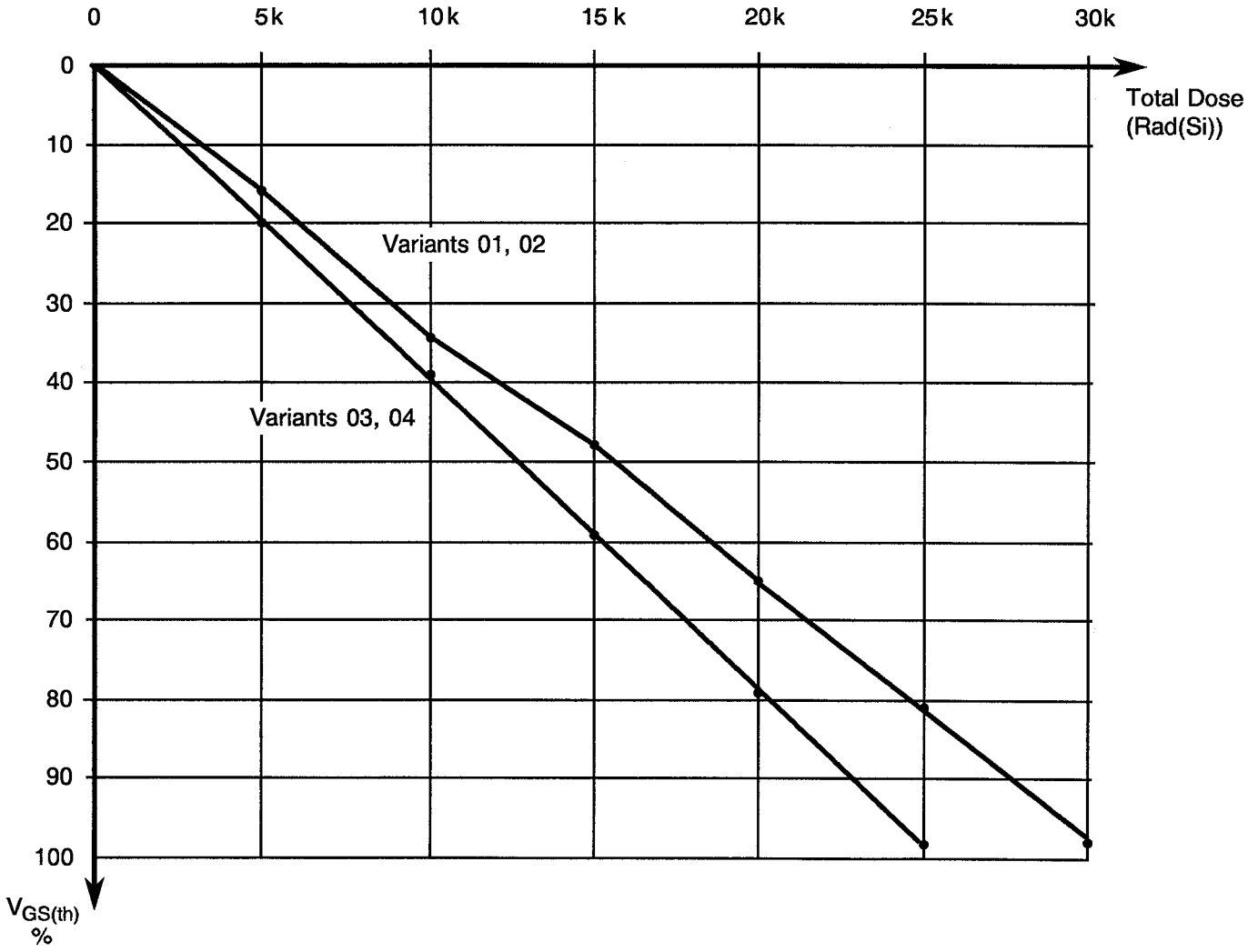
1. 100% of Table 1(a), Column 3.

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
2	Gate Threshold Voltage	$V_{GS(th)}$	As per Table 2	As per Table 2	Note 1	V

NOTES

1. The graph given below shall be used to determine the maximum permitted change.



APPENDIX 'A'

AGREED DEVIATIONS FOR INTERNATIONAL RECTIFIER COMPANY LTD. (G.B.)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.2	(a) An "Isolation" test between terminals and case may be performed on 100% basis at any time during Chart II using the following conditions:- Test Voltage: 1000V Visual Inspection for "flashover" during the test. (b) Para. 9.7, "Particle Impact Noise Detection (PIND)" test shall not be performed as the cavity is filled with gel.