european space agency
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RADIOGRAPHIC INSPECTION OF INTEGRATED CIRCUITS

ESA/SCC Basic Specification No. 2099000

space components
coordination group

Issue/Rev.	Date	Approved by	
		SCCG Chairman	ESA Director General or his Deputy
Issue 1	September 1994	[signature]	[signature]

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference	CHANGE Item	Approved DCR No.

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1. SCOPE

This specification, to be read in conjunction with ESA/SCC Basic Specification No. 20900, Radiographic Inspection, contains additional requirements to be applied to Integrated Circuits.

2. GENERAL REQUIREMENTS

2.1 APPLICABILITY

The following criteria may not be varied or modified after commencement of any inspection stage. Any ambiguity or proposed deviation shall be referred to the Qualifying Space Agency for resolution and approval.

2.2 PROCEDURE

All items shall be examined in such a manner that a minimum of handling and movement of the components is involved.

3. X-RAY PHOTOGRAPHS

Each component shall be radiographed once along one axis.

4. DETAILED REQUIREMENTS

4.1 REJECT CRITERIA

The individual device examination shall include, but not be limited to, inspection for foreign particles, build-up of bonding material, placement of lead wires, bond of lead to semiconductor element and lead to terminal post, and mounting of semiconductor element. Any device for which the radiograph reveals any of the following defects shall be rejected.

4.2 PRESENCE OF EXTRANEOUS MATTER

Extraneous matter (foreign particles) shall include, but not be limited to:-

(a) Any foreign particle, loose or attached, greater than 0.0254mm (see Figure I), or of any lesser size which is sufficient to bridge non-connected conducting elements of the device.

(b) Any wire tail extending beyond its normal end by more than two diameters at the semiconductor die pad or by more than four wire diameters at the package post (see Figure I).

(c) Any burr on a post (header lead) greater than 0.08mm in its major dimension or of such configuration that it may break away.

(d) Excessive semiconductor element bonding material build-up.

(1) A semiconductor element shall be mounted and bonded so that it is not tilted more than 10 degrees from the normal mounting surface. The bonding agent that accumulates around the perimeter of the semiconductor element and touches the side of the semiconductor element shall not accumulate to a thickness greater than that of the semiconductor element (see Figures II and III). Where the bonding agent is built up, but is not touching the semiconductor element, the build-up shall not be greater than twice the thickness of the semiconductor element.

(2) There shall be no visible extraneous material of 0.0254mm or larger in the major dimension. Loose bonding material will be considered extraneous material. Excessive (but not loose) bonding material will not be considered extraneous unless it fails to meet the requirements of Paragraph 4.2(d) (1) or the accumulation of bonding material is in the pedestal form (see Figures II and III).

(e) Gold flaking on the header or posts or anywhere inside the case.

(f) Extraneous ball bonds anywhere inside the case, except for attached residue when rebonding is allowed.

4.3 UNACCEPTABLE CONSTRUCTION

In the examination of devices, the following aspects shall be considered unacceptable construction and devices that exhibit the following defects shall be rejected:-

(a) Voids - When radiographing devices, certain types of mounting do not give true representations of voids. When such devices are inspected, the mounting shall be noted on the inspection report (see Figure I).

(1) Contact area voids in excess of one-half of the total contact area.

(2) A single void equal to the length of the semiconductor element.

(3) A single void that traverses the width of the semiconductor element.

(b) Wires present other than those connecting specific areas of the semiconductor element to the external leads. Device designs calling for the use of such wires, including jumping wires, are acceptable (see Figure I).

(c) Cracks, splits or chips of the electrical elements.

(d) Defective seal - Any device wherein the integral lid seal is not continuous or is reduced from its designed sealing width by more than 75%. Expulsion resulting from the final sealing operation is not considered extraneous material as long as it can be established that it is attached to the parent material and does not exhibit a tear-drop confuguration (i.e. where the base support's least dimension is smaller than the dimension it is supposed to support).

(e) Inadequate clearance - Acceptable devices shall have adequate internal clearance to ensure that the elements cannot contact one another or the case. No cross-overs shall be allowed. Depending upon the case type, devices shall be rejected for the following conditions:-

(1) Flat pack and dual-in-line (see Figure IV).

   (a) Any lead wire that appears to touch or cross another lead wire or bond (Y plan only).

   (b) Any lead wire that deviates from a straight line from bond to external lead and appears to be within 0.05mm of another wire or bond (Y plane only).

   (c) Lead wires that do not deviate from a straight line from bond to external lead and appear to touch antoher wire or bond (Y plane only).

   (d) Any lead wire that touches or comes within 0.05mm of the case or external lead to which it is not attached (X and Y planes).

   (e) Any bond that is less than 0.025mm (excluding bonds connected by a common conductor) from another bond (Y plane only).

   (f) Any wire making a straight line run from die bonding pad to package post that has no arc.

(2) Round Transistor Type (see Figure V).

   (a) Any lead wire that touches or comes within 0.05mm of the case or external lead to which it is not attached (X and Y planes).

   (b) Lead wires that sag below an imaginary plane across the top of the bond (X plane only).

   (c) Any lead wire that appears to touch or cross another lead wire or bond (Y plane only).

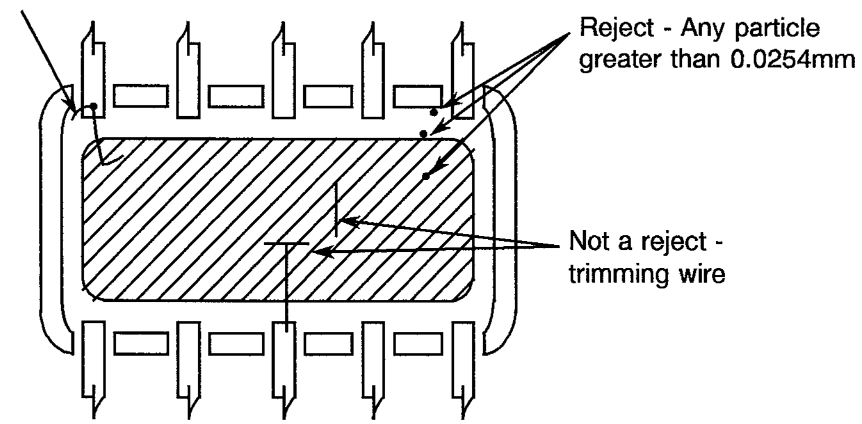
   (d) Any lead wire that deviates from a straight line from bond to external lead and appears to touch or be within 0.05mm of another wire or bond (Y plane only).

   (e) Any bond that is less than 0.025mm (excluding bonds connected by a common conductor) from another bond (Y plane only).

   (f) Any wire making a straight line run from die bonding pad to package post that has no arc.

FIGURE I - PARTICLE LOCATIONS, PIGTAILS, TRIMMING WIRES AND VOIDS

(a) Particle Locations, Pigtails & Trimming Wires



(b) Voids

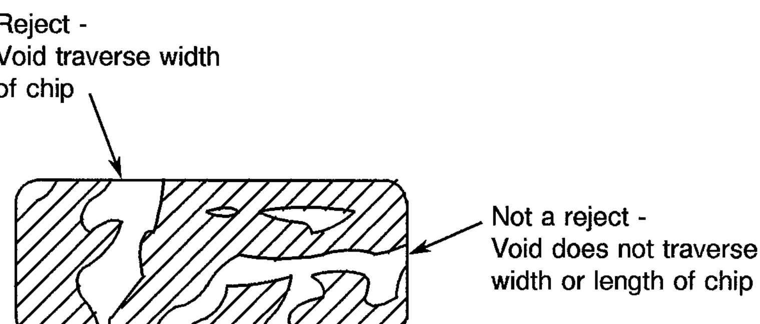
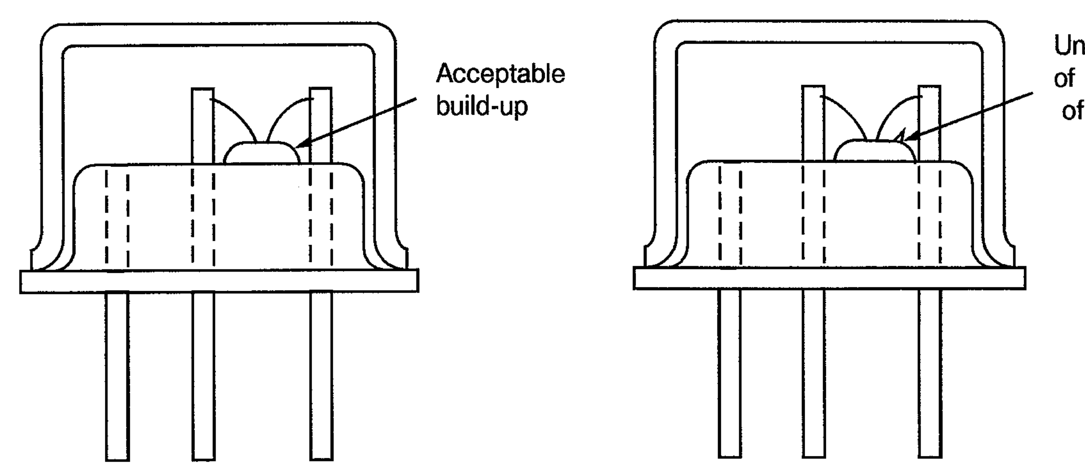


FIGURE II - ACCEPTABLE AND UNACCEPTABLE BONDING MATERIAL BUILD-UP



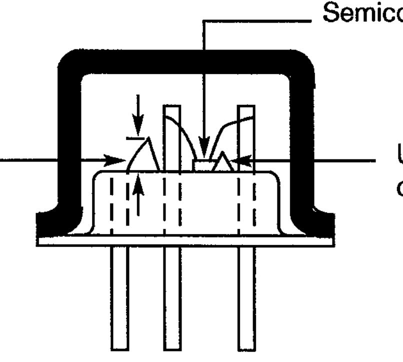
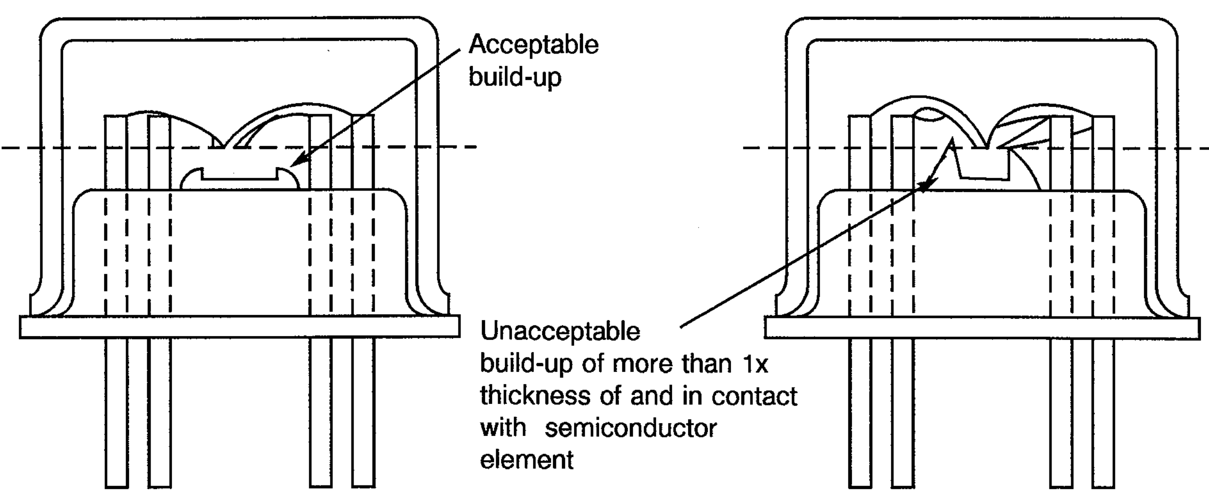


FIGURE III - EXTRANEOUS BONDING MATERIAL BUILD-UP



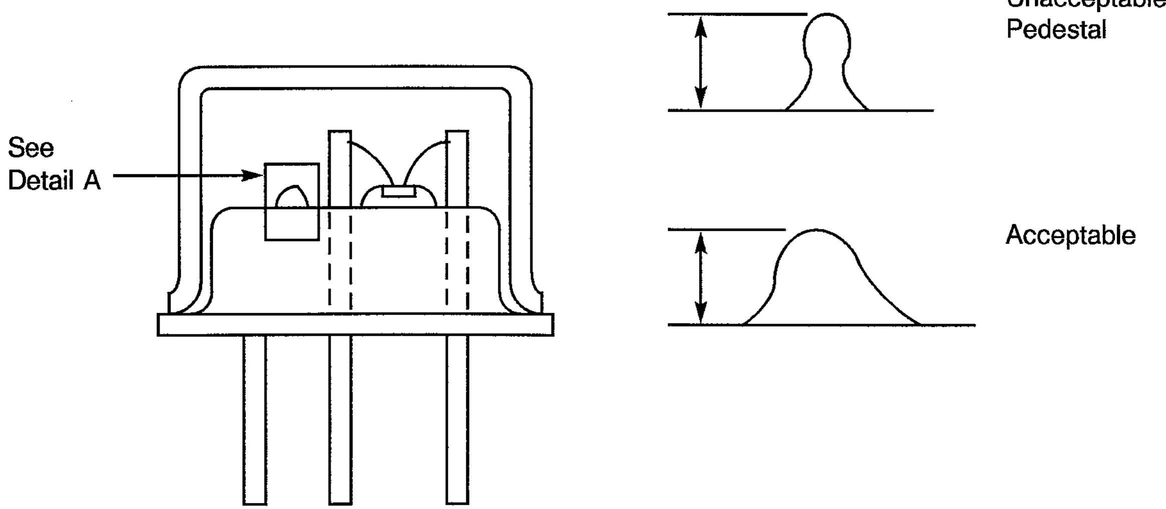


FIGURE IV - CLEARANCE IN DUAL-IN-LINE OR FLAT PACK TYPE DEVICE

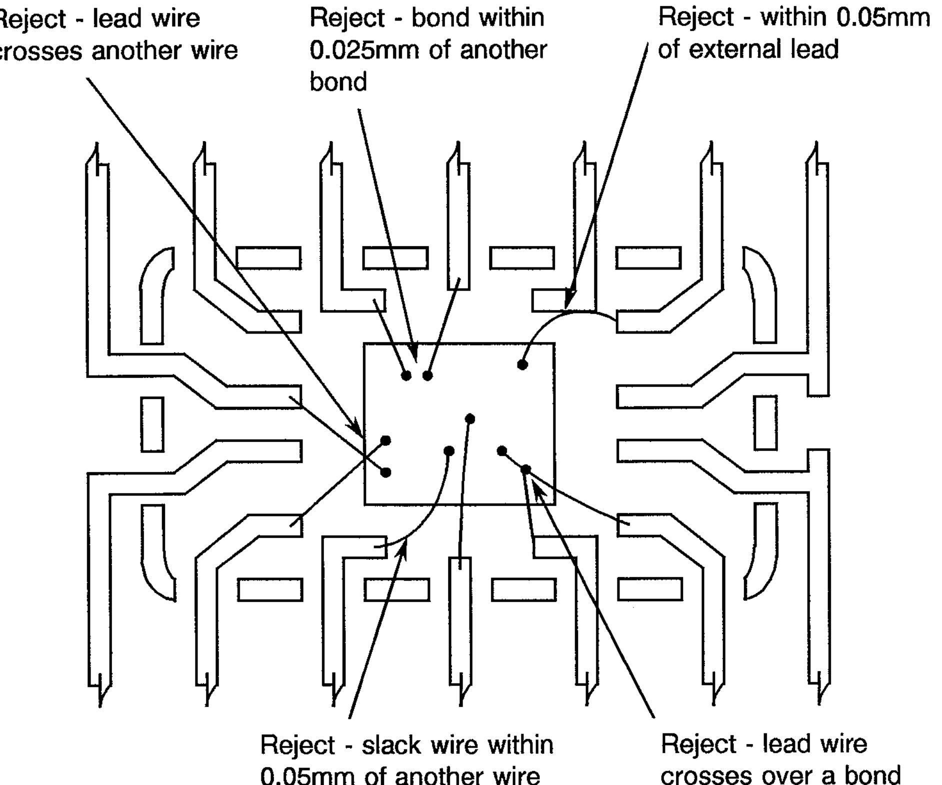
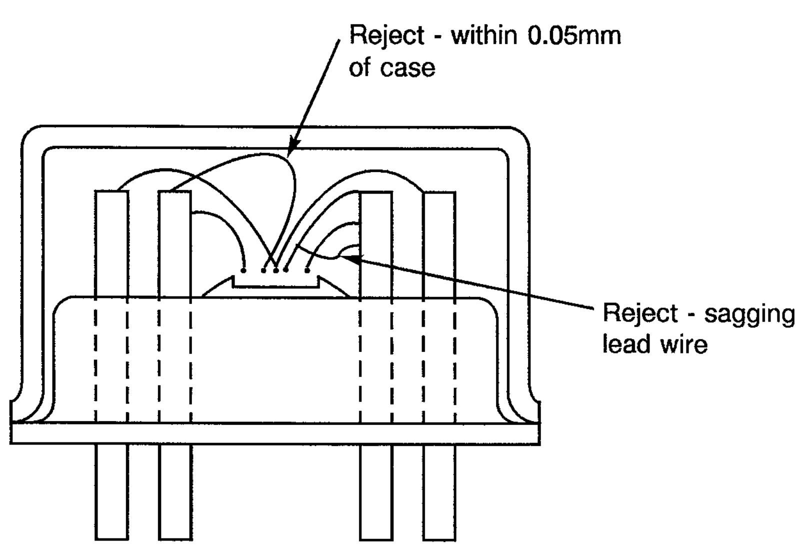


FIGURE V - CLEARANCE IN ROUND TRANSISTOR TYPE DEVICE

(a) X-AXIS CLEARANCE



(b) Y-AXIS CLEARANCE