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TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS FOR INTEGRATED CIRCUITS

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1. SCOPE

This specification forms part of ESA/SCC Basic Specification No. 21300, Terms, Definitions, Abbreviations, Symbols and Units, and covers integrated circuits.

2. TERMS, DEFINITIONS AND SYMBOL LETTERS

2.1 DIGITAL INTEGRATED CIRCUITS

PARAMETER	SYMBOL	DEFINITION
High Level		The level which is the most positive of the 2 logic levels.
Low Level		The level which is the most negative of the 2 logic levels.
Negative Logic		The logic is termed negative when logic 0 state is assigned to the high level and logic 1 state to the low level.
Positive Logic		The logic is termed positive when logic 1 state is assigned to the high level and logic 0 state to the low level.
Truth Table		A tabulation relating all output logic levels to all possible combinations of input logic levels for sufficient successive time intervals (t_n, t_n + 1) to completely characterise the static and dynamic functions of the logic microcircuit, expressed in logic levels or appropriate symbols.
Minimum Asynchronous Input Pulse Width	APW	The smallest pulse width for which stable transition of logic levels, according to the truth table, is guaranteed when the asynchronous inputs are returned to their non-controlling levels.
Minimum Clock Pulse Width	CPW	The smallest pulse width for which stable transition of logic levels, according to the truth table, is guaranteed when the clock goes through the required sequence.
Minimum and Maximum Clock Repetition Rates	CRR	The lowest and highest rates at which clock pulses may repeat logic levels for which stable transition of logic levels, according to the truth table, is guaranteed when the clock goes through its required sequence.
High-level Supply Current	I_{CCH} I_{DDH} I_{EEH}	The current flowing into a supply terminal of a microcircuit when all the outputs are at a high-level voltage.
Low-level Supply Current	I_{CCL} I_{DDL} I_{EEL}	The current flowing into a supply terminal of a microcircuit when all the outputs are at a low-level voltage.
Maximum Collector Cut-off Current	I_{CEX}	The maximum forced current measured at the collector of an output transistor without a current source (pull-up) that will produce a specified high-level output voltage.

PARAMETER	SYMBOL	DEFINITION
High-level Input Current	I_{IH}	The current flowing into an input when a specified high-level voltage is applied to that input.
Low-level Input Current	I_{IL}	The current flowing into an input when a specified low-level voltage is applied to that input.
High-level Node Input Current	I_{INH}	The current flowing into an input node with a specified high-level voltage applied to that node.
Low-level Node Input Current	I_{INL}	The current flowing into an input node with a specified low-level voltage applied to that node.
High-level Output Current	I_{OH}	The current flowing into the output at a specified high-level voltage.
Low-level Output Current	I_{OL}	The current flowing into the output at a specified low-level output voltage.
Output Short-circuit Current	I_{OS}	The current which flows into an output when the output is short-circuited to ground with the specified conditions applied to establish the output logic level farthest from ground potential.
Input Signal Timing Relationships (Synchronous, Asynchronous and Clock)	t_{TR}	The time relationship which must exist between input signals as a necessary condition to ensure compliance with the truth table. Time must be specified from positive- or negative-going edges of the clock pulse.
Propagation Delay Time, High-to-Low Level Output	t_{PHL}	The time between the specified reference points on the input and output voltage waveforms with the specified output changing from the defined high level to the defined low level. The reference points on both the input and output waveforms are the same value which is midway between the maximum low-level input voltage (V_{ILmax}) and the minimum high-level input voltage (V_{IHmin}).
Propagation Delay Time, Low-to-High Level Output	t_{PLH}	The time between the specified reference points on the input and output voltage waveforms with the specified output changing from the defined low level to the defined high level. The reference points on both the input and output waveforms are the same value which is midway between the maximum low-level input voltage (V_{ILmax}) and the minimum high-level input voltage (V_{IHmin}).
Transition Time, High-to-Low Level Output	t_{THL}	The time between a specified high-level voltage and a specified low-level voltage on the output voltage waveform with the specified output changing from the defined high level to the defined low level.
Transition Time, Low-to-High Level Output	t_{TLH}	The time between a specified low-level voltage and a specified high-level voltage on the output voltage waveform with the specified output changing from the defined low level to the defined high level.

PARAMETER	SYMBOL	DEFINITION
Minimum and Maximum Clock-level Transition Times	t_{TC}	The shortest and longest transition times of a clock pulse for which stable transition of logic levels, according to the truth table, is guaranteed when the clock goes through its required sequence.
Minimum and Maximum Clock Levels, High and Low	V_{CH} and V_{CL}	The lowest and highest magnitudes of clock voltages, for both high and low levels, for which stable transition of logic levels, according to the truth table, is guaranteed when the clock goes through its required sequence at the specified maximum repetition rate.
Maximum High-level Input Voltage	V_{IHmax}	The most positive (least negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.
Minimum High-level Input Voltage	V_{IHmin}	The least positive (most negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.
Maximum Low-level Input Voltage	V_{ILmax}	The most positive (least negative) value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.
Minimum Low-level Input Voltage	V_{ILmin}	The least positive (most negative) value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.
Maximum High-level Node Input Voltage	V_{INHmax}	The most positive (least negative) value of high-level node voltage for which operation of the logic element within specification limits is guaranteed.
Minimum High-level Node Input Voltage	V_{INHmin}	The least positive (most negative) value of high-level node voltage for which operation of the logic element within specification limits is guaranteed.
Maximum Low-level Node Input Voltage	V_{INLmax}	The most positive (least negative) value of low-level node voltage for which operation of the logic element within specification limits is guaranteed.
Minimum Low-level Node Input Voltage	V_{INLmin}	The least positive (most negative) value of low-level node voltage for which operation of the logic element within specification limits is guaranteed.
Noise Margin	V_N	The voltage amplitude of extraneous signal which can be algebraically added to the noise-free worst-case "input" level before the output voltage deviates from the allowable logic voltage levels. The term "input" is used here to refer to logic input terminals, power supply terminals, or ground reference terminals.
High-level Output Voltage	V_{OH}	The voltage level at an output terminal for a specified output current with the specified conditions applied to establish a high level at the output.
Low-level Output Voltage	V_{OL}	The voltage level at the output terminal for a specified output current with the specified conditions applied to establish a low level at the output.

2.2 LINEAR (ANALOGUE) INTEGRATED CIRCUITS

PARAMETER	SYMBOL	DEFINITION
Balanced Amplifier		An amplifier having 1 output is considered balanced when the quiescent D.C. output voltage is reduced to 0 or a specified level. An amplifier having 2 outputs is considered balanced when the difference between the quiescent D.C. output voltages is reduced to 0 or a specified level.
Automatic Gain Control Range	AGC range	The maximum change in gain expressed in dB which may be achieved by application of a specified range of D.C. voltages to the AGC input.
Common-mode Voltage Amplification	A_{VC} or A_{vc}	The ratio of the change in voltage at the output terminal in respect of ground (or change in voltage between the output terminals) to the change in common-mode input voltage with the differential input voltage held constant.
Differential Voltage Amplificiation	A_{VD} or A_{vd}	The ratio of the change in voltage at the output terminal in respect of ground (or change in voltage between the output terminals) to the change in differential input voltage with the common-mode input voltage held constant.
Single-ended Voltage Amplification	A_{VS} or A_{vs}	The ratio of the change in single-ended output voltage of a differential amplifier to the change in single-ended input voltage
Bandwidth	B or BW	The range of frequencies within which the gain of the amplifier is not more than 3dB below the value of the midband gain. Midband gain is the gain at a specified frequency or the average gain over a specified frequency range.
Maximum Output Swing Bandwidth	B_{OM}	The range of frequencies within which the maximum output voltage swing is above a specified value for a specified load impedance.
Common-Mode Rejection Ratio	CMRR	The ratio of the differential voltage amplification to the common-mode voltage amplification.
Noise Factor	F	The ratio of the total noise power delivered to the load, to the noise power that would be delivered to the load if the only output noise component were due to the thermal noise of the input source resistance at a temperature of 290°K.
Power Gain or Insertion Power Gain	G_P or G_p	The ratio, usually expressed in dB, of the signal power delivered to the load(s) to the signal power delivered to the input(s). ($dB = 10 \log P_{load}/P_{in}$).
Transducer Power Gain	G_T or G_t	The ratio, usually expressed in dB, of the signal power delivered to the load(s) to the signal power available from the source. ($dB = 10 \log P_{load}/P_{in}$).
Input Bias Current	I_{IB}	The current into the input or the average of the currents into the inputs when the device is in the quiescent or balanced state.

PARAMETER	SYMBOL	DEFINITION
Input Offset Current	I_{IO}	The difference between the currents into the input terminals of a differential input device in the quiescent or balanced state.
Noise Figure	NF	Noise factor expressed in decibels.
DC Power Dissipation	P_D	The total D.C. power supplied to a device less any power delivered from the device to a load.
Power Supply Rejection Ratio	PSRR or $\Delta V_{IO}/\Delta V_{CC}$ $\Delta V_{IO}/V_{DD}$	The ratio of the change in input offset voltage to the corresponding change in value of 1 power supply voltage with all remaining power supply voltages held constant.
Slew Rate	SR	The time rate of change of the closed loop amplifier output voltage for a step-signal input. Normally, slew rate is measured using the largest input voltage step for which the amplifier performance remains linear with feedback adjusted for unity gain.
Total Harmonic Distortion	THD	The ratio, expressed in percent, of the RMS voltage of all harmonics present in the output to the total RMS voltage of the output for a pure sine wave input. The RMS voltages are measured at an output terminal in respect of ground.
Transient Response	TR	The closed-loop step function response of an amplifier under small signal conditions.
Overload Recovery Time	t_{or}	The time required for an amplifier to recover its ability to perform amplification within stated specification limits after the output voltage amplitude has been distorted by the application of a specified input voltage in excess of rated amplitude.
Quiescent Input Voltage	V_I	The D.C. voltage at the input of an amplifier with reference to a common terminal, normally ground, with no signal applied to the input.
Common-mode Input Voltage	V_{IC}	The components of the voltages at the 2 input terminals which are identical in phase and amplitude.
Common-mode Input Voltage Range	V_{ICR}	The range of common-mode voltages which, if exceeded, will cause the total harmonic distortion of the amplifier to exceed a specified maximum value.
Differential Input Voltage	V_{ID}	The difference between the 2 voltages applied to the input terminals of an amplifier.
Input Offset Voltage	V_{IO}	The D.C. voltage which must be applied between the input terminals to force the quiescent D.C. output voltage to 0 or other specified level.
Single-ended Input Voltage	V_{IS}	The signal voltage which is applied to 1 input of a differential amplifier with the other input terminal at signal ground.

PARAMETER	SYMBOL	DEFINITION
Single-ended Input Voltage Range	V_{ISR}	The range of single-ended input voltage which, if exceeded on any input terminal, will cause the total harmonic distortion of the amplifier to exceed a specified maximum value.
Quiescent Output Voltage	V_O	The D.C. voltage at an output terminal with reference to a common terminal, normally ground, when no signal is applied to the input.
Common-mode Output Voltage	V_{OC}	The difference between the A.C. voltages present at 2 output terminals (or the output terminal and ground for amplifiers with 1 output) when signals of identical phase and amplitude are applied to the input terminals.
Differential Output Voltage	V_{OD}	The difference between the voltages present at 2 output terminals when a differential input voltage is applied to the input terminals of an amplifier.
Output Offset Voltage	V_{OO}	The difference between the D.C. voltages present at 2 output terminals (or the output terminals and ground for amplifiers with 1 output) when the input terminals are grounded.
Maximum Output Voltage Swing	V_{OPP}	The maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent D.C. output voltage is set at a specified reference level.
Single-ended Output Voltage	V_{OS}	The signal voltage present between 1 output terminal and ground of an amplifier having differential outputs.
A.C. Unbalance Voltage	V_{OU}	The difference between the peak values of the A.C. voltages at the 2 outputs when the amplifier is operating in the maximum output voltage swing condition.
Differential Input Impedance	z_{id}	The small signal impedance between 2 ungrounded input terminals of a differential amplifier.
Differential Output Impedance	z_{od}	The small signal impedance between 2 ungrounded output terminals of a differential amplifier.
Single-ended Output Impedance	z_{os}	The small signal impedance between 1 output terminal of a differential amplifier and ground with the other output terminal A.C. grounded.
Input Bias Current Temperature Sensitivity	$\Delta I_{IB}/\Delta T$	The ratio of the change in the input bias current to the change in circuit temperature for a constant output voltage. This is an average value for a specified current range.
Input Offset Current Temperature Sensitivity	$\Delta I_{IO}/\Delta T$	The ratio of the change of input offset current to the change of circuit temperature for a constant output voltage. This is an average value for a specified current range.

PARAMETER	SYMBOL	DEFINITION
Input Offset Voltage Temperature	$\Delta V_{IO}/\Delta T$	The ratio of the change of input offset voltage to the change of circuit temperature for a constant output voltage. This is an average value for a specified temperature range.
Phase Margin	ϕm	A figure equal to 180° minus the absolute value of the phase shift measured around the loop at that frequency at which the magnitude of the loop gain is unity.
	V_{DD}	Most positive supply voltage terminal.
	V_{SS}	Most negative supply voltage terminal.
	I_{DD}	Quiescent device current.
	V_{NL}	Noise immunity voltage low level.
	V_{NH}	Noise immunity voltage high level.
	I_{DN}	Output drive current N-channel.
	I_{DP}	Output drive current P-channel.
	V_{THN}	Threshold voltage N-channel.
	V_{THP}	Threshold voltage P-channel.
	C_{IN}	Input capacitance.
	$f_{(CL)}$	Clock frequency.

2.3 CUSTOM BUILT OR APPLICATION SPECIFIC INTEGRATED CIRCUITS

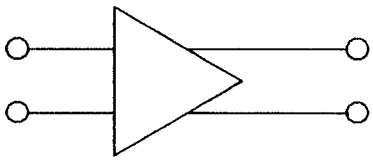
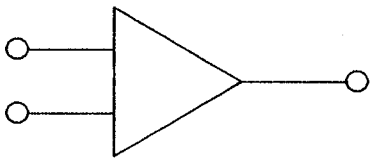
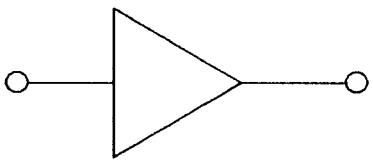
TERM	DEFINITION
Netlist	A description, in the form of an alphanumeric list, of a network of logical or electronic devices giving function and interrelationship of the constituent parts. The description is as detailed as required by the level of abstraction chosen. The most common levels encountered in computer aided design for integrated circuits are: - Functional Netlist Objects: - Functional units (logic gates/functions, standard cells...). Relations: - Logical interconnection of the terminals of the objects contained in the set. - Discrete Netlist Objects: - "Discrete" devices (transistors, diodes, resistors, capacitors...). Relations: - Electrical interconnection of device terminals. - Full Netlist Objects: - As discrete netlist + terminal characterisation (I/P, O/P, tristate...). Relations: - As discrete netlist + interconnect specifics (signal, power, ground, length, capacity...).

TERM	DEFINITION
Layout	Geometrical representation of mask levels of an integrated circuit.
Physical Design	Circuit design technique(s), comprising electrical and geometrical rules and parameters, to implement circuitry. The set of rules is derived from, and are required by, the manufacturing process in order to achieve a specified functionality, reliability and yield. The rules define shape, size and relative location of devices and structures and any necessary restrictions on their application.
Design System	A computer based system featuring dedicated programmes for the design of integrated electronic devices. Depending on the scope and maturity of the system, it is composed of programmes supporting areas of design activity including: - System: - Behavioral definition level. - Logic: - NOR, NAND ... - Circuit: - Electrical circuit definition level, strongly dependent on targeted technology e.g. MOS, TTL, ECL ... - Layout: - Geometrical definition level, strongly technology dependent. - Floorplanning: - Topological definition level, layout design on system level. - Testing: - Testability checker, test pattern generator, fault simulator, test coverage calculation... These areas are in fact handled by software packages incorporating human interface(s), simulators, rule checkers, circuit interfaces and other utilities.
IC Design Methodology	This can be classified into 2 basic approaches:- (a) Full custom design for "optimal" results. (b) Semi-custom design for economical design of application specific integrated circuits. Approach (a) builds a design virtually from scratch and has the vernacular title of "polygon pushing". Approach (b) utilises a certain degree of prefabrication, thereby limiting the range of possible solutions. The degree of prefabrication is highest in the classical gate array which employs a wafer whose design is pre-arranged up to the polysilicon mask, leaving only the metallisation layers for customisation. More flexibility, and room for optimisation, is offered by the standard cell approach and its derivatives. The latter makes use of pre-designed circuitry down to the layout level but does not involve the prefabricated wafers.
Gate Array Master	Incompletely manufactured IC featuring transistors, contact holes and all other structures except the metallisation.
Human Interface	Structured graphical and/or textual communication channel between User and system.
Elementary Cell	Smallest repetitive arrangement of transistors, contacts and dedicated routing on an array master.

TERM	DEFINITION
Subcell	Basic piece of circuitry (itself not comprising other subcells) used to assemble or compile more complex circuits.
Macrocell	Circuit/layout assembled or compiled from subcells.
Parametrisable Cell	Circuit/layout assembled or compiled from subcells according to geometrical function and performance parameters set by the designer.
Postprocessing	Any action required to complete a particular task outside of the original programme, or any intermediate or preparatory work necessary to start another processing step.
Sheet Capacitance	Capacitance per unit area as calculated or measured for a conductive layer in a distance of at least 1 times the thickness of the layer away from its edge.
Edge Capacitance	Capacitance per unit length of the edge of a conductive layer accounting for the contribution of the surface perpendicular to the reference plane.

3. GRAPHICAL SYMBOLS

Amplifier Types (1)

SYMBOL	DESCRIPTION
	Differential, video, RF general purpose
	Operational wide band, IF, audio frequency
	Audio frequency Video, IF, RF, wide band, HF general purpose

NOTES

1. Digital (logic) types to be defined.