(19) Europäisches Patentamt
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(11) **EP 1 041 610 A1**

(43) Date of publication:
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(21) Application number: **98950452**
(22) Date of filing: **29.10.1998**

(51) Int. Cl. **H01L 21/20** , H01L 21/205, H01L 21/203, H01L 21/208, H01L 33/00, H01S 3/18, C01B 21/06

(87) International publication number:
WO 99/23693 (04.10.2000 Gazette **/**)**

(84) Designated Contracting States:
DE FR GB
(30) Priority: **30.10.1997 JP 29830097**
20.01.1998 JP 900898
14.04.1998 JP 10254698
(71) Applicant: **Sumitomo Electric Industries, Ltd.**

(72) Inventors:
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- **OKAHISA, Takuji Itami Works of Sumitomo Electric**
- **MATSUMOTO, Naoki Itami Works of Sumitomo Electric**

(54) **GaN SINGLE CRYSTALLINE SUBSTRATE AND METHOD OF PRODUCING THE SAME**

Patent published on CD-ROM : **ESPACE 00/051**

(57) The method of making a GaN single crystal substrate comprises a mask layer forming step of forming on a GaAs substrate 2 a mask layer 8 having a plurality of opening windows 10 disposed separate from each other; and an epitaxial layer growing step of growing on the mask layer 8 an epitaxial layer 12 made of GaN.

(19) Europäisches Patentamt
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(11) **EP 1 034 325 A1**

(43) Date of publication:
13.09.2000 Bulletin **/****
(21) Application number: **98950142**
(22) Date of filing: **15.10.1998**

(51) Int. Cl. **C30B 25/02**, H01L 33/00, C30B 29/40
(87) International publication number:
WO 99/20816 (13.09.2000 Gazette **/**)**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
(30) Priority: **20.10.1997 FR 9713096**
(71) Applicant: **CENTRE NATIONAL DE LA RECHERCHE SCIENTIFIQUE (CNRS)**

(72) Inventors:
- **BEAUMONT, Bernard**
- **GIBART, Pierre**
- **GUILLAUME, Jean-Claude**
- **HAFFOUZ, Soufien**
- **NATAF, Gilles**
- **VAILLE, Michel**

(54) **METHOD FOR PRODUCING A GALLIUM NITRIDE EPITAXIAL LAYER**

(87) **This international application for which the EPO is a designated office has not been republished by the EPO according to article 158(1) EPC.**

Cette demande internationale pour laquelle l'OEB est office désigné n'a pas été republiée par l'OEB en vertu de l'article 158(1) CBE.

Diese internationale Anmeldung, für die das EPA Bestimmungsamt ist, würde, gemäß Artikel 158(1) EPÜ, vom EPA nicht wieder veröffentlicht.

Patent published on CD-ROM : **ESPACE 00/046, FIRST 00/005, FIRST 99/002, WORLD 99/065**

(57) The invention concerns a method for producing a gallium nitride (GaN) epitaxial layer characterised in that it consists in depositing on a substrate a dielectric layer acting as a mask and depositing on the masked gallium nitride, by epitaxial deposit, so as to induce the deposit of gallium nitride patterns and the anisotropic lateral growth of said patterns, the lateral growth being pursued until the different patterns coalesce. The deposit of the gallium nitride patterns can be carried out ex-situ by dielectric etching or in-situ by treating the substrate for coating it with a dielectric film whereof the thickness is of the order of one angstrom. The invention also concerns the gallium nitride layers obtained by said method.

(57) La présente invention concerne un procédé de réalisation d'une couche épitaxiale de nitrure de gallium (GaN) caractérisé en ce qu'il comprend le dépôt sur un substrat d'une couche de diélectrique fonctionnant comme un masque et la reprise du substrat masqué par du nitrure de gallium, dans des conditions de dépôt par épitaxie, de façon à induire le dépôt de motifs de nitrure de gallium et la croissance anisotrope et latérale desdits motifs, la croissance latérale étant poursuivie jusqu'à la coalescence des différents motifs. Le procédé de dépôt de motifs de nitrure de gallium peut être effectué ex situ par gravure de délectrique ou in situ par traitement du substrat consistant à recouvrir celui-ci par un film diélectrique dont l'épaisseur est de l'ordre de l'angström. L'invention concerne également les couches de nitrure de gallium susceptibles d'être obtenues par le procédé.

(19) Europäisches Patentamt
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(11) **EP 1 007 771 A1**

(43) Date of publication:
14.06.2000 Bulletin **/****
(21) Application number: **98935545**
(22) Date of filing: **02.07.1998**

(51) Int. Cl. **C30B 2 3/04** , C30B 25/04, C30B 25/18, C30B 29/40
(87) International publication number:
WO 99/01594 (14.06.2000 Gazette **/**)**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
(30) Priority: **03.07.1997 US 51688 P**
03.07.1997 US 51816 P

(71) Applicant: **CBL Technologies**

(72) Inventor: **SOLOMON, Glenn, S.**

(54) **THERMAL MISMATCH COMPENSATION TO PRODUCE FREE STANDING SUBSTRATES BY EPITAXIAL DEPOSITION**

(87) **This international application for which the EPO is a designated office has not been republished by the EPO according to article 158(1) EPC.**

Cette demande internationale pour laquelle l'OEB est office désigné n'a pas été republiée par l'OEB en vertu de l'article 158(1) CBE.

Diese internationale Anmeldung, für die das EPA Bestimmungsamt ist, würde, gemäB Artikel 158(1) EPÜ, vom EPA nicht wieder veröffentlicht.

Patent published on CD-ROM : **ESPACE 00/028, FIRST 00/003, FIRST 99/001, WORLD 99/005**

(57) A method for producing thick, high quality GaN substrates uses an epitaxially deposited film and is used as a substrate material for further device or epitaxial processing. The film (11) is deposited using an epitaxial technique on a thin substrate called the disposable substrate (10). The deposited film is thick enough so that upon cooling the thermal mismatched strain is relieved through cracking of the lower disposable substrate and not the newly deposited epitaxy. The epitaxial film now becomes a platform for either further epitaxial deposition or device processing.

(57) La présente invention concerne un procédé de production de substrats GaN épais de grande qualité comportant une couche déposée par épitaxie utilisée comme matériau de substrat pour un nouveau dispositif ou traitement épitaxique. La couche (11) est déposée sur un substrat mince appelé substrat jetable (10), en utilisant une technique épitaxique. La couche déposée est assez épaisse, de sorte que lors du refroidissement, la contrainte du déséquilibre thermique est réduite par la fissuration du substrat inférieur jetable et non par celle de l'épitaxie fraîchement déposée. La couche épitaxique devient ainsi une plate-forme, soit pour un nouveau dépôt épitaxique, soit pour un nouveau traitement de dispositif.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 1 001 468 A1**

(43) Date of publication:
17.05.2000 Bulletin **/****

(51) Int. Cl. **H01L 2 9/51**

(21) Application number: **99308690**

(22) Date of filing: **02.11.1999**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **12.11.1998 US 190193**

(71) Applicant: **LUCENT TECHNOLOGIES INC.**

(72) Inventors:
- **Hong, Minghwei**
- **Kortan, Ahmet Refik**
- **Kwo, Jueinai Raynien**
- **Mannaerts, Joseph Petrus**

(54) Rare earth oxide layer on a GaAs- or GaN-based semiconductor body

Patent published on CD-ROM : **ESPACE 00/023, FIRST 00/003**

(57) We have found that a single crystal, single domain oxide layer of thickness less than 5 nm can be grown on a (100) oriented GaAs-based semiconductor substrate. Similar epitaxial oxide can be grown on GaN and GaN-based semiconductors. The oxide typically is a rare earth oxide of the Mn2O3 structure (e.g., Gd2O3). The oxide/semiconductor interface can be of high quality, with low interface state density, and the oxide layer can have low leakage current and high breakdown voltage. The low thickness and high dielectric constant of the oxide layer result in a MOS structure of high capacitance per unit area. Such a structure advantageously forms a GaAs-based MOS-FET.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 0 987 741 A1**

(43) Date of publication:
22.03.2000 Bulletin **/****

(51) Int. Cl. **H01L 2 1/20**

(21) Application number: **99113574**

(22) Date of filing: **08.07.1999**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **14.09.1998 US 152848**

(71) Applicant: **Hewlett-Packard Company**

(72) Inventors:
- **Wang, Shih-Yuan**
- **Chen, Yong**

(54) **Method for relieving stress in GaN devices**

Patent published on CD-ROM : **ESPACE 00/013, FIRST 00/002**

(57) An improved method for growing a first layer[10, 30] on a second layer[12, 32] in which the first and second layers have different thermal indices of expansion and/or a mismatch of the lattice constants and the deposition being carried out at a temperature above ambient. The first layer[10, 30] includes a material that decomposes upon heating above a decomposition temperature. One of the first and second layers absorbs light in a first frequency range and the other of the first and second layers is transparent to the light in the first frequency range. In the method of the present invention, the one of the first and second layers that absorbs light in the first frequency range is exposed to light[14] in the first frequency range by passing the light through the other of the first and second layers. This exposure heats the first layer[10, 30] to a temperature above the decomposition temperature at the interface of the first and second layers after the first layer[10, 30] has been deposited on the second layer[12,32]. The decomposition can also mean to physically remove the material by means such as chemical etching. The present invention is well suited to the deposition of III-V semiconducting materials on substrates such as sapphire.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 0 972 097 A1**

(43) Date of publication:
19.01.2000 Bulletin **/****
(21) Application number: **98907295**
(22) Date of filing: **13.03.1998**

(51) Int. Cl. **C30B 3 3/00** , C30B 29/40
(87) International publication number:
WO 98/45511 (19.01.2000 Gazette **/**)**

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
(30) Priority: **04.04.1997 PL 31932997**
(71) Applicant: **Centrum badan Wysokocisnieniowych**

(72) Inventors:
- **GRZEGORY, Izabella**
- **NOWAK, Grzegorz**
- **POROWSKI, Sylwester**
- **WEYHER, Jan**

(54) **MECHANO-CHEMICAL POLISHING OF CRYSTALS AND EPITAXIAL LAYERS OF GaN AND Ga 1-x-yAl xIn yN**

(87) **This international application for which the EPO is a designated office has not been republished by the EPO according to article 158(1) EPC.**

Cette demande internationale pour laquelle l'OEB est office désigné n'a pas été republiée par l'OEB en vertu de l'article 158(1) CBE.

Diese internationale Anmeldung, für die das EPA Bestimmungsamt ist, würde, gemäB Artikel 158(1) EPÜ, vom EPA nicht wieder veröffentlicht.

Patent published on CD-ROM : **ESPACE 00/003, FIRST 00/001, FIRST 98/004, WORLD 98/124**

(57) This method of removal of irregularities and highly defected regions of the surface of crystals and epitaxial layers of GaN and Ga1-x-yAlxInyN characterized by mechano-chemical polishing on the soft polishing pad under pressure in presence of chemical etching agent of water solution of bases of the total concentration above 0.01N in time longer than 10 seconds after which the agent is replaced by the pure water without interruption of the polishing and polishing by at least 1 minute and subsequent diminution of the load and stopping of the machine and then the polished GaN crystal or GaA1InN epitaxial layer is removed of the polishing machine and dried in the stream of dry nitrogen.

(57) L'invention concerne un procédé d'enlèvement d'irrégularités et de zones très défectueuses de la surface de cristaux et de couches épitaxiales de GaN et de Ga1-x-yAlxInyN, lequel procédé est caractérisé par un polissage mécanochimique consistant à utiliser un tampon de polissage doux, sous pression, en présence d'un agent d'attaque chimique placé dans une solution aqueuse de bases dont la concentration totale est supérieure à 0,01N, et ce pendant une période supérieure à 10 secondes, puis à remplacer l'agent d'attaque par de l'eau pure, sans interrompre le polissage, à polir pendant au moins 1 minute, à diminuer ensuite la charge, à stopper la machine, à enlever alors de la machine de polissage le cristal de GaN ou la couche épitaxiale de GaA1InN, polis, et enfin à les sécher dans un courant d'azote sec.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 0 967 664 A1**

(43) Date of publication:
29.12.1999 Bulletin **/****

(51) Int. Cl. **H01L 33/00** , H01L 21/205

(21) Application number: **99110229**

(22) Date of filing: **26.05.1999**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **28.05.1998 JP 14771698**

(71) Applicant: **Sumitomo Electric Industries, Ltd.**

(72) Inventors:
- **Motoki, Kensaku**
- **Okahisa, Takuji**
- **Matsumoto, Naoki**
- **Matsushima, Masato**

(54) Gallium nitride single crystal substrate and method of producing the same

Patent published on CD-ROM : **ESPACE 99/097**

(57) An n-type GaN substrate having a safe n-type dopant instead of Si which is introduced by perilous silane gas. The safe n-dopant is oxygen. An oxygen doped n-type GaN free-standing crystal is made by forming a mask on a GaAs substrate, making apertures on the mask for revealing the undercoat GaAs, growing GaN films through the apertures of the mask epitaxially on the GaAs substrate from a material gas including oxygen, further growing the GaN film also upon the mask for covering the mask, eliminating the GaAs substrate and the mask, and isolating a freestanding GaN single crystal. The GaN is an n-type crystal having carriers in proportion to the oxygen concentration.

(19) Europäisches Patentamt
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Office européen des brevets

(11) **EP 0 966 047 A2**

(43) Date of publication:
22.12.1999 Bulletin **/****

(21) Application number: **99111739**

(22) Date of filing: **17.06.1999**

(51) Int. Cl. **H01L 33/00** , C30B 25/02, C30B 29/40

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **18.06.1998 JP 17127698**
30.06.1998 JP 18344698

(71) Applicant: **Sumitomo Electric Industries, Ltd.**

(72) Inventors:

- **Motoki, Kensaku, Sumitomo Electric Ind., Ltd.**
- **Okahisa, Takuji, Sumitomo Electric Ind., Ltd.**
- **Matsumoto, Naoki, Sumitomo Electric Ind., Ltd.**
- **Nishimoto, Tatsuya, Sumitomo Electric Ind., Ltd.**

(54) GaN single crystal substrate and method of producing same

Patent published on CD-ROM : **ESPACE 99/095**

(57) A freestanding GaN single crystal substrate is made by the steps of preparing a (111) GaAs single crystal substrate, forming a mask having periodically arranged windows on the (111) GaAs substrate, making thin GaN buffer layers on the GaAs substrate in the windows of the mask, growing a GaN epitaxial layer on the buffer layers and the mask by an HVPE or an MOC, eliminating the GaAs substrate and the mask away and obtaining a freestanding GaN single crystal substrate. The GaN single crystal has a diameter larger than 20mm and a thickness more than 0.07mm, being freestanding and substantially distortion-free.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 942 459 A1

(12) EUROPEAN PATENT APPLICATION

published in accordance with Art. 158(3) EPC

(43) Date of publication:
15.09.1999 Bulletin 1999/37

(21) Application number: **98912742.8**

(22) Date of filing: **09.04.1998**

(51) Int. Cl.[6]: **H01L 21/205**, H01L 33/00, C23C 16/34

(86) International application number:
PCT/JP98/01640

(87) International publication number:
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(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **11.04.1997 JP 9331597**
30.06.1997 JP 17449497
07.07.1997 JP 18107197
28.07.1997 JP 20147797
09.10.1997 JP 27744897
22.10.1997 JP 29009897
26.11.1997 JP 32499797

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- **KOZAKI, Tokuya-Nichia Chemical Industries, Ltd.**
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- **IWASA, Naruhito-Nichia Chemical Industries, Ltd.**
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(74) Representative:
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(54) METHOD OF GROWING NITRIDE SEMICONDUCTORS, NITRIDE SEMICONDUCTOR SUBSTRATE AND NITRIDE SEMICONDUCTOR DEVICE

(57) A method of growing a nitride semiconductor crystal which has very few crystal defects and can be used as a substrate is disclosed. This invention includes the step of forming a first selective growth mask on a support member including a dissimilar substrate having a major surface and made of a material different from a nitride semiconductor, the first selective growth mask having a plurality of first windows for selectively exposing the upper surface of the support member, and the step of growing nitride semiconductor portions from the upper surface, of the support member, which is exposed from the windows, by using a gaseous Group 3 element source and a gaseous nitrogen source, until the nitride semiconductor portions grown in the adjacent windows combine with each other on the upper surface of the selective growth mask.

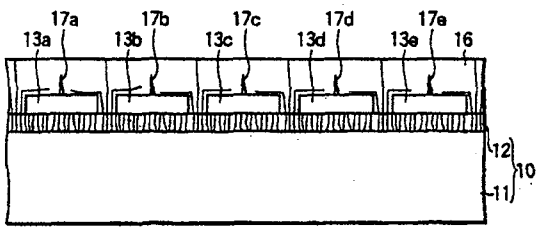

FIG. 1C

EP 0 942 459 A1

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 0 937 790 A2**

(43) Date of publication:
25.08.1999 Bulletin **/****

(51) Int. Cl. **C30B 2 3/00** , C30B 29/40

(21) Application number: **99101114**

(22) Date of filing: **21.01.1999**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **26.01.1998 JP 1264598**

(71) Applicants:
- **Sumitomo Electric Industries, Ltd.**
- **NISHINO, Shigehiro**

(72) Inventors:
- **Shiomi, Hiromu**
- **Tatsumi, Masami**
- **Nishino, Shigehiro**

(54) Method of making GaN single crystal and apparatus for making GaN single crystal

Patent published on CD-ROM : **ESPACE 99/061, FIRST 99/004**

(57) An apparatus comprises a Ga-disposing section in which Ga is disposed; a seed-crystal-disposing section in which a seed crystal of GaN is disposed; a synthesis vessel adapted to accommodate the Ga-disposing section, the seed-crystal-disposing section, and a gas containing nitrogen; heating means adapted to heat the Ga-disposing section and the seed-crystal-disposing section; and a control section for transmitting to the heating means a command for heating the Ga to an evaporation temperature of Ga or higher and heating the seed crystal to a temperature higher than that of the Ga, wherein the Ga evaporated by the heating means is adapted to react with the nitrogen of a nitrogen component in the gas so as to yield a GaN-forming gas, the GaN-forming gas being adapted to reach the seed-crystal-disposing section.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 887 436 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
30.12.1998 Bulletin 1998/53

(51) Int. Cl.[6]: **C23C 16/30**, C23C 16/34

(21) Application number: **98111626.2**

(22) Date of filing: **24.06.1998**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **25.06.1997 JP 168553/97**

(71) Applicant: **SONY CORPORATION**
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(72) Inventors:
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- **Hashimoto, Shigeki**
  Shinagawa, Tokyo (JP)
- **Nakamura, Fumihiko**
  Shinagawa, Tokyo (JP)
- **Yanashima, Katsunori**
  Shinagawa, Tokyo (JP)
- **Ikeda, Masao**
  Shinagawa, Tokyo (JP)

(74) Representative:
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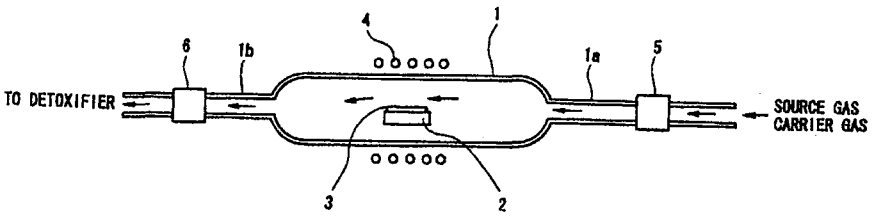
MÜLLER & HOFFMANN,
Innere Wiener Strasse 17
81667 München (DE)

(54) Method and apparatus for growth of a nitride III-V compound semiconductor

(57) It is intended to provide a method and apparatus for growing a high-quality nitride III-V compound semiconductor efficiently. A nitride III-V compound semiconductor, such as GaN or InGaN, is grown in a reaction tube of a MOCVD apparatus by setting the inner pressure of the reaction tube to a value not lower than 1.1 atmospheres, particularly, not lower than 1.1 atmospheres and not higher than two atmospheres, and more preferably not lower than 1.2 atmospheres and not higher than 1.8 atmospheres. The reaction tube is made of quartz glass or another material which is sufficiently resistive against a difference between inner and outer pressures.

Fig. 1



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(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 0 884 767 A2**

(43) Date of publication:
16.12.1998 Bulletin **/****

(51) Int. Cl. **H01L 21/20**

(21) Application number: **98110817**

(22) Date of filing: **12.06.1998**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **13.06.1997 DE 19725900**

(71) Applicants:
- **Strittmatter, André**
- **Bimberg, Dieter, Prof. Dr.**
- **Krost, Alois**

(72) Inventor: **Strittmatter, André**

(54) Method of epitaxy of gallium nitride on silicon substrates

Patent published on CD-ROM : **ESPACE 98/089, FIRST 98/005**

(57) Gallium nitride epitaxy on silicon In a process for gallium nitride epitaxy on a silicon substrate, an aluminium arsenide layer is applied between the substrate and the gallium nitride layer. A GaAs layer is preferably deposited on the aluminium arsenide layer and converted

to gallium nitride before gallium nitride deposition is completed and the aluminium arsenide layer is preferably partially or completely converted into an aluminium nitride layer in a nitrogen-rich atmosphere. The silicon substrate may be oriented with its surface normals in the crystallographic [100] direction (or equivalent directions) and its surface may be structured with V-shaped trenches having side faces oriented in the [111] direction (or equivalent directions). Alternatively, the silicon substrate may be oriented with its surface normals at 2-6 degrees to the crystallographic [100] direction (or equivalent directions).

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 0 881 666 A3**

(43) Date of publication A2:
02.12.1998 Bulletin **/****
(21) Application number: **98109371**
(22) Date of filing: **22.05.1998**

(51) Int. Cl. **H01L 33/00** , H01L 29/205, H01L 29/207

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
(30) Priority: **26.05.1997 JP 13540697**
(71) Applicant: **SONY CORPORATION**

(72) Inventors:

- **Asatsuma, Tsunenori**
- **Yanashima, Katsunori**
- **Miyajima, Takao**

(54) **P-type nitrogen compound semiconductor and method of manufacturing same**

Patent published on CD-ROM : **ESPACE 98/085, FIRST 98/005, ESPACE 99/061**

(57) A plurality of first layers made of AlGaN mixed crystal each having a thickness of the order of 1 to 100 nm and a plurality of second layers of p-type GaN with Mg each having a thickness of the order of 1 to 100 nm are alternately stacked. Since each of the first and second layers is thin, the stacked layers as a whole have properties of p-type AlGaN mixed crystal although the first layers do not include Mg and the second layers do not include Al. An Al source and a Mg source are temporally separated to be introduced in a stacking process. A reaction between the Al source and Mg source which may interfere desirable crystal growth is thereby prevented. Crystals of good quality are thus grown and electrical conductivity is thereby improved.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 0 871 208 A3**

(43) Date of publication A2:
14.10.1998 Bulletin **/****

(51) Int. Cl. **H01L 2 1/20**

(21) Application number: **97120023**

(22) Date of filing: **14.11.1997**

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **09.04.1997 US 833813**

(71) Applicant: **Hewlett-Packard Company**

(72) Inventors:

- **Chen, Yong**
- **Schneider, Richard P., Jr.**
- **Wang, Shih-Yun**

(54) **Reduction threading dislocations by amorphization and recrystalization**

Patent published on CD-ROM : **ESPACE 98/072, FIRST 98/004, ESPACE 98/088**

(57) A method for providing an epitaxial layer[14] of a first material over a substrate[11] comprising a second material having a lattice constant different from that of the first material. In the method of the present invention, a first layer of the first material is grown on the substrate[11]. A portion of the first layer is treated to render that portion amorphous. The amorphous portion is then annealed at a temperature above the recrystallization point of the amorphous portion, but below the melting point of the crystallized portion of the first layer thereby recrystallizing the amorphous portion of the first layer. The first layer may rendered amorphous by ion implantation. The method may be used to generate GaN layers on sapphire having fewer dislocations than GaN layers generated by conventional deposition techniques. ***<IMAGE>***

(19) Europäisches Patentamt
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(11) **EP 0 865 088 A2**

(43) Date of publication:
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(21) Application number: **98301948**

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(30) Priority: **14.03.1997 JP 8231997**
11.03.1998 JP 7833398

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- **Koukitu, Akinori**

(54) Epitaxial wafer having a gallium nitride epitaxial layer deposited on semiconductor substrate and method for preparing the same

Patent published on CD-ROM : **ESPACE 98/064, FIRST 98/004**

(57) The present invention provides an epitaxial wafer comprising a (111) substrate of a semiconductor having cubic crystal structure, a first GaN layer having a thickness of 60 nanometers or more, a second GaN layer having a thickness of 0.1μm or more and a method for preparing it. ***<IMAGE>***

(19) Europäisches Patentamt
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(11) **EP 0 864 672 A3**

(43) Date of publication A2:
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(21) Application number: **98301842**

(22) Date of filing: **12.03.1998**

(51) Int. Cl. **C30B 23/02** , C30B 29/40, C23C 16/34, C23C 16/44, H01L 21/205

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **13.03.1997 GB 9705233**

(71) Applicant: **Sharp Kabushiki Kaisha**

(72) Inventors:

- **Hooper, Stewart**
- **Kean, Alistair**
- **Duggan, Geoffrey**

(54) Molecular beam epitaxy method

Patent published on CD-ROM : **ESPACE 98/063, FIRST 98/004, ESPACE 99/032**

(57) An epitaxial deposit of GaN is formed on a substrate S by molecular beam epitaxy. The substrate S is located in a vacuum chamber 10 containing a heated support 12 for the substrate S. The chamber 10 is fitted with an exhaust conduit 16 and connected with an ultra high vacuum pump 14. An ammonia supply conduit 20 is adjustably mounted in the chamber 10. The inner end of the exhaust conduit 16 defines an exhaust outlet 18 of the chamber 10, whilst the first supply conduit 20 has an ammonia outlet 22 opening into the chamber 10. The outlet 22 and the vacuum outlet 18 are disposed adjacent the substrate S. The ammonia outlet 22 of the first supply conduit 20 is disposed nearer to the substrate S than those of conventionally positioned effusion cells 24 and 26 defining second and further supply conduits respectively for gallium and another elements to be supplied in elemental form to the vacuum chamber 10.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 0 846 791 A1**

(43) Date of publication:
10.06.1998 Bulletin **/****

(51) Int. Cl. **C30B 25/02** , C30B 29/40

(21) Application number: **97121460**

(22) Date of filing: **05.12.1997**

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **05.12.1996 JP 32526096**

(71) Applicant: **SONY CORPORATION**

(72) Inventors:

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- **Tomioka, Satoshi**

(54) Method for growing nitride III-V compound semiconductor layers and method for fabricating a nitride III-V compound semiconductor substrate

Patent published on CD-ROM : **ESPACE 98/039, FIRST 98/003**

(57) A method for growing nitride III-V compound semiconductor layers, comprises the steps of: growing a first BwAlxGaylnzN layer (where $0 \leq w \leq 1$, $0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq z \leq 1$ and $w+x+y+z=1$) on a substrate by first vapor deposition at a growth rate not higher than 4μm/h; and growing a second BwAlxGaylnzN layer (where $0 \leq w \leq 1$, $0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq z \leq 1$ and $w+x+y+z=1$) on the first BwAlxGaylnzN layer by second vapor deposition at a growth rate higher than 4μm/h and not higher than 200μm/h. A method for fabricating a nitride III-V compound semiconductor substrate, comprises the steps of: growing a first BwAlxGaylnzN layer (where $0 \leq w \leq 1$, $0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq z \leq 1$ and $w+x+y+z=1$) on a substrate by first vapor deposition at a growth rate not higher than 4μm/h; growing a second BwAlxGaylnzN layer (where $0 \leq w \leq 1$, $0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq y \leq 1$ and $w+x+y+z=1$) on the first BwAlxGaylnzN layer by second vapor deposition at a growth rate higher than 4μm/h and not higher than 200μm/h; and removing the substrate. ***<IMAGE>***

(19) Europäisches Patentamt
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(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
11.11.1998 Bulletin 1998/46

(43) Date of publication A2:
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(21) Application number: **97303785.6**

(22) Date of filing: **03.06.1997**

(51) Int Cl.[6]: **C30B 23/02**, C30B 29/38

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **04.06.1996 JP 141236/96**
11.04.1997 JP 94078/97

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(54) Single crystal of nitride and process for preparing it

(57) A single crystal of a nitride having a length of not less than 10 mm, a width of not less than 10 mm and a thickness of not less than 300 μm, or having a length of not less than 20 mm and a diameter of not less than 10 μm. In the production of the single crystal, either a mixed powder composed of a nitride powder and an oxide powder or an amorphous nitride powder is provided as a source material powder, the source material powder is heated in a nitrogen atmosphere or in a nitrogen atmosphere containing hydrogen and/or carbon at a temperature below the sublimation temperature or melting temperature of the nitride to decompose and vaporize the nitride powder, and the decomposed and vaporized component is subjected to crystal growth from the vapor phase on a substrate. The nitride single crystal is useful as a bulk material for heat sinks, electric and electronic components, such as semiconductors, optical components, and components of electric equipment and office automation equipment.

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(19) Europäisches Patentamt
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(43) Date of publication:
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(51) Int. Cl. **C30B 23/02** , C30B 29/40

(21) Application number: **97303690**

(22) Date of filing: **02.06.1997**

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **01.06.1996 GB 9611471**

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- **Hooper, Stewart Edward**
- **Duggan, Geoffrey**
- **Cheng, Tin Sun**
- **Foxon, Charles Thomas Bayley**

(54) Method of forming a compound semiconductor film

Patent published on CD-ROM : **ESPACE 97/073, FIRST 97/009**

(57) A method of forming a smooth, continuous GaN film in which Ga is caused to arrive at a sapphire substrate in accordance with a first arrival rate profile over a growth period during which said film is formed, and nitrogen is caused to arrive at said substrate in accordance with a second arrival rate profile over said growth period. The first and second arrival rate profiles are such that the Ga and N are caused to arrive simultaneously at the substrate over said growth period and so that (i) during an initial part of said growth period, growth of the film takes place under a stoichiometric excess of Ga and (ii) during a subsequent part of the growth period, growth of the film takes place under a stoichiometric excess of N. ***<IMAGE>***

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 0 801 156 A2**

(43) Date of publication:
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(51) Int. Cl. **C30B 25/02** , C30B 29/40, H01L 21/205

(21) Application number: **97302033**

(22) Date of filing: **25.03.1997**

(84) Designated Contracting States:
DE FR GB

(30) Priority: **25.03.1996 JP 6776296**
21.03.1997 JP 8757097

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- **Matsushima, Masato, Sumitomo Electric Ind. Ltd.**
- **Miura, Yoshiki, Sumitomo Electric Industries Ltd.**
- **Motoki, Kensaku, Sumitomo Electric Industries Ltd.**
- **Seki, Hisashi**
- **Koukitu, Akinori**

(54) Process for vapor phase epitaxy of compound semiconductor

Patent published on CD-ROM : **ESPACE 97/063, FIRST 97/008**

(57) The present invention provides a process for forming a high quality epitaxial compound semiconductor layer of indium gallium nitride<x<1) on a substrate (1).

nitrideepitaxially
galliumepitaxial
GaN

(19) Europäisches Patentamt
European Patent Office
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(11) **EP 0 720 240 A2**

(43) Date of publication:
03.07.1996 Bulletin **/****

(51) Int. Cl. **H01L 3 3/00** , H01L 21/205

(21) Application number: **95120238**

(22) Date of filing: **21.12.1995**

(84) Designated Contracting States:
DE FR GB NL

(30) Priority: **26.12.1994 JP 33779794**
27.03.1995 JP 6804895

(71) Applicant: **SUMITOMO ELECTRIC INDUSTRIES, LTD.**

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- **Matsushima, Masato, c/o Sumitomo Elec. Ind., Ltd**
- **Matsubara, Hideki, c/o Sumitomo Elec. Ind., Ltd**
- **Takagishi, Shigenori, c/o Sumitomo Elec. Ind., Ltd**
- **Seki, Hisashi**
- **Koukitu, Akinori**

(54) Epitaxial wafer and method of preparing the same

Patent published on CD-ROM : **ESPACE 96/036, FIRST 96/005**

(57) Provided are an epitaxial wafer of high performance which is applicable to a light emitting device, for example, and a method which can industrially prepare the same. The epitaxial wafer comprises a substrate (1) of a compound semiconductor selected from a group consisting of GaAs, GaP, InAs and InP, a buffer layer (2), consisting if GaN, of 10 nm to 80 nm in thickness which is formed on the substrate (1), and an epitaxial layer (3), containing GaN, which is formed on the buffer layer (2). The buffer layer (2) is formed at a first temperature by organic metal chloride vapor phase epitaxy, while the epitaxial layer (3) is formed at a second temperature, which is higher than the first temperature, by the organic metal chloride vapor phase epitaxy.

<IMAGE>

(19) Europäisches Patentamt
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(11) **EP 0 713 542 A1**

(43) Date of publication:
29.05.1996 Bulletin **/****
(21) Application number: **94913850**
(22) Date of filing: **27.04.1994**

(51) Int. Cl. **C30B 1 1/00** , C30B 11/12, C30B 29/40
(87) International publication number:
WO 95/04845 (29.05.1996 Gazette **/**)**

(84) Designated Contracting States:
AT BE CH DE DK ES FR GB GR IE IT LI LU MC NL PT SE
(30) Priority: **10.08.1993 PL 30001993**
(71) Applicant: **Centrum badan Wysokocisnieniowych**

(72) Inventors:
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- **JUN, Jan**
- **GRZEGORY, Izabella**
- **KRUKOWSKI, Stanislaw**
- **WROBLEWSKI, Miroslaw**

(54) **CRYSTALLINE MULTILAYER STRUCTURE AND MANUFACTURING METHOD THEREOF**

(87) **This international application for which the EPO is a designated office has not been republished by the EPO according to article 158(1) EPC.**

Cette demande internationale pour laquelle l'OEB est office désigné n'a pas été republiée par l'OEB en vertu de l'article 158(1) CBE.

Diese internationale Anmeldung, für die das EPA Bestimmungsamt ist, würde, gemäß Artikel 158(1) EPÜ, vom EPA nicht wieder veröffentlicht.

Patent published on CD-ROM : **ESPACE 96/028, FIRST 96/004, FIRST 95/001, WORLD 95/013**

(57) A process for fabricating a multilayer crystalline structure of nitrides of metals from group III of periodic table including GaN, AlN and InN is provided. The process includes the steps of heating a group III metal (26) to a temperature T1 under an equilibrium nitrogen pressure while maintaining group III metal nitride stability to form a first crystal layer of the group III metal nitride. Thereafter the method includes the step of forming a second crystal layer (28) of the group III metal nitride by decreasing the nitrogen pressure such that the second crystal layer grows on the first layer with a growth rate slower than the growth rate of the first layer at a temperature T2 not greater than temperature T1. The second layer (28) grows on at least a portion of the first layer at a predetermined thickness under the new nitrogen pressure.

(57) Procédé de fabrication d'une structure multicouche cristalline de nitrures de métaux du groupe III du tableau périodique, notamment le GaN, l'AiN et l'InN. Le procédé consiste à porter un métal du groupe III (26) à une température (T1) sous une pression d'équilibre d'azote, et simultanément à préserver la stabilité du nitrure du métal du groupe III, de manière à former une première couche cristalline du nitrure du métal du groupe III; puis à former une seconde couche cristalline (28) du nitrure du métal du groupe III par réduction de la pression de l'azote de manière à provoquer la croissance de la seconde couche cristalline sur la première couche à une vitesse inférieure à la vitesse de croissance de la première couche, et à une température (T2) égale ou inférieure à la température (T1). La croissance de la seconde couche (28) se produit sur au moins une partie de la première couche et selon une épaisseur prédéterminée sous la nouvelle pression d'azote.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 0 711 853 A1**

(43) Date of publication:
15.05.1996 Bulletin **/****
(21) Application number: **95914510**
(22) Date of filing: **05.04.1995**

(51) Int. Cl. **C30B 2 3/00** , H01L 21/203
(87) International publication number:
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(84) Designated Contracting States:
DE FR GB
(30) Priority: **08.04.1994 JP 9396394**
16.09.1994 JP 24680394
(71) Applicant: **JAPAN ENERGY CORPORATION**

(72) Inventors:
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(54) METHOD FOR GROWING GALLIUM NITRIDE COMPOUND SEMICONDUCTOR CRYSTAL, AND GALLIUM NITRIDE COMPOUND SEMICONDUCTOR DEVICE

Patent published on CD-ROM : **ESPACE 96/025, FIRST 96/004, FIRST 95/006, WORLD 95/071**

(57) In a method for growing a gallium nitride semiconductor crystal on a single-crystal substrate, the (011) or (101) face of perovskite containing group 13 (3B) rare-earth elements is used as the single-crystal substrate, so that a gallium nitride semiconductor crystal having an excellent crystallinity is formed on the surface of the substrate by epitaxial growth.

(57) Procédé de tirage d'un cristal semi-conducteur à base de nitrure de gallium sur un substrat monocristallin, selon lequel la face (011) ou (101) d'éléments de terres rares 13 (3B) du groupe contenant de la pérovskite est utilisé comme substrat monocristallin, de sorte que l'on obtient par croissance épitaxiale un cristal semi-conducteur de nitrure de gallium présentant un excellente cristallinité sur la surface du substrat.

(19) Europäisches Patentamt
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(11) EP 0 647 730 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
28.01.1998 Bulletin 1998/05

(43) Date of publication A2:
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(21) Application number: **94115739.8**

(22) Date of filing: **06.10.1994**

(51) Int. Cl.[6]: **C30B 29/38**, H01L 21/00

(84) Designated Contracting States:
DE FR GB

(30) Priority: **08.10.1993 JP 253098/93**
31.03.1994 JP 62813/94
31.03.1994 JP 62815/94

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(54) GaN single crystal

(57) A GaN single crystal having a full width at half-maximum of the double-crystal X-ray rocking curve of 5-250 sec and a thickness of not less than 80 μm, a method for producing the GaN single crystal having superior quality and sufficient thickness permitting its use as a substrate and a semiconductor light emitting element having high luminance and high reliability, comprising, as a substrate, the GaN single crystal having superior quality and/or sufficient thickness permitting its use as a substrate.

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(19) Europäisches Patentamt
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(12) EUROPEAN PATENT APPLICATION

(21) Application number: **94106587.2**

(22) Date of filing: **27.04.94**

(51) Int. Cl.5: **H01L 33/00**, H01L 31/0224, H01L 21/28

(30) Priority: **28.04.93 JP 124890/93**
31.05.93 JP 129313/93
28.07.93 JP 207274/93
21.09.93 JP 234684/93
21.09.93 JP 234685/93
08.10.93 JP 253171/93
28.01.94 JP 8726/94
28.01.94 JP 8727/94

(43) Date of publication of application:
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(84) Designated Contracting States:
DE FR GB IT NL

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(54) Gallium nitride-based III-V group compound semiconductor device and method of producing the same.

(57) A gallium nitride-based III-V Group compound semiconductor device (10) has a gallium nitride-based III-V Group compound semiconductor layer (13) provided over a substrate (11), and an ohmic electrode (15) provided in contact with the semiconductor layer (13). The ohmic electrode (15) is formed of a metallic material, and has been annealed.

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(19) Europäisches Patentamt
European Patent Office
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(11) **EP 0 609 799 A3**

(43) Date of publication A2:
10.08.1994 Bulletin **/****
(21) Application number: **94101374**
(22) Date of filing: **31.01.1994**

(51) Int. Cl. **H01L 21/20** , H01L 21/36, C30B 25/18

(84) Designated Contracting States:
DE FR GB IT NL
(30) Priority: **02.02.1993 US 12556**
(71) Applicant: **TEXAS INSTRUMENTS INCORPORATED**

(72) Inventor: **Summerfelt, Scott R.**

(54) **Improvements in heteroepitaxy by large surface steps**

Patent published on CD-ROM : **ESPACE 94/056, FIRST 94/005, ESPACE 97/024**

(57) A method for heteroepitaxial growth and the device wherein a single crystal ceramic substrate 20, preferably Y stabilized zirconia, $MgAl_2O_4$, Al_2O_3, 3C-SiC, 6H-SiC or MgO is cut and polished at from about 1.0 to about 10 degrees off axis to produce a substantially flat surface. The atoms on the surface are redistributed on the surface to produce surface steps 22 of at least three lattice spacings. An optional epitaxially grown ceramic buffer layer, preferably AlN or GaN, is then formed on the substrate. Then a layer of semiconductor 24, preferably SiC, AlN when the buffer layer is used and is not AlN or GaN is grown over the substrate and buffer layer, if used. ***<IMAGE>***

(19) Europäisches Patentamt
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(11) **EP 0 576 566 A1**

(43) Date of publication:
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(21) Application number: **92908776**
(22) Date of filing: **18.03.1992**

(51) Int. Cl. **H01L 21/203**, H01L 21/205
(87) International publication number:
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(84) Designated Contracting States:
DE GB
(30) Priority: **18.03.1991 US 670692**

(71) Applicant: **TRUSTEES OF BOSTON UNIVERSITY**

(72) Inventor: **MOUSTAKAS, Theodore, D.**

(54) **A METHOD FOR THE PREPARATION AND DOPING OF HIGHLY INSULATING MONOCRYSTALLINE GALLIUM NITRIDE THIN FILMS**

Patent published on CD-ROM : **ESPACE 94/001, FIRST 94/001, FIRST 92/006, WORLD 92/040**

(57) This invention relates to a method of preparing highly insulating GaN single crystal films in a molecular beam epitaxial growth chamber. A single crystal substrate is provided with the appropriate lattice match for the desired crystal structure of GaN. A molecular beam source of Ga and source of activated atomic and ionic nitrogen are provided within the growth chamber. The desired film is deposited by exposing the substrate to Ga and nitrogen sources in a two step growth process using a low temperature nucleation step and a high temperature growth step. The low temperature process is carried out at 100-400 °C and the high temperature process is carried out at 600-900 °C. The preferred source of activated nitrogen is an electron cyclotron resonance microwave plasma.

(57) Procédé de préparation de couches monocristallines de GaN très isolant dans une chambre de croissance épitaxiale à faisceau moléculaire. On confère à un substrat monocristallin la structure en treillis appropriée pour obtenir la structure cristalline de GaN désirée. Une source de faisceaux moléculaires de Ga et une source d'azote atomique et ionique activé sont présentes dans la chambre de croissance. On dépose la couche désirée en exposant le substrat aux sources de Ga et d'azote dans un processus de croissance en deux étapes comprenant une étape de nucléation à basse température et une étape de croissance à haute température. Le processus à basse température est exécuté à 100-400 °C et le processus à haute température est exécuté à 600-900 °C. La source préférée d'azote activé est un plasma à micro-ondes de résonance produit par un cyclotron à électrons.

(19) Europäisches Patentamt
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(11) Publication number: **0 559 326 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 93300724.7

(51) Int. Cl.5: C30B 25/14, C23C 16/44

(22) Date of filing: 01.02.93

(30) Priority: 06.03.92 JP 49711/92

(43) Date of publication of application:
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(84) Designated Contracting States:
DE FR GB

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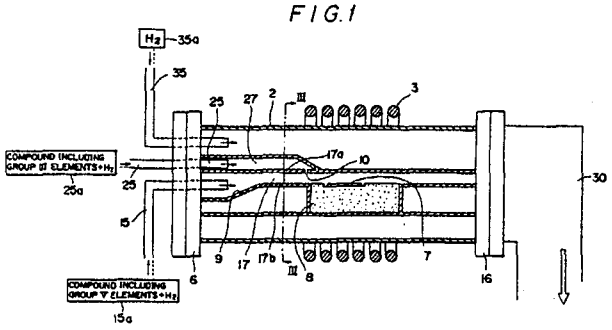
(54) Compound semiconductor vapor phase epitaxial device.

(57) A compound semiconductor vapor phase epitaxial device comprises a cylindrical reactor vessel (2), a plurality of flow channels (17, 27) disposed in the reactor vessel, a crystal substrate (7) disposed in one of the flow channels, a plurality of gas supply pipes for respectively supplying gas containing element of compound to be grown on the crystal substrate and at least one slit (10) or linearly arranged fine holes (P) communicating adjacent two flow channels so as to extend in a direction normal to a direction of the gas flow to form a laminate layer flow consisting of two or more than two gases at an upstream portion of location of the crystal substrate.

FIG.1



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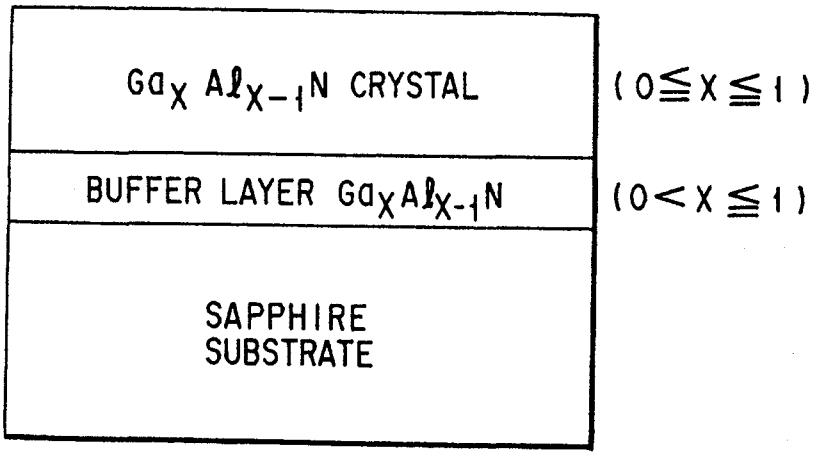
(54) **Crystal growth method for gallium nitride-based compound semiconductor.**

(57) Crystals of a gallium nitride-based compound semiconductor are grown on the surface of a buffer layer represented by formula $Ga_XAl_{1-X}N$ ($0 < X \leq 1$). The crystallinity of the gallium nitride-based compound semiconductor grown on the surface of the buffer layer can be drastically improved.



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(54) **Chambre de réacteur pour croissance épitaxiale en phase vapeur des matériaux semi-conducteurs.**

(57) Chambre de réacteur pour effectuer la croissance épitaxiale en phase vapeur de couches de matériaux semiconducteurs sur des substrats semiconducteurs (12), cette chambre contenant un porte-échantillon (11) pour le substrat (12), et chambre dans laquelle circule parallèlement au substrat des composés gazeux sous une pression et une température appropriées à obtenir la croissance épitaxiale des couches monocristallines sur le substrat, caractérisée en ce qu'elle est équipée d'un premier moyen consistant en un dispositif de chauffage piloté (30) de la partie de la paroi de la chambre opposée au porte-échantillon, cette partie de paroi étant dite plafond de la chambre, pour provoquer des variations du profil de température de ce plafond, d'un second moyen consistant en un dispositif de chauffage piloté du porte-échantillon pour provoquer des variations du profil de température de ce porte-échantillon indépendamment de celles du plafond de la chambre, et d'un troisième moyen consistant en un dispositif de rotation du porte-échantillon autour d'un axe perpendiculaire à son plan, ces trois moyens coopérant pour qu'en chaque point du substrat d'une part le taux de croissance soit uniforme et d'autre part la composition de la couche épitaxiale soit uniforme.

Application : Réalisation de composants discrets en semiconducteurs III-V

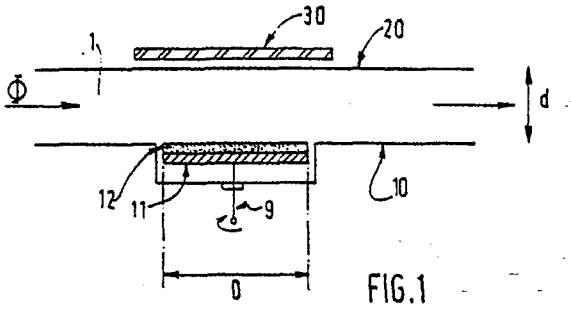

FIG.1

EP 0 231 544 A1