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Pages 1 to 23

TRANSISTORS, MICROWAVE, METAL

SEMICONDUCTOR FIELD EFFECT, POWER,

GALLIUM ARSENIDE

BASED ON TYPE CLY32

ESA/SCC Detail Specification No. 5614/006

space components
coordination group

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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a Transistor, Microwave, Metal Semiconductor Field Effect (MESFET), Power, Gallium Arsenide, based on Type CLY32. It shall be read in conjunction with ESA/SCC Generic Specification No. 5010, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type transistors specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the transistors specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The derating information applicable to the transistors specified herein is shown in Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the transistors specified herein are shown in Figure 2.

1.6 FUNCTIONAL DIAGRAM

The functional diagram, showing lead identification of the transistors specified herein, is shown in Figure 3.

1.7 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore suitable precautions shall be employed for protection during all phases of manufacture test, packaging, shipping and handling.

These components are catagorised as Class 2 with a Minimum Critical Path Failure Voltage of 1▮500V.

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESA/SCC Generic Specification No. 5010 for Discrete Microwave Semiconductor Components.

(b) MIL-STD-750, Test Methods for Semiconductor Devices.

TABLE 1(a) - TYPE VARIANTS

VARIANT	BASED ON TYPE	CASE	FIGURE	LEAD MATERIAL AND FINISH
01	CLY32	MWP25	2	D2

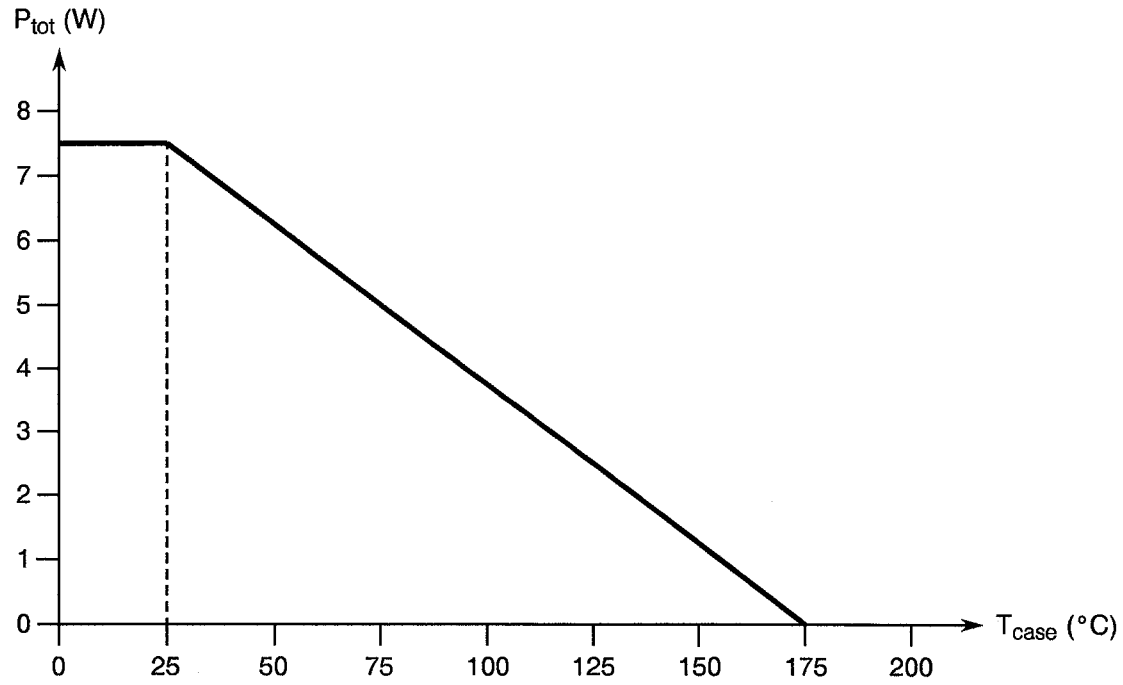
TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Drain-Source Voltage	V_{DS}	14	V	
2	Drain-Gate Voltage	V_{DG}	16	V	
3	Gate-Source Voltage	V_{GS}	−6.0	V	
4	Drain Current	I_D	1200	mA	
5	Compression Level	P_c	1.5 at V_{DS} = 9.0V 2.5 at V_{DS} = 8.0V 3.5 at V_{DS} = 7.0V	dB	Note 1
6	Power Dissipation	P_{tot}	7.5	W	Note 2
7	Channel Temperature Range	T_{ch}	- 65 to + 175	°C	
8	Storage Temperature Range	T_{stg}	−65 to +175	°C	
9	Soldering Temperature	T_{sol}	+230	°C	Note 3
10	Thermal Resistance	$R_{TH(J-S)}$	20	°C/W	

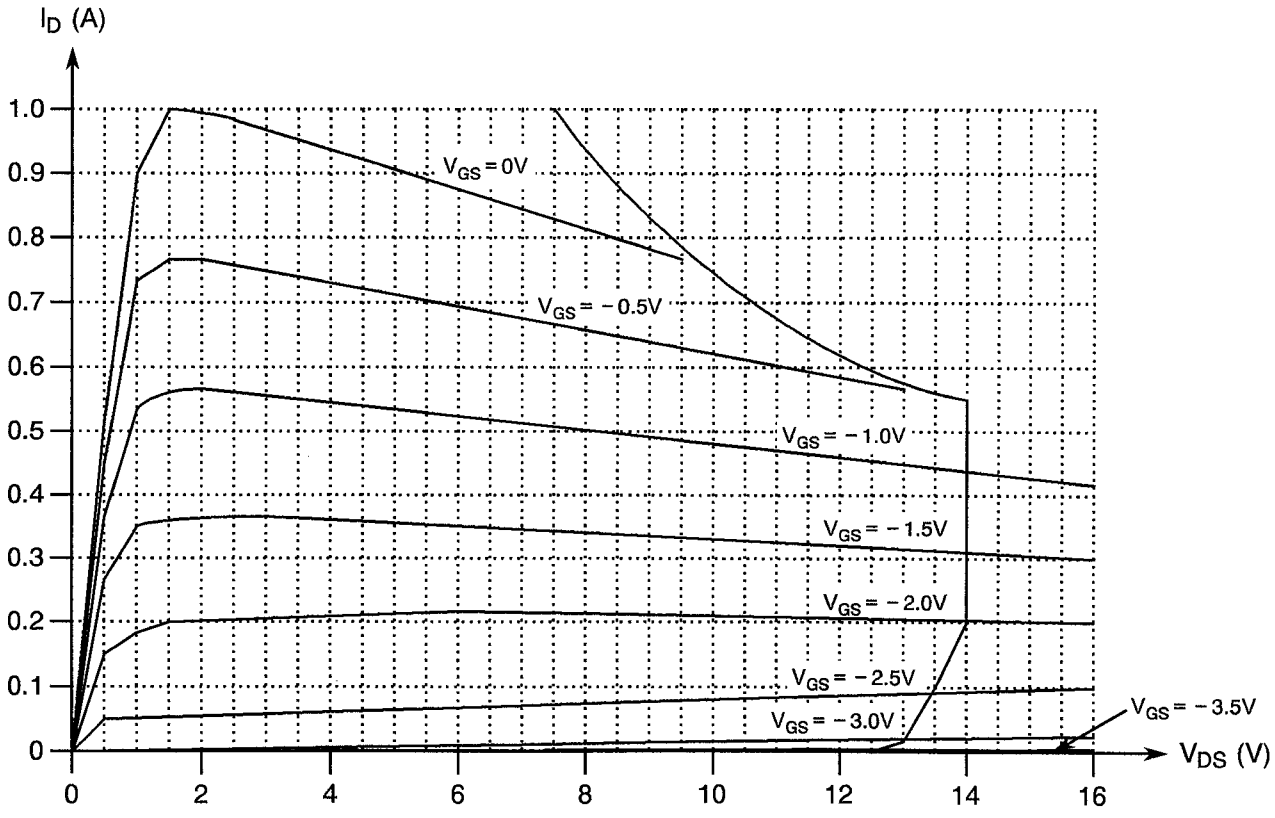
NOTES

1. $I_{DS} \geq I_{dss}$ x 0.35 and under continuous wave.
2. At T_{case} = +25°C. For derating at T_{case} > +25°C, see Figure 1.
3. Duration 15 seconds maximum at a distance of not less than 0.5mm from the device body and the same termination shall not be resoldered until 3 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION

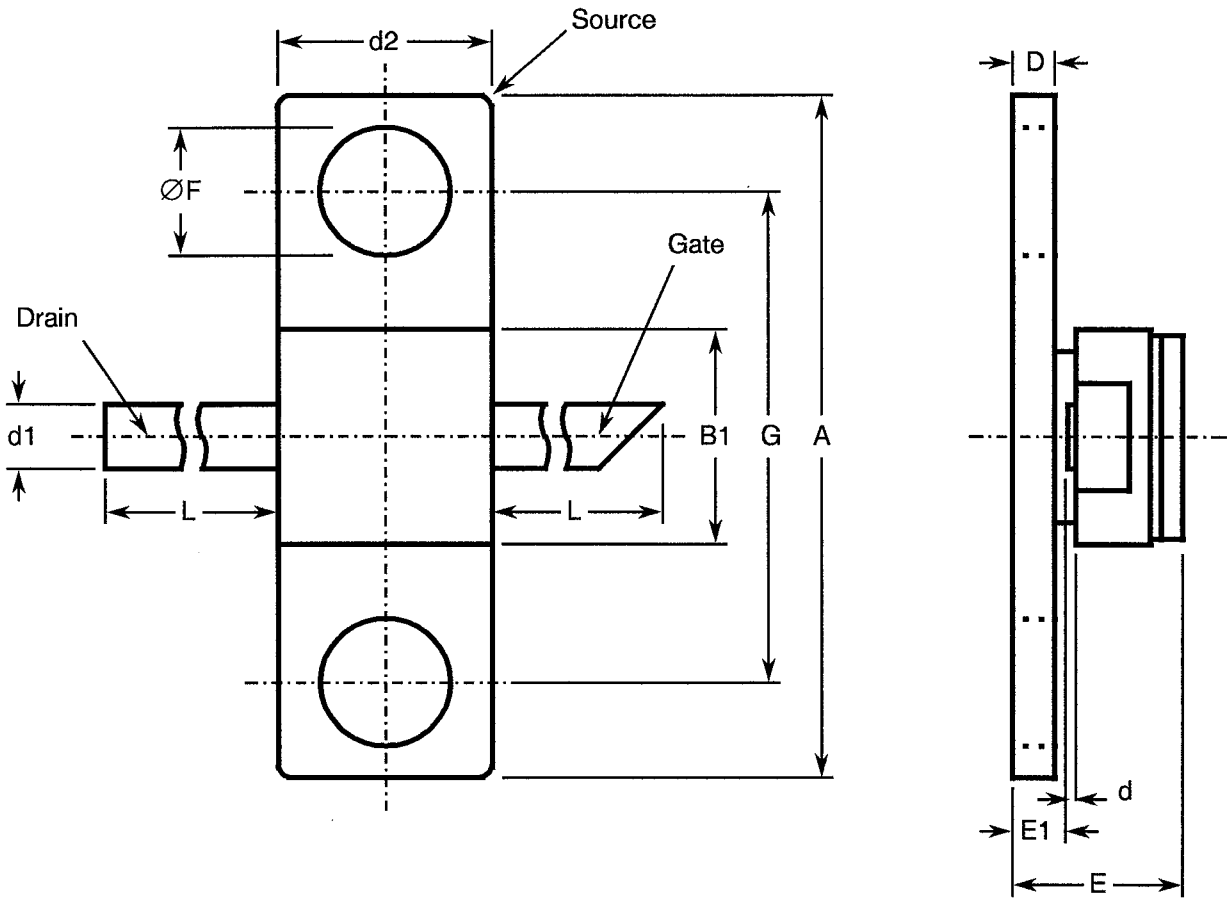


Power Dissipation versus Temperature



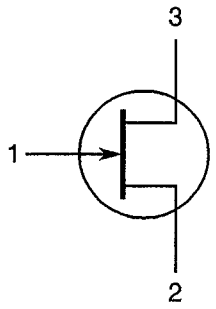
Drain Current vs Drain Source Voltage
(Typical behaviour, supplied for information only)

FIGURE 2 - PHYSICAL DIMENSIONS



SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	8.30	8.70	
B1	2.30	2.70	
d	0.09	0.15	
d1	0.50	0.70	
d2	2.30	2.70	
D	0.50	0.70	
E	1.80	2.20	
E1	0.70	0.90	
ØF	1.50	1.70	
G	6.00	6.20	
L	2.70	3.70	

FIGURE 3 - FUNCTIONAL DIAGRAM



1. Gate
2. Source
3. Drain

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following symbols are used:-

$R_{TH(J-S)}$ = Thermal Resistance, Junction to Soldering Point.
T_{ch} = Channel Temperature.
V_{DS} = Drain Source Voltage.
V_{GS} = Gate Source Voltage.
V_{DG} = Drain Gate Voltage.
I_D = Drain Current.
I_{DSS} = Drain Saturation Current.
V_{Gth} = Gate Threshold Voltage.
I_{Dp} = Drain Leakage Current at Pinch-off.
I_{Gp} = Gate Leakage Current at Pinch-off.
gm = Transconductance.
P_O = Power Outputs.
G_p = Power Gain.
ηadd = Power Added Efficiency.
I_{Do} = Operation Drain Current at Actual P_O.
I_{Go} = Operational Gate Current at Actual P_O.
I_{GD0} = Gate Drain Leakage Current.
P_c = Compression Level.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the transistors specified herein shall be as stated in this specification and ESA/SCC Generic Specification No. 5010 for Discrete Microwave Semiconductor Components. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

(a) Para. 5.3, Wafer Lot Acceptance: Shall be performed as an S.E.M. inspection only.

4.2.2 Deviations from Final Production Tests (Chart II)

(a) Para. 9.6, Constant Acceleration: Shall not be performed.

(b) Para. 9.7, Particle Impact Noise Detection (PIND) Test: May be performed at any point after the position indicated in Chart II.

(c) Para. 9.14, Vibration, Variable Frequency: Shall not be performed.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

(a) Para. 7.1.1(b), Power Burn-in 2 and Δ3 measurements: Shall be performed if drift after power burn-in 1 exceeds half of the allowed limit in Table 4 (applicable PDA: 5.0%).

For Level C, power burn-in 2 shall be performed for 168 hours if pre-burn-in is performed during Chart II.

(b) Para. 9.9.2, may be performed at any stage after power burn-in 2.

(c) Para. 9.9.3, may be performed at any stage after power burn-in 2.

4.2.4 Deviations from Qualification Tests (Chart IV)

(a) Para. 9.13, Shock Test: Shall not be performed.

(b) Para. 9.14, Vibration Test: Shall not be performed.

(c) Para. 9.15, Constant Acceleration: Shall not be performed.

(d) Para. 9.20, Operating Life: Shall be performed at 1 temperature only on 30 pieces.

(e) Para. 9.23, Special Testing: Shall not be performed.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

(a) Para. 9.13, Shock Test: Shall not be performed.

(b) Para. 9.14, Vibration Test: Shall not be performed.

(c) Para. 9.15, Constant Acceleration: Shall not be performed.

(d) Para. 9.20, Operating Life: Shall be performed at 1 temperature only on 16 pieces.

(e) Para. 9.23, Special Testing: Shall not be performed.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the transistors specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the transistors specified herein shall be 0.2 grammes.

4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Generic Specification No. 5010. The test conditions shall be as follows:-

(a) Condition: 'A' (Tension).

(b) Force: 2.2N.

(c) Duration: 5 seconds.

4.3.4 Bond Strength

The requirements for bond strength are specified in Section 9 of ESA/SCC Generic Specification No. 5010. The test conditions shall be as follows:-

(a) Condition: 'A'.

(b) Bond Strength: 0.03N force minimum.

4.3.5 Die Shear

The requirements for die shear are specified in Section 9 of ESA/SCC Generic Specification No. 5010. The test conditions shall be as follows:-

(a) Minimum acceptable die shear strength: 4.0N.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the transistors specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body.

4.4.2 Lead Material and Finish

The lead material shall be Type 'D' with Type '2' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500.

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700 and the following paragraphs. When the component is too small to accommodate all of the marking as specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence, shall be as follows:-

(a) Terminal Identification.

(b) The SCC Component Number.

(d) Traceability Information.

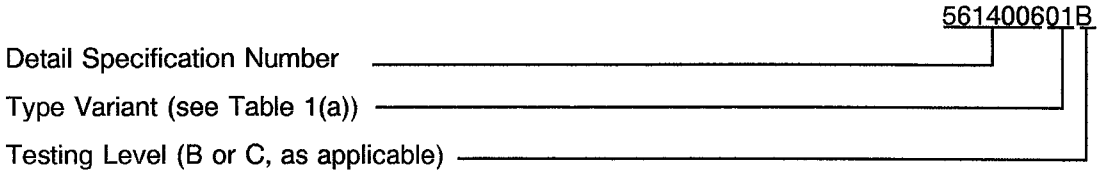
The primary package shall bear an "ESD sensitive" label.

4.5.2 Terminal Identification

Terminal identification shall be as shown in Figures 2 and 3 of this specification.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured at room temperature are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +140(+0-5)$°C.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Table 2 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

Burn-in shall be to Chart III(b).

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +25 \pm 3$ °C. The parameter drift values (Δ) applicable to the scheduled parameters shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-in

The requirements for high temperature reverse bias burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 5010. The conditions for high temperature reverse bias burn-in shall be as specified in Table 5(a) of this specification.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 5010. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for High Temperature Reverse Bias Burn-in

The circuit for use in performing the high temperature reverse bias burn-in test is shown in Figure 5(a) of this specification.

4.7.5 Electrical Circuits for Power Burn-in

The circuit for use in performing the power burn-in test is shown in Figure 5(b) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	Drain Saturation Current	I_{DSS}	4(a)	$V_{DS} = 3.0V$ $V_{GS} = 0V$	600	1200	mA
2	Gate Threshold Voltage	$-V_{Gth}$	4(a)	$V_{DS} = 3.0V$ $I_D = 10mA$	1.6	3.6	V
3	Drain Current at Pinch-off	I_{Dp}	4(a)	$V_{DS} = 3.0V$ $V_{GS} = -3.8V$	-	100	µA
4	Gate Leakage Current at Pinch-off	$-I_{Gp}$	4(a)	$V_{DS} = 3.0V$ $V_{GS} = -3.8V$	-	40	µA
5	Transconductance	gm	4(a)	$V_{DS} = 3.0V$ $I_D = 450mA$	300	-	mS
6	Gate Drain Leakage Current	$-I_{GD0}$	4(a)	$I_S = 0mA$ $V_{GD} = -16V$	-	400	µA

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
7	Output Power	P_O	4(b)	$V_{DS} = 9.0V$ $I_D = 450mA$ $f = 2.0GHz$ $P_{IN} = 21dBm$ Power matched	32	-	dBm
8	Power Added Efficiency	ηadd	4(b)	$V_{DS} = 9.0V$ $I_D = 450mA$ $f = 2.0GHz$ $P_{IN} = 21dBm$ Power matched	45	-	%
9	Operational Drain Current	I_{Do}	4(b)	$V_{DS} = 9.0V$ $I_D = 450mA$ $f = 2.0GHz$ $P_{IN} = 21dBm$ Power matched	350	-	mA
10	Operational Gate Current	I_{Go}	4(b)	$V_{DS} = 9.0V$ $I_D = 450mA$ $f = 2.0GHz$ $P_{IN} = 21dBm$ Power matched	-	10	mA

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
2	Gate Threshold Voltage	$-V_{Gth}$	4(a)	$V_{DS} = 3.0V$ $I_D = 10mA$	-	3.6	V
3	Drain Current at Pinch-off	I_{Dp}	4(a)	$V_{DS} = 3.0V$ $V_{GS} = -3.8V$	-	4.0	mA
4	Gate Leakage Current at Pinch-off	$-I_{Gp}$	4(a)	$V_{DS} = 3.0V$ $V_{GS} = -3.8V$	-	400	µA
5	Transconductance	gm	4(a)	$V_{DS} = 3.0V$ $I_D = 450mA$	240	-	mS

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - TEST CIRCUIT FOR d.c. PARAMETERS

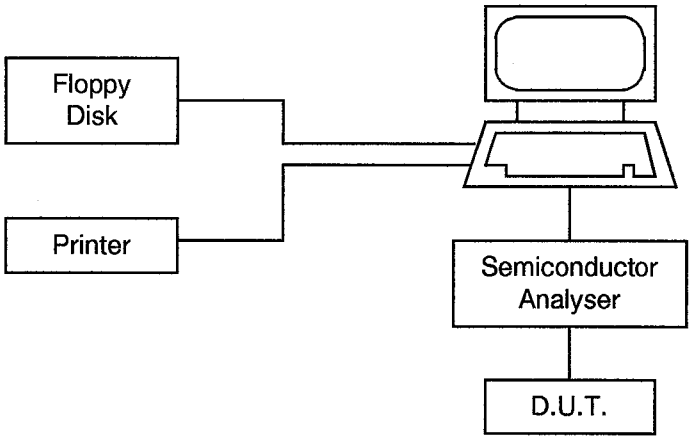
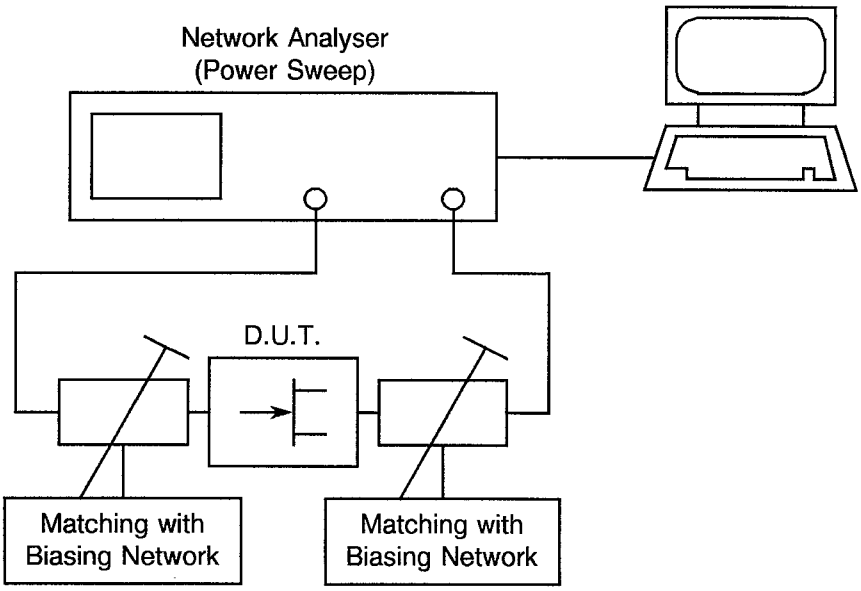


FIGURE 4(b) - TEST CIRCUIT FOR a.c. PARAMETERS



NOTES

1. d.c. Gate Resistance = 1.0kΩ.

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
1	Drain Saturation Current	I_{DSS}	As per Table 2	As per Table 2	±100	mA
2	Gate Threshold Voltage	$-V_{Gth}$	As per Table 2	As per Table 2	±200	mV
3	Drain Current at Pinch-off	I_{Dp}	As per Table 2	As per Table 2	±20	µA
4	Gate Leakage Current at Pinch-off	$-I_{Gp}$	As per Table 2	As per Table 2	±10	µA
5	Transconductance	gm	As per Table 2	As per Table 2	±20	mS
7	Output Power	P_O	As per Table 2	As per Table 2	±0.5	dBm

NOTES

1. $\Delta 1 = \Delta 2 = \Delta 3$.

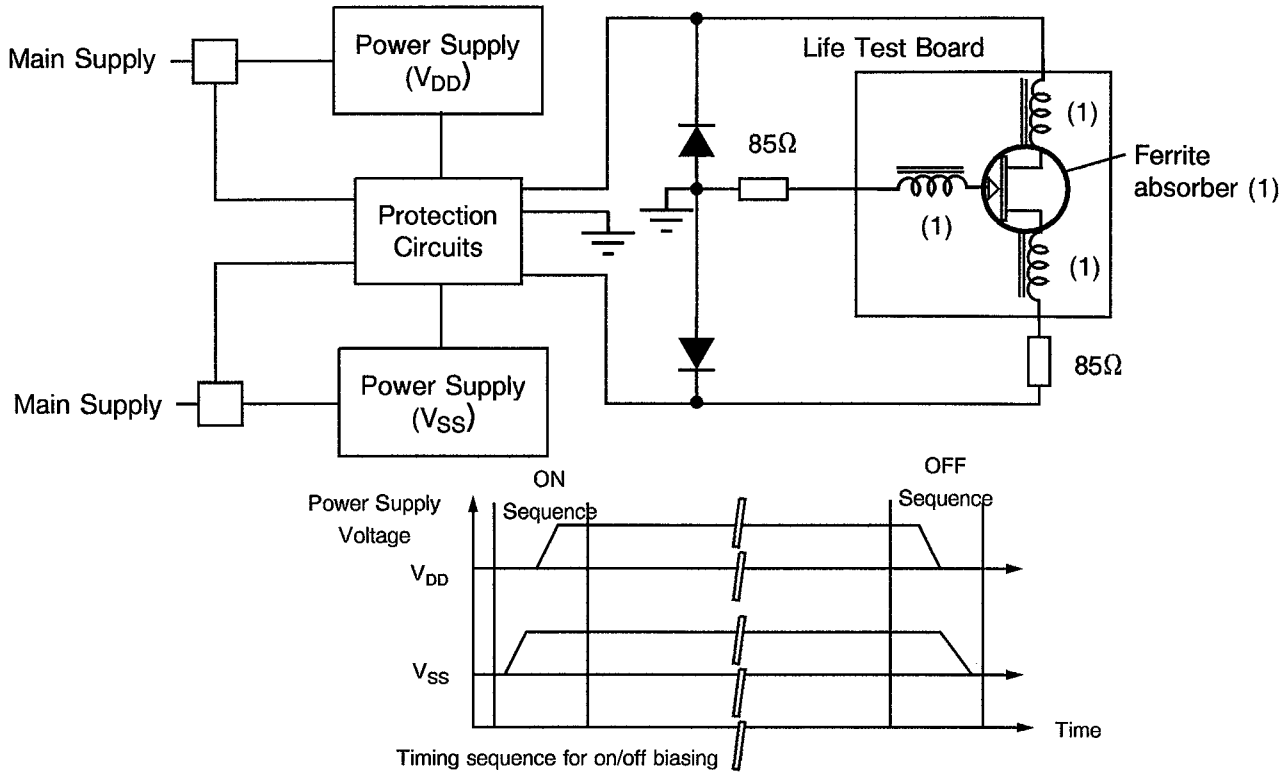
TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

No.	CHARACTERISTICS	SYMBOL	CONDITIONS	UNIT
1	Ambient Temperature	T_{amb}	+175(+0−5)	°C
2	Gate to Source Voltage	V_{GS}	−4.0	V
3	Drain Source Voltage	V_{DS}	12	V

TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITIONS	UNIT
1	Ambient Temperature	T_{amb}	+83(+0−5)	°C
2	Channel Temperature	T_{ch}	+175(+0−5)	°C
3	Drain Source Voltage	V_{DS}	8.0	V
4	Drain Current	I_D	450	mA

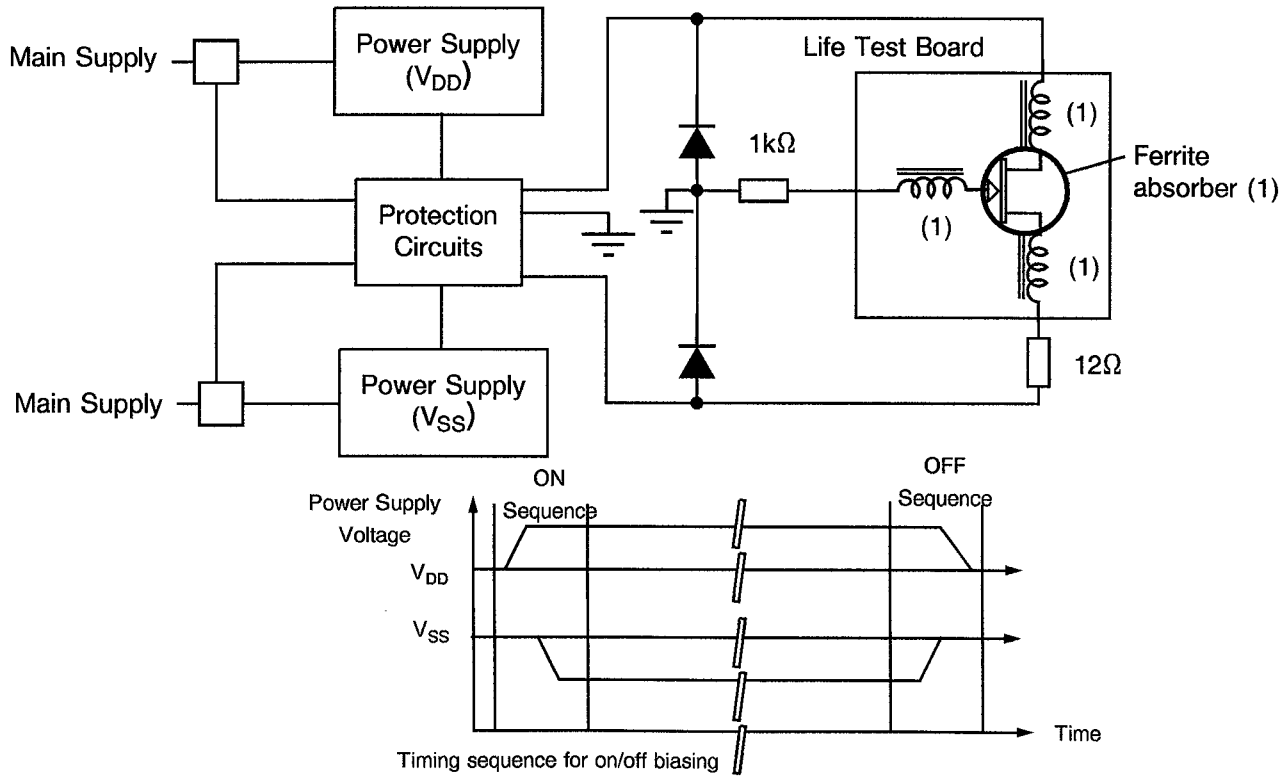
FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN



NOTES

1. Damping elements against self oscillation.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



NOTES

1. Damping elements against self oscillation.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION No. 5010)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 2. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests

The parameters to be measured at intermediate points and on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.3 Conditions for Operating Life Tests (Part of Endurance Testing)

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 5010. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.4 Electrical Circuits for Operating Life Tests

The circuit for use in performing the operating life test shall be the same as shown in Figure 5(b) for power burn-in.

4.9 TOTAL DOSE IRRADIATION TESTING

Not applicable.

4.10 SPECIAL TESTING

Not applicable.

TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	LIMITS		UNIT
						MIN.	MAX.	
1	Drain Saturation Current	I_{DSS}	As per Table 2	As per Table 2	±150	-	-	mA
2	Gate Threshold Voltage	$-V_{Gth}$	As per Table 2	As per Table 2	±300	-	-	mV
3	Drain Current at Pinch-off	I_{Dp}	As per Table 2	As per Table 2	±30	-	-	µA
4	Gate Leakage Current at Pinch-off	$-I_{Gp}$	As per Table 2	As per Table 2	±15	-	-	µA
5	Transconductance	gm	As per Table 2	As per Table 2	±30	-	-	mS
7	Output Power	P_O	As per Table 2	As per Table 2	±0.7	-	-	dBm

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING

Not applicable.

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTIN(

Not applicable.

APPENDIX 'A'

AGREED DEVIATIONS FOR SIEMENS (D)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.2	Para. 9.4, High Temperature Stabilisation Bake: May be performed at +175▮(+0▮-3) °C.
Para. 4.2.3	Para. 9.12, Radiographic Inspection: May be replaced by a Visual Inspection for verifying the length, height and shape of the wire bonding.