european space agency
agence spatiale européenne

Pages 1 to 32

INTEGRATED CIRCUITS, SILICON MONOLITHIC,

OPERATIONAL AMPLIFIERS,

BASED ON TYPE HA 2520-2

ESA/SCC Detail Specification No. 9101/010

space components
coordination group

Issue/Rev.	Date	Approved by	
		SCCG Chairman	ESA Director General or his Deputy
Issue 1	September 1981	-	-
Revision 'A'	December 1991		

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference / Item	Approved DCR No.
		This issue incorporates all modifications agreed on the basis of Policy DCR 21016 for adaption to new qualification requirements and Policy DCR 21019 (Appendices to Detail Specifications)	
'A'	Dec. '91	P1. Cover page P2. DCN P13. Para. 4.2.2 : PIND deviation deleted	None None 21048
		This specification has been transferred from hardcopy to electronic format. The content is unchanged but minor differences in presentation exist.	

TABLE OF CONTENTS

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, operational amplifier, based on Type HA 2520-2. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the integrated circuits specified herein are shown in Figure 2.

1.6 PIN ASSIGNMENT

As per Figures 3(a) and 3(b).

1.7 TRUTH TABLE

Not applicable.

1.8 CIRCUIT SCHEMATIC

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

TABLE 1(a) - TYPE VARIANTS

DASH No.	CASE	FIGURE	LEAD FINISH
01	FLAT	2(a)	Gold-plated
02	FLAT	2(a)	Solder-dipped/tin-plated
03	TO	2(b)	Gold-plated
04	TO	2(b)	Solder-dipped/tin-plated

TABLE 1(b) - MAXIMUM RATINGS

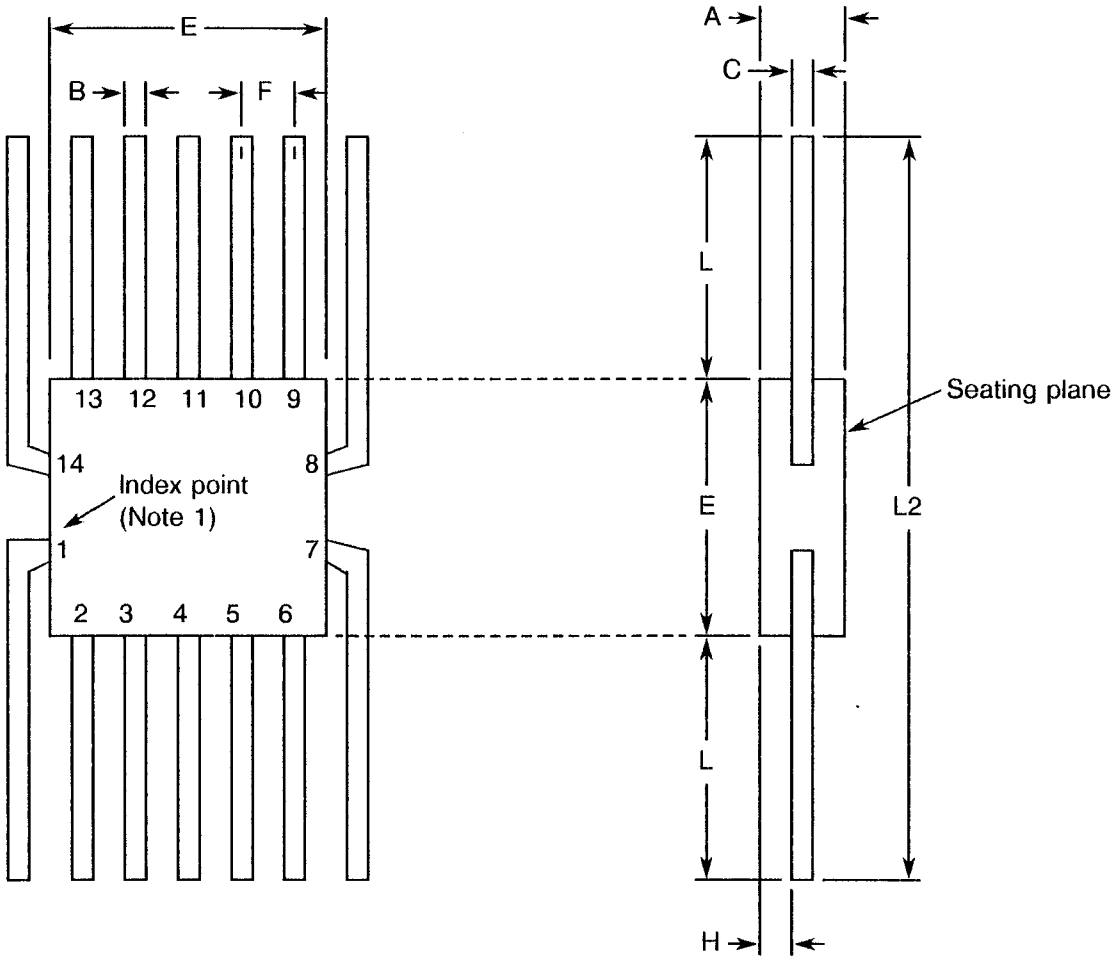
No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNITS	REMARKS
1	Supply Voltage	V_{CC}	40	V	Note 1
2	Differential Input Voltage	V_{IN}	± 15	V	
3	Peak Output Current	I_P	50	mA	
4	Device Dissipation	P_D	300	mWdc	
5	Operating Temperature	T_{op}	− 55 to + 125	°C	
6	Storage Temperature	T_{stg}	− 65 to + 150	°C	
7	Soldering Temperature	T_{sol}	+ 300	°C	Note 2

NOTES

1. Voltage between positive and negative supply.
2. Duration: 10 seconds maximum at a distance of not less than 1.5mm from the can, and the same lead shall not be resoldered until 3 minutes have elapsed.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE TO-86

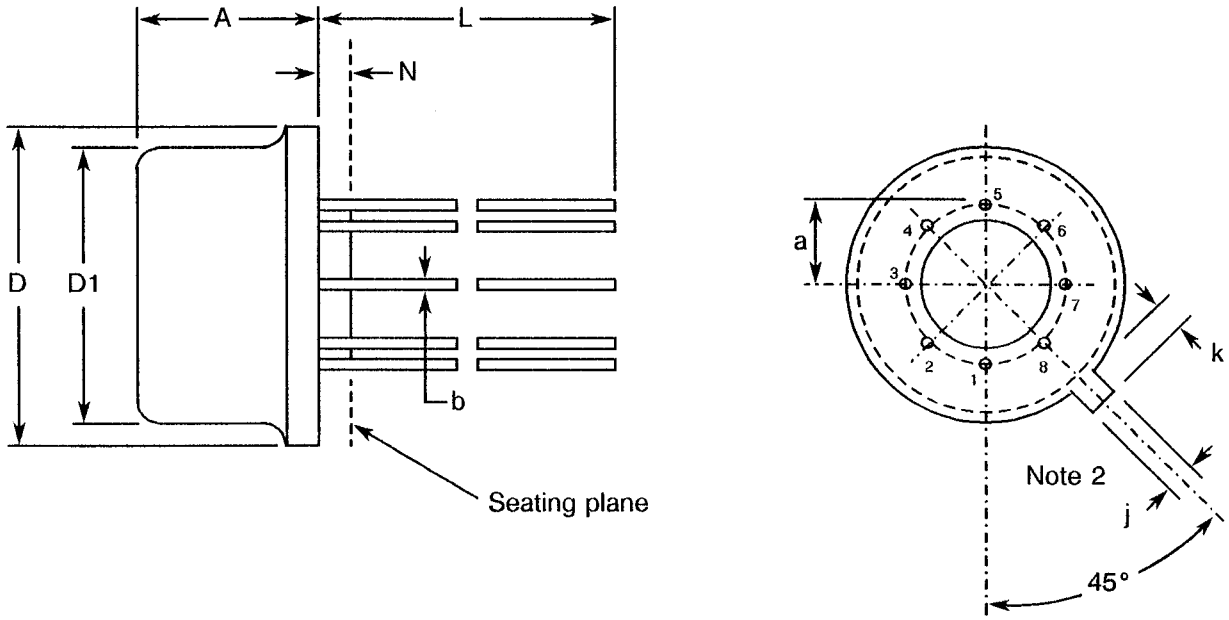


SYMBOL	INCHES		MILLIMETRES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	-	0.070	-	1.78	
B	0.014	0.018	0.36	0.46	4
C	0.004	0.006	0.10	0.16	
E	-	0.25	-	6.35	
F	0.50 TYP.		1.27 TYP.		
L	0.25	-	6.35	-	
L2	0.75	-	19.05	-	
Q	-	0.015	-	0.38	3

NOTES: See Page 9.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - TO99 PACKAGE



SYMBOL	INCHES		MILLIMETRES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	-	0.17	-	4.32	
a	0.1 TYP.		2.52 TYP.		
b	0.015	0.019	0.38	0.48	4
D	-	0.36	-	9.14	
D1	-	0.326	-	8.28	
j	0.28	0.38	7.11	9.65	
k	-	0.035	-	0.89	
N	-	0.025	-	0.64	
L	0.50	-	12.70	-	

NOTES: See Page 9.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES

1. Index point shall be identified by the enlargement of Pin 1 lead at the point of exit from the package.
2. Index point shall be identified by a tab which shall correspond to Pin 8.
3. Dimension Q shall be measured at the point of exit of the lead from the body.
4. Applies to all leads.

FIGURE 3(a) - PIN ASSIGNMENT

(FLAT PACKAGE TO-86)

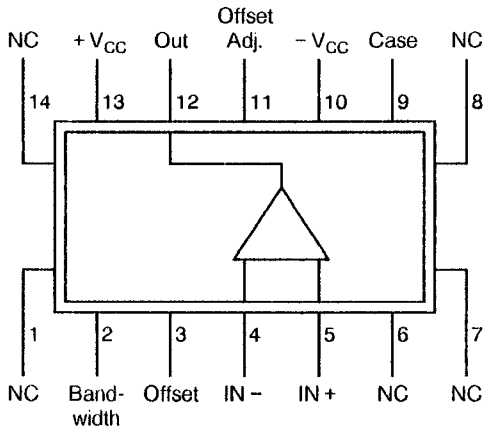
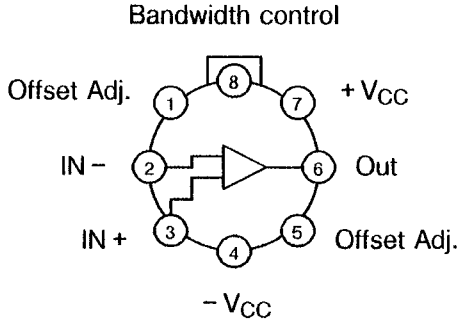


FIGURE 3(b) - PIN ASSIGNMENT

(TO CAN TO-99)



TOP VIEW

FIGURE 3(c) - CIRCUIT SCHEMATIC

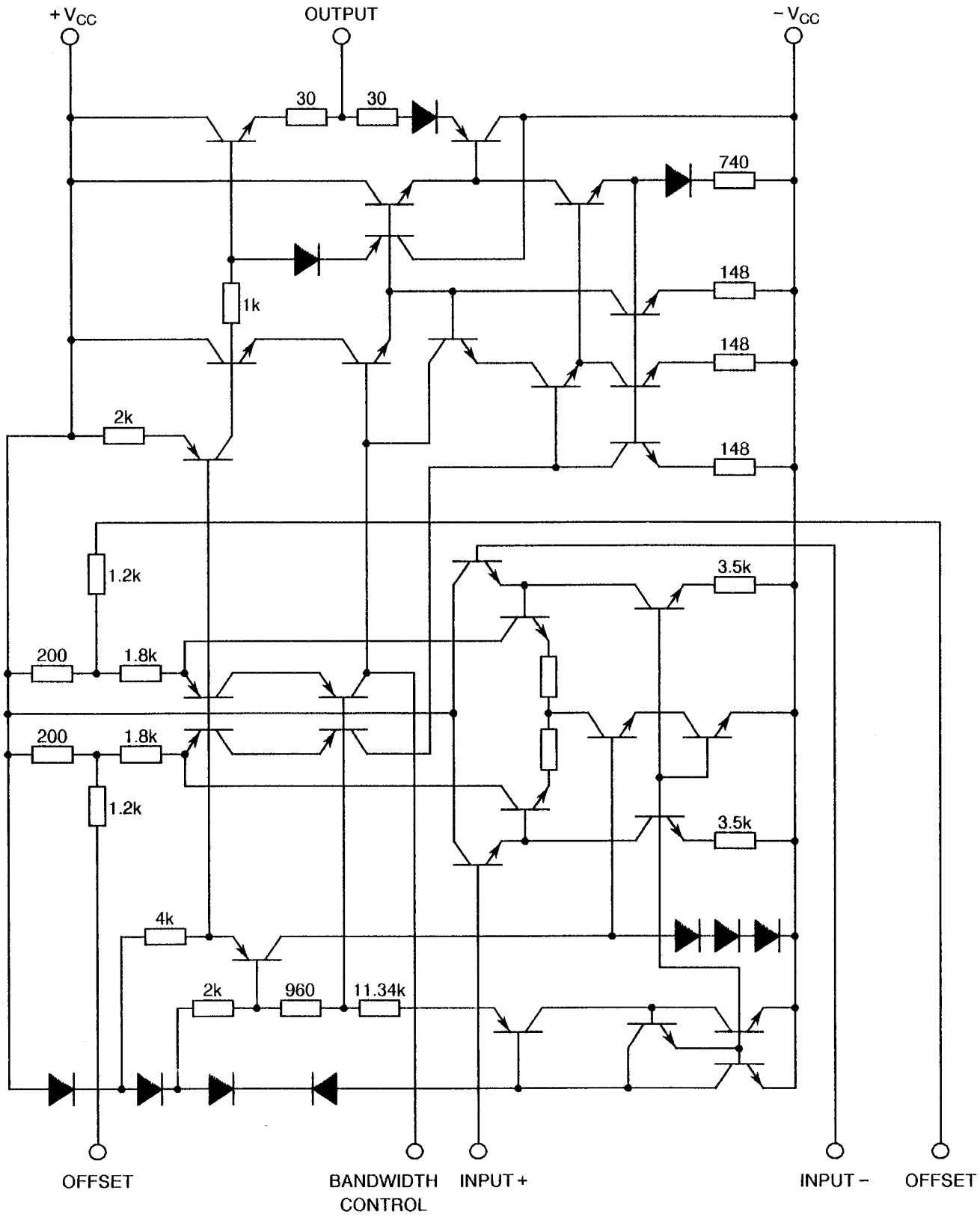
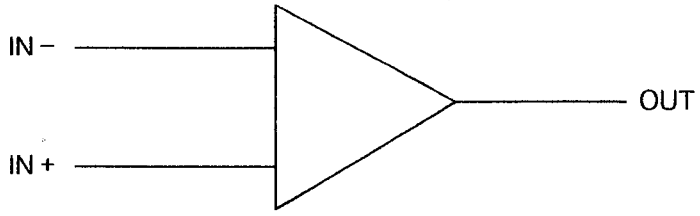


FIGURE 3(d) - FUNCTIONAL DIAGRAM



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

(c) MIL-STD-1276, Leads, Weldable, for Electronic Component Parts.

(d) MIL-M-38510, Microcircuits, General Specification for.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

I_{CC} = Supply Current.
V_{CC} = Supply Voltage.
$V_{IO(ADJ)}$ = Input Offset Adjust Voltage.
V_{OUT} = Output Voltage.
O_S = Overshoot.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

(a) The following test shall be added to the chart after "Bond Strength Test" (Para. 9.2.1):-

"Die-shear Test: In accordance with Method 2019 of MIL-STD-883. The sample size shall be 3 devices with no failures permitted".

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

Subpara. 7.1.1(a), "High Temperature Reverse Bias": Not applicable.

4.2.4 Deviations from Qualification, Environmental and Endurance Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 0.25 grammes for the flat package and 1.0 gram for the TO package.

4.4 MATERIALS

The materials shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body, and the lids shall be welded, brazed, preform-soldered or glass frit-sealed.

4.4.2 Lead Material and Finish

KOVAR in accordance with Type 'K' of MIL-STD-1276, gold-plated or solder-dipped/tin-plated. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

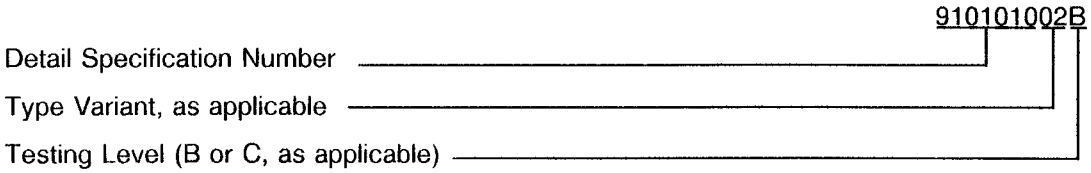
(c) Traceability Information.

4.5.2 Lead Identification

An index shall be located as specified in in Note 1 or 2 of Figure 2 for the flat package and the TO can respectively. The pin numbering shall be in accordance with Figure 2.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL CHARACTERISTICS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$°C and $-55(+5-0)$°C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits and functional test sequence for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for Burn-in

The requirements for burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for burn-in shall be as specified in Table 5 of this specification.

4.7.3 Electrical Circuits for Burn-in

Circuits for use in performing the burn-in tests are shown in Figure 5 of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions	Limits		Unit
							Min	Max	
1	Input Offset Voltage	V_{IO1}	4001	4(a)	E_1 (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{IN} = 0V	-	8.0	mV
2	Input Offset Voltage	V_{IO2}	4001	4(a)	E_2 (V)	$+V_{CC}$ = +25V, $-V_{CC}$ = −5.0V V_{IN} = 10V	-	8.0	mV
3	Input Offset Voltage	V_{IO3}	4001	4(a)	E_3 (V)	$+V_{CC}$ = +5.0V, $-V_{CC}$ = −25V V_{IN} = −10V	-	8.0	mV
4	Input Offset Current	I_{IO1}	4001	4(b)	E_4 (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{IN} = 0V, R_S = 10kΩ	-	25	nA
5	Input Offset Current	I_{IO2}	4001	4(b)	E_5 (V)	$+V_{CC}$ = +25V, $-V_{CC}$ = −5.0V V_{IN} = 10V, R_S = 10kΩ	-	25	nA
6	Input Offset Current	I_{IO3}	4001	4(b)	E_6 (V)	$+V_{CC}$ = +5.0V, $-V_{CC}$ = −25V V_{IN} = −10V, R_S = 10kΩ	-	25	nA
7	Input (Plus) Bias Current	I_{IB1}	4001	4(c)	E_7 (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{IN} = 0V, R_S = 10kΩ	-	200	nA
8	Input (Plus) Bias Current	I_{IB2}	4001	4(c)	E_8 (V)	$+V_{CC}$ = +25V, $-V_{CC}$ = −5.0V V_{IN} = 10V, R_S = 10kΩ	-	200	nA
9	Input (Plus) Bias Current	I_{IB3}	4001	4(c)	E_9 (V)	$+V_{CC}$ = +5.0V, $-V_{CC}$ = −25V V_{IN} = −10V, R_S = 10kΩ	-	200	nA
10	Input (Minus) Bias Current	I_{-IB1}	4001	4(d)	E_{10} (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{IN} = 0V, R_S = 10kΩ	-	200	nA
11	Input (Minus) Bias Current	I_{-IB2}	4001	4(d)	E_{11} (V)	$+V_{CC}$ = +25V, $-V_{CC}$ = −5.0V V_{IN} = 10V, R_S = 10kΩ	-	200	nA
12	Input (Minus) Bias Current	I_{-IB3}	4001	4(d)	E_{12} (V)	$+V_{CC}$ = +5.0V, $-V_{CC}$ = −25V V_{IN} = −10V, R_S = 10kΩ	-	200	nA
13	Power Supply Current	I_{CC}	4005	4(a)	I_{CC}	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{IN} = 0V	-	6.0	mA
14	Input Offset Adjust Voltage (Plus)	$V_{IO(Adj)+}$	-	4(e)	E_{13} (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{IN} = Open $V_{IO(Adj)}$ = 15V	9.0	-	mV
15	Input Offset Adjust Voltage (Minus)	$V_{IO(Adj)-}$	-	4(e)	E_{14} (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{IN} = Open $V_{IO(Adj)}$ = 15V	-	−9.0	mV
16	Output Voltage Positive	$+V_{OUT}$	-	4(f)	E_{15} (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V I_{load} = 10mA V_{IN} = 0.5V	10	-	V
17	Output Voltage Negative	$-V_{OUT}$	-	4(f)	E_{16} (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V I_{load} = 10mA V_{IN} = −0.5V	-	−10	V

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions	Limits		Unit
							Min	Max	
18	Power Supply Rejection Ratio (Plus)	+PSRR	4003	4(a)	E_{17} (V)	$+V_{CC} = +10V$, $-V_{CC} = -15V$ $V_{IN} = 0V$	80	-	dB
					E_{18} (V)	$+V_{CC} = +20V$, $-V_{CC} = -15V$ $V_{IN} = 0V$			
19	Power Supply Rejection Ratio (Minus)	-PSRR	4003	4(a)	E_{19} (V)	$+V_{CC} = +15V$, $-V_{CC} = -10V$ $V_{IN} = 0V$	80	-	dB
					E_{20} (V)	$+V_{CC} = +15V$, $-V_{CC} = -20V$ $V_{IN} = 0V$			
20	Common Mode Rejection Ratio	CMRR	4003	4(a)	E_{21} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -25V$ $V_{IN} = -10V$	80	-	dB
					E_{22} (V)	$+V_{CC} = +25V$, $-V_{CC} = -5.0V$ $V_{IN} = 10V$			
21	Output Voltage Swing (Plus)	V_{OPP}	4004	4(g)	E_{23} (V)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{IN} = 0.5V$, $R_L = 2.0k\Omega$	10	-	V
22	Output Voltage Swing (Minus)	V_{OPP}	4004	4(g)	E_{24} (V)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{IN} = -0.5V$, $R_L = 2.0k\Omega$	-	-10	V
23	Open Loop Voltage Gain (Plus)	$+A_{VS}$	4004	4(h)	E_{25} (V)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{IN} = 0V$, $R_L = 2.0k\Omega$	10	-	V/mV
					E_{26} (V)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{IN} = 10V$, $R_L = 2.0k\Omega$			
24	Open Loop Voltage Gain (Minus)	$-A_{VS}$	4004	4(h)	E_{27} (V)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{IN} = 0V$, $R_L = 2.0k\Omega$	10	-	V/mV
					E_{28} (V)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{IN} = -10V$, $R_L = 2.0k\Omega$			

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Test Conditions	Limits		Unit
						Min	Max	
25	Slew Rate (Plus)	SR(+)	4002	4(i)	$V_{CC} = \pm 15V$ $V_{IN} = -1.67V$ to $1.67V$ square $R_L = 2.0k\Omega$, $C_L = 50pF$	100	-	V/µs
26	Slew Rate (Minus)	SR(−)	4002	4(i)	$V_{CC} = \pm 15V$ $V_{IN} = 1.67V$ to $-1.67V$ square $R_L = 2.0k\Omega$, $C_L = 50pF$	100	-	V/µs
27	Transient Response Rise and Fall Times	t_r	4002	4(i)	$V_{CC} = \pm 15V$ $V_{IN} = 0V$ to $66.7mV$ square $R_L = 2.0k\Omega$, $C_L = 50pF$	-	50	ns
28		t_f		4(i)	$V_{CC} = \pm 15V$ $V_{IN} = 0V$ to $-66.7mV$ square $R_L = 2.0k\Omega$, $C_L = 50pF$	-	50	
29	Overshoot (Plus)	+OS	4002	4(i)	$V_{CC} = \pm 15V$ $V_{IN} = 0V$ to $-66.7mV$ square $R_L = 2.0k\Omega$, $C_L = 50pF$	-	40	%
30	Overshoot (Minus)	−OS	4002	4(i)	$V_{CC} = \pm 15V$ $V_{IN} = 0V$ to $66.7mV$ square $R_L = 2.0k\Omega$, $C_L = 50pF$	-	40	%
31	Setting Time	t_s	4002	4(i)	$V_{CC} = \pm 15V$ $V_{IN} = 1.67V$ to $-1.67V$ square $R_L = 2.0k\Omega$, $C_L = 50pF$ Note 1	-	−1.5	µs
32	Bandwidth	B	4004	-	$V_{CC} = \pm 15V$ $V_{OUT} = \pm 10V$ Note 1	1500	-	kHz

NOTES:
1. Guaranteed but not tested.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, +125(+0-5) AND -55(+5-0) °C

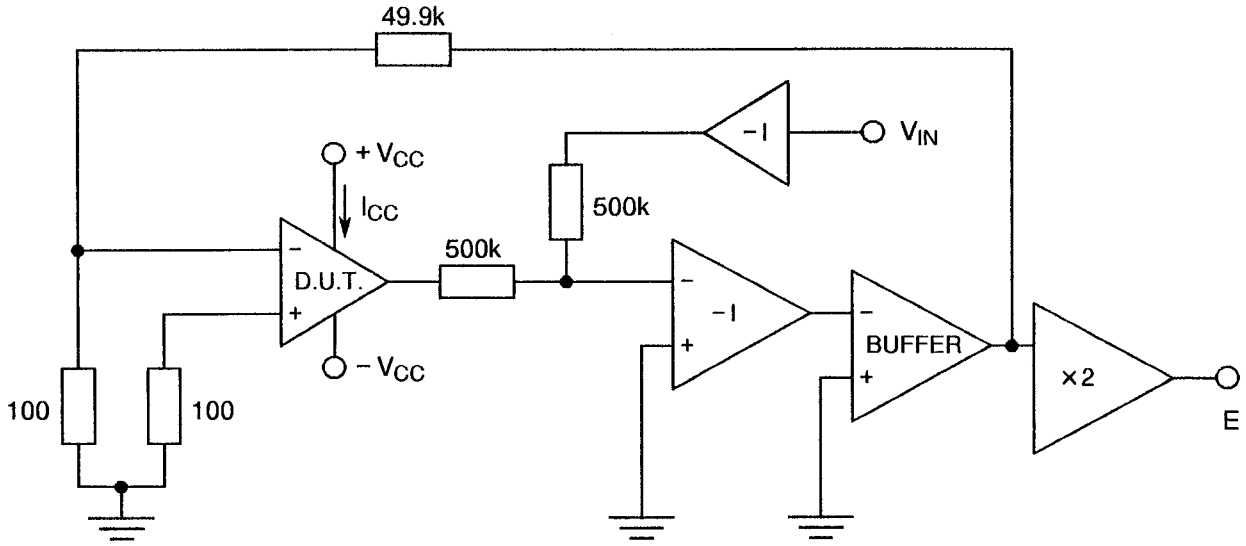
No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions	Limits		Unit
							Min	Max	
1	Input Offset Voltage	V_{IO1}	4001	4(a)	E_1 (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = -15V V_{IN} = 0V	-	11	mV
2	Input Offset Voltage	V_{IO2}	4001	4(a)	E_2 (V)	$+V_{CC}$ = +25V, $-V_{CC}$ = -5.0V V_{IN} = 10V	-	11	mV
3	Input Offset Voltage	V_{IO3}	4001	4(a)	E_3 (V)	$+V_{CC}$ = +5.0V, $-V_{CC}$ = -25V V_{IN} = -10V	-	11	mV
4	Input Offset Current	I_{IO1}	4001	4(b)	E_4 (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = -15V V_{IN} = 0V, R_S = 10kΩ	-	50	nA
5	Input Offset Current	I_{IO2}	4001	4(b)	E_5 (V)	$+V_{CC}$ = +25V, $-V_{CC}$ = -5.0V V_{IN} = 10V, R_S = 10kΩ	-	50	nA
6	Input Offset Current	I_{IO3}	4001	4(b)	E_6 (V)	$+V_{CC}$ = +5.0V, $-V_{CC}$ = -25V V_{IN} = -10V, R_S = 10kΩ	-	50	nA
7	Input (Plus) Bias Current	I_{IB1}	4001	4(c)	E_7 (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = -15V V_{IN} = 0V, R_S = 10kΩ	-	400	nA
8	Input (Plus) Bias Current	I_{IB2}	4001	4(c)	E_8 (V)	$+V_{CC}$ = +25V, $-V_{CC}$ = -5.0V V_{IN} = 10V, R_S = 10kΩ	-	400	nA
9	Input (Plus) Bias Current	I_{IB3}	4001	4(c)	E_9 (V)	$+V_{CC}$ = +5.0V, $-V_{CC}$ = -25V V_{IN} = -10V, R_S = 10kΩ	-	400	nA
10	Input (Minus) Bias Current	I_{-IB1}	4001	4(d)	E_{10} (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = -15V V_{IN} = 0V, R_S = 10kΩ	-	400	nA
11	Input (Minus) Bias Current	I_{-IB2}	4001	4(d)	E_{11} (V)	$+V_{CC}$ = +25V, $-V_{CC}$ = -5.0V V_{IN} = 10V, R_S = 10kΩ	-	400	nA
12	Input (Minus) Bias Current	I_{-IB3}	4001	4(d)	E_{12} (V)	$+V_{CC}$ = +5.0V, $-V_{CC}$ = -25V V_{IN} = -10V, R_S = 10kΩ	-	400	nA
13	Power Supply Current	I_{CC}	4005	4(a)	I_{CC}	$+V_{CC}$ = +15V, $-V_{CC}$ = -15V V_{IN} = 0V	-	6.5	mA
14	Input Offset Adjust Voltage (Plus)	$V_{IO(Adj)+}$	-	4(e)	E_{13} (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = -15V V_{IN} = Open $V_{IO(Adj)}$ = 15V	11	-	mV
15	Input Offset Adjust Voltage (Minus)	$V_{IO(Adj)-}$	-	4(e)	E_{14} (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = -15V V_{IN} = Open $V_{IO(Adj)}$ = 15V	-	-11	mV
16	Output Voltage Positive	$+V_{OUT}$	-	4(f)	E_{15} (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = -15V I_{load} = 5.0mA V_{IN} = 0.5V	10	-	V
17	Output Voltage Negative	$-V_{OUT}$	-	4(f)	E_{16} (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = -15V I_{load} = 5.0mA V_{IN} = -0.5V	-	-10	V

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, +125(+0-5) AND -55(+5-0) °C (CONT'D)

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions	Limits		Unit
							Min	Max	
18	Power Supply Rejection Ratio (Plus)	+PSRR	4003	4(a)	E_{17} (V)	$+V_{CC}$ = +10V, $-V_{CC}$ = -15V V_{IN} = 0V	80	-	dB
					E_{18} (V)	$+V_{CC}$ = +20V, $-V_{CC}$ = -15V V_{IN} = 0V			
19	Power Supply Rejection Ratio (Minus)	-PSRR	4003	4(a)	E_{19} (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = -10V V_{IN} = 0V	80	-	dB
					E_{20} (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = -20V V_{IN} = 0V			
20	Common Mode Rejection Ratio	CMRR	4003	4(a)	E_{21} (V)	$+V_{CC}$ = +5.0V, $-V_{CC}$ = -25V V_{IN} = -10V	80	-	dB
					E_{22} (V)	$+V_{CC}$ = +25V, $-V_{CC}$ = -5.0V V_{IN} = 10V			
21	Output Voltage Swing (Plus)	V_{OPP}	4004	4(g)	E_{23} (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = -15V V_{IN} = 0.5V, R_L = 2.0kΩ	10	-	V
22	Output Voltage Swing (Minus)	V_{OPP}	4004	4(g)	E_{24} (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = -15V V_{IN} = -0.5V, R_L = 2.0kΩ	-	-10	V
23	Open Loop Voltage Gain (Plus)	$+A_{VS}$	4004	4(h)	E_{25} (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = -15V V_{IN} = 0V, R_L = 2.0kΩ	7.5	-	V/mV
					E_{26} (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = -15V V_{IN} = 10V, R_L = 2.0kΩ			
24	Open Loop Voltage Gain (Minus)	$-A_{VS}$	4004	4(h)	E_{27} (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = -15V V_{IN} = 0V, R_L = 2.0kΩ	7.5	-	V/mV
					E_{28} (V)	$+V_{CC}$ = +15V, $-V_{CC}$ = -15V V_{IN} = -10V, R_L = 2.0kΩ			

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - INPUT OFFSET VOLTAGE, SUPPLY CURRENT, POWER SUPPLY REJECTION RATIO AND COMMON MODE REJECTION RATIO



Input Offset Voltage

$V_{IO1} = E_1$, $V_{IO2} = E_2$, $V_{IO3} = E_3$.

Power Supply Rejection Ratio

$$+PSRR = 20 \log_{10} \frac{10^4}{E_{17} - E_{18}}$$

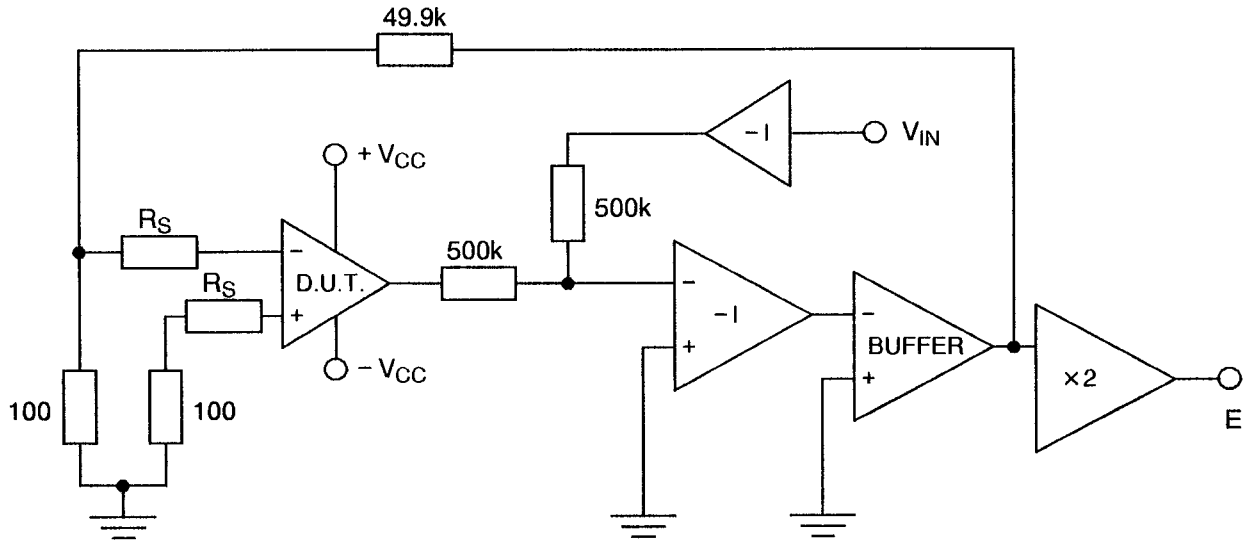
$$-PSRR = 20 \log_{10} \frac{10^4}{E_{19} - E_{20}}$$

Common Mode Rejection Ratio

$$CMRR = 20 \log_{10} \frac{2 \times 10^4}{E_{21} - E_{22}}$$

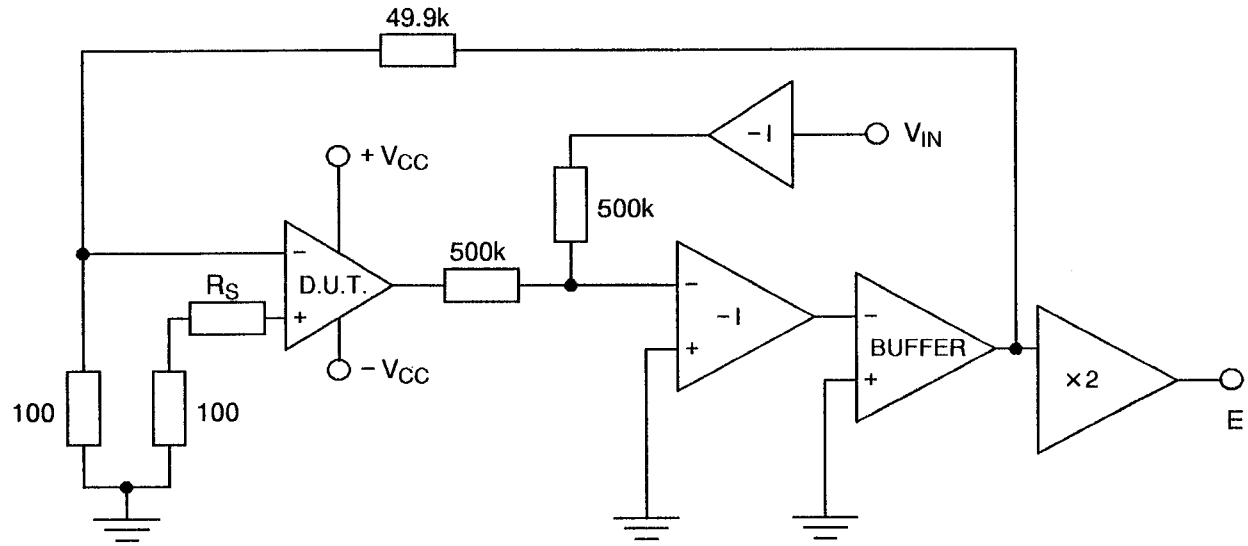
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(b) - INPUT OFFSET CURRENT



$I_{IO1} = (E_1 - E_4) \times 100$
$I_{IO2} = (E_2 - E_5) \times 100$
$I_{IO3} = (E_3 - E_6) \times 100$

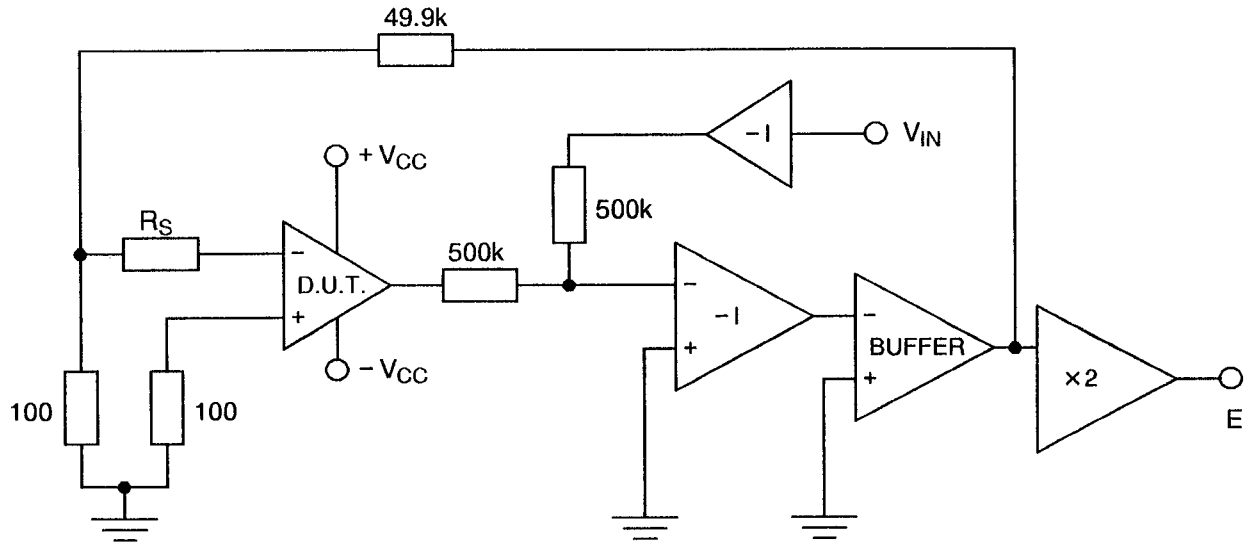
FIGURE 4(c) - INPUT BIAS CURRENT



$I_{IB1} = (E_1 - E_7) \times 100$
$I_{IB2} = (E_2 - E_8) \times 100$
$I_{IB3} = (E_3 - E_9) \times 100$

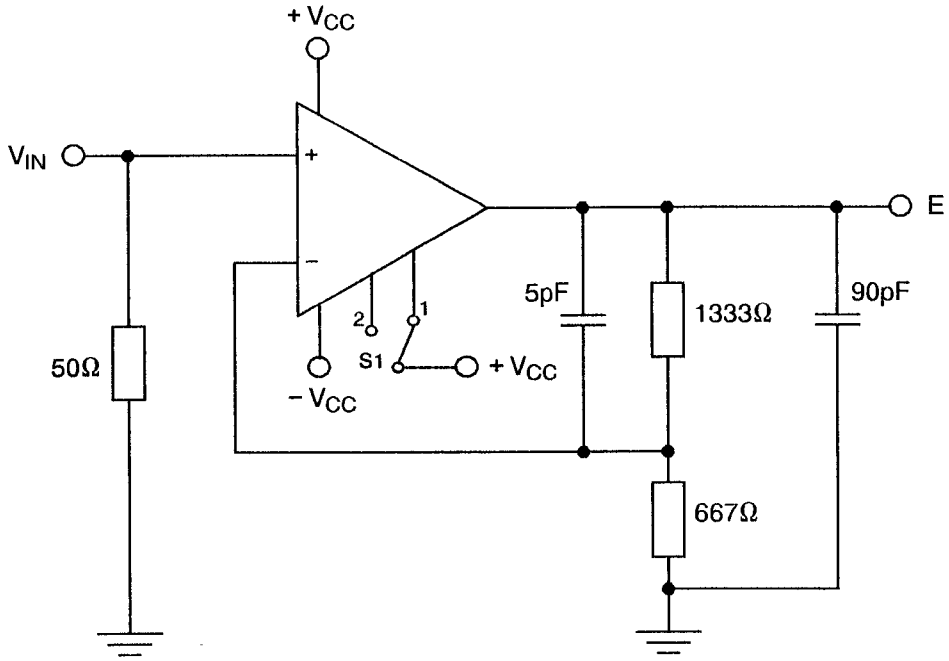
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(d) - INPUT (MINUS) BIAS CURRENT



$-I_{IB1} = (E_1 - E_{10}) \times 100$
$-I_{IB2} = (E_2 - E_{11}) \times 100$
$-I_{IB3} = (E_3 - E_{12}) \times 100$

FIGURE 4(e) - INPUT OFFSET ADJUST VOLTAGE



NOTES

1. $V_{IO(Adj)}$ is positive if $E_1 < 0$, and negative if $E_1 > 0$.
2. S1 to position 1 for $V_{IO(Adj)}$ positive and position 2 for $V_{IO(Adj)}$ negative.
   $+V_{IO(Adj)} = E_{13} - E_1$, $-V_{IO(Adj)} = E_{14} - E_1$.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(f) - OUTPUT VOLTAGE

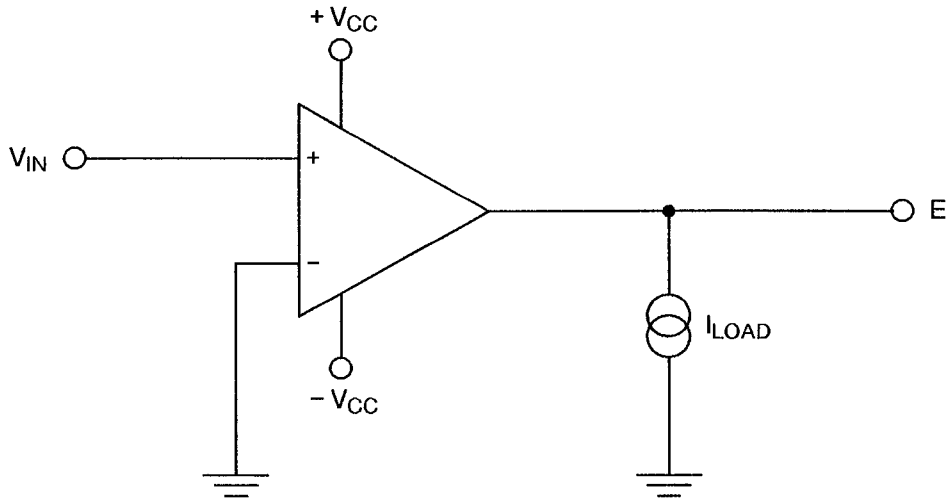


FIGURE 4(g) - OUTPUT VOLTAGE SWING

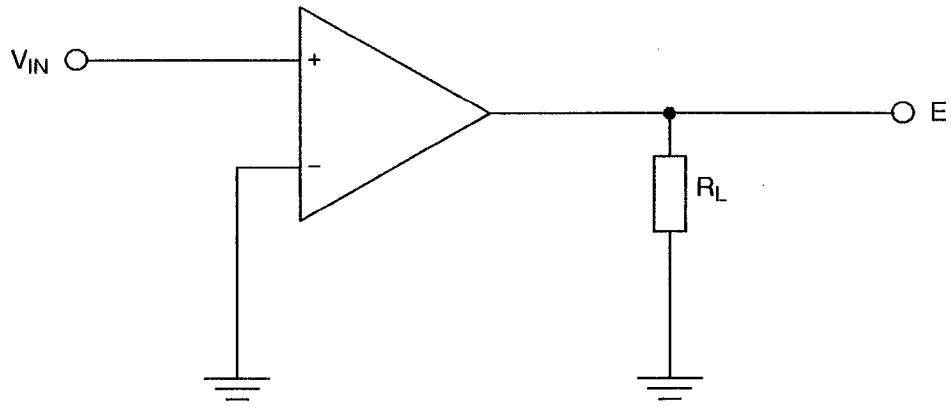
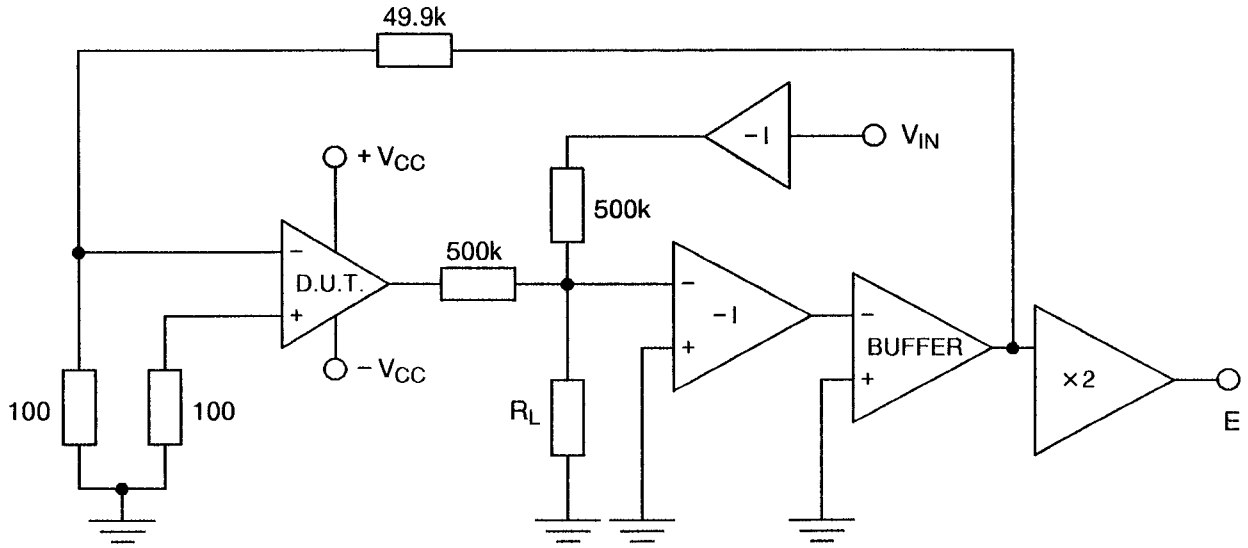


FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(h) - OPEN LOOP VOLTAGE GAIN

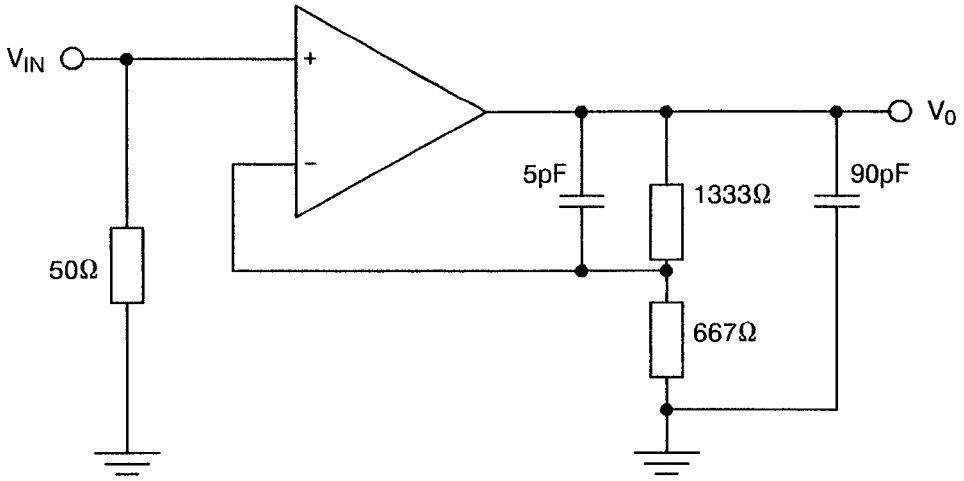


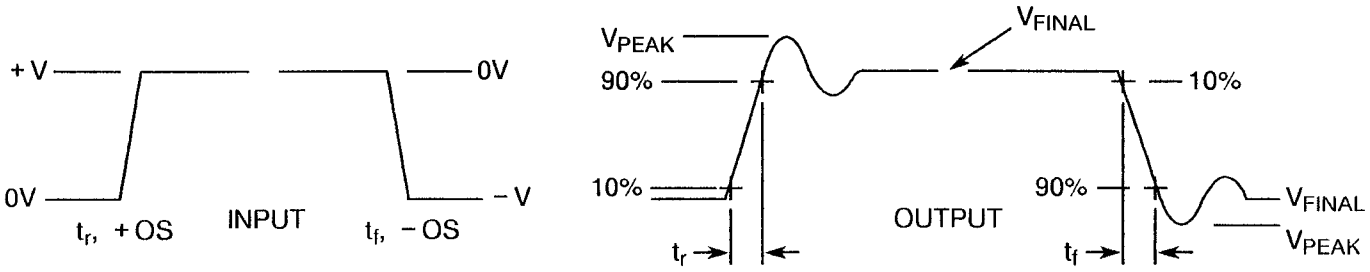
$$+A_{VS} = \frac{10}{E_{26} - E_{25}}$$

$$-A_{VS} = \frac{10}{E_{27} - E_{28}}$$

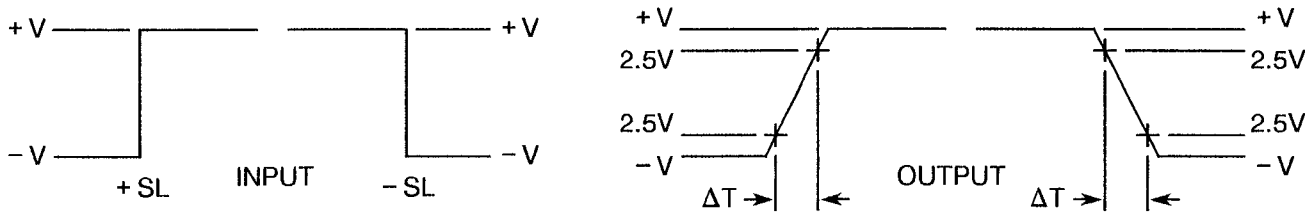
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - DYNAMIC TEST MEASUREMENT CIRCUIT





OVERSHOOT, RISE AND FALL TIME WAVEFORMS



SLEW RATE WAVEFORMS

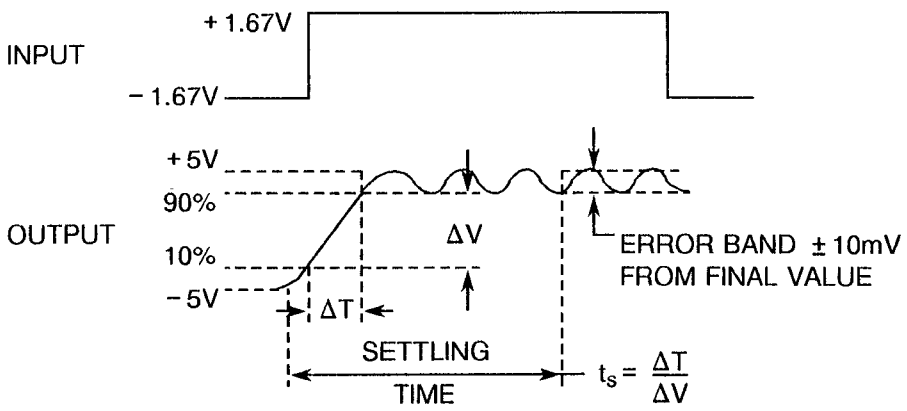


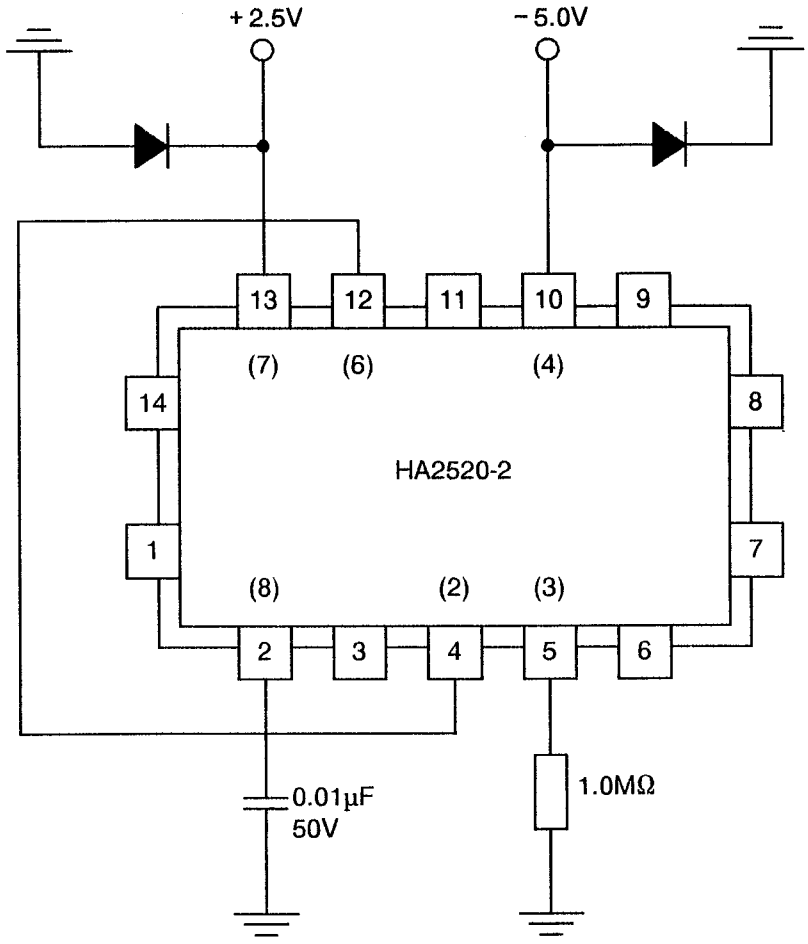
TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
1	Input Offset Voltage	V_{IO1}	As per Table 2	As per Table 2	±2.0	mV
7	Input (Plus) Bias Current	I_{IB1}	As per Table 2	As per Table 2	50	nA
10	Input (Minus) Bias Current	$-I_{B1}$	As per Table 2	As per Table 2	50	nA

TABLE 5 - CONDITIONS FOR BURN-IN AND OPERATING LIFE TEST

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0−5)	°C
2	Power Supply	V_S	+25, −5	V

FIGURE 5 - ELECTRICAL CIRCUIT FOR BURN-IN AND OPERATING LIFE TEST



NOTES

1. Pin numbers marked in parenthesis correspond to TO99 Can Pin Assignments.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 2. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5 of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The conditions for high temperature storage shall be $T_{amb} = +150(+0-5)$ °C.

TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
1	Input Offset Voltage	V_{IO1}	As per Table 2	As per Table 2	-	8.0	mV
4	Input Offset Current	I_{IO1}	As per Table 2	As per Table 2	-	25	nA
7	Input (Plus) Bias Current	I_{IB1}	As per Table 2	As per Table 2	-	200	nA
13	Power Supply Current	I_{CC}	As per Table 2	As per Table 2	-	6.0	mA
16	Output Voltage Positive	$+V_{OUT}$	As per Table 2	As per Table 2	10	-	V
17	Output Voltage Negative	$-V_{OUT}$	As per Table 2	As per Table 2	-	−10	V
23	Open Loop Voltage Gain (Plus)	$+A_{VS}$	As per Table 2	As per Table 2	10	-	V/mV

APPENDIX 'A'

AGREED DEVIATIONS FOR HARRIS (U.S.)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.1	Deviations from Special In-process Controls (Para. 5.1) (a) Para. 5.1.1, "Scanning Electron Microscope Inspection (SEM)" This shall be performed in accordance with Method 2018 of MIL-STD-883, with the following exceptions:- 1. A SEM lot is defined at the metallisation step. One wafer is selected from the inside row and one from the outside row of the same planet. Sampling condition B_2 (segment, prior to glassivation) is used regardless of the glassivation temperature. 2. All four directional edges of every type of oxide step shall be examined on each wafer. The manufacturer shall mount each of the wafer's four sample dice 90° out of phase from each other, so that all four edge directions can be properly inspected on each wafer. Questionable steps which are not at the proper viewing angle are inspected by rotating the sample as needed. 3. A lot is unacceptable if the directional edge of any contact window, or other type of oxide step, has a reduced cross-sectional area greater than 50%, or if it is reduced in thickness such that, at worst case specified operating conditions, the current density exceeds the limits specified in MIL-M-38510, Para. 3.5.5 (5×10^5 A/cm^2 for glassivated aluminium products). The current density is determined per Para. 3.5.5(a) of MIL-M-38510. Reduced cross-sectional area due to voids or defects that can be readily observed by Method 2010 of MIL-STD-883, "Visual Inspection of Metallisation", is no cause for SEM lot rejection. 4. A lot is unacceptable if the general metallisation (metallisation at all locations except at oxide steps) shows peeling or lifting as a result of poor adhesion. General metallisation is unacceptable if voiding or undercutting of the metal reduces the cross-sectional area by more than 50% or if it is reduced in thickness such that, at worst case specified operating conditions, the current density exceeds the limits specified in MIL-M-38510, Para. 3.5.5. Voids and defects in the general metallisation that can be readily observed by Method 2010 of MIL-STD-883, "Visual Inspection of Metallisation", is no cause for SEM lot rejection.