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INTEGRATED CIRCUITS, SILICON MONOLITHIC, LOW POWER, QUAD, BIPOLAR OPERATIONAL AMPLIFIERS, BASED ON TYPES LM124 AND LM124A

ESA/SCC Detail Specification No. 9101/011

space components
coordination group

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		SCCG Chairman	ESA Director General or his Deputy
Issue 2	March 1995		

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
		This Issue supersedes Issue 1 and incorporates all modifications defined in Revisions 'A', 'B', 'C' and 'D' to Issue 1 and the following DCR's:-		
		Cover Page		None
		DCN		None
		Table 1(a)	: Lead Material column heading amended	221145
			: Variants 11 and 12 added	221145
		Table 1(b)	: Nos. 3, 4 and 6, Symbol amended	221145
			: No. 6, Characteristics amended, Variants 11 and 12 added and Note 5 reference amended to "4"	221145
			: No. 7, "T_{amb}" added to Remarks	221145
			: No. 9, existing temperature referenced to FP and DIL, new temperature added for CCP and Note 6 reference amended to "7"	221145
			: Notes 2 and 4 amended	221145
			: Note 5, text deleted and new text added	221145
			: Note 6 renumbered "7" and new Note 6 added	221145
			: New Note 8 added	221145
		Figure 1	: Title amended and Undertitle added	221145
			: Existing slopes allocated to Variants and new slope added	221145
		Figures 2(a), 2(b)	: Title amended and Sub-title added	221145
			: Imperial dimensions deleted	221145
			: Notes moved and standardised	221145
		Figure 2(c)	: Added	221145
		Figure 2	: Notes consolidated onto 1 page	221145
		Figure 3(a)	: Title added to existing drawing	221145
			: New Title and drawing added	221145
			: Pin assignment added	221145
			: Note deleted	221145
		Para. 3	: Abbreviations for "V_{CC}" and "$I_{OS(t)}$" added and RT abbreviation amended	221145
		Para. 4.3.2	: Text amended	221145
		Para. 4.4.2	: Text amended	221145
		Para. 4.5.1	: Text deleted and new text added	23723
		Para. 4.5.2	: Text amended	221145
		Para. 4.5.5	: Deleted in toto	23723
		Para. 4.7.2	: Renumbered to "4.7.3" and text amended	221145
			: New Para. added	221145
		Para. 4.7.3	: Renumbered to "4.7.5" and text amended	221145
		Para. 4.7.4	: New Para. added	221145
		Table 2	: Nos. 130 to 133, Symbol amended	221145
			: Note 6 amended	221145
		Table 5(a)	: Entry added	221145
		Table 5	: Renumbered to "5(b)" and Title amended	221145
		Figure 5(a)	: Entry added	221145
		Figure 5	: Renumbered to "5(b)" and Title amended	221145
		Para. 4.8.2	: Second sentence added	221145
		Para's. 4.8.4 & 4.8.5	: In second sentence, 5 changed to "5(b)"	221145
		Para. 4.8.6	: Second sentence amended	23723
		Table 6	: Note amended	221145

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TABLES

FIGURES

APPENDICES (Applicable to specific Manufacturers only)

None.

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, Low Power, Quad, Bipolar Operational Amplifier, based on Types LM124 and LM124A. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The parameter derating information of the integrated circuits specified herein is shown in Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the integrated circuits specified herein are shown in Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE (FIGURE 3(b))

Not applicable.

1.8 CIRCUIT SCHEMATIC

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

TABLE 1(a) - TYPE VARIANTS

VARIANT	BASED ON TYPE	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	LM124	FLAT	2(a)	D2
02	LM124	FLAT	2(a)	D3 or D4
03	LM124	D.I.L.	2(b)	D2
04	LM124	D.I.L.	2(b)	D3 or D4
05	LM124A	FLAT	2(a)	D2
06	LM124A	FLAT	2(a)	D3 or D4
07	LM124A	D.I.L.	2(b)	D2
08	LM124A	D.I.L.	2(b)	D3 or D4
09	LM124	D.I.L.	2(b)	G4
10	LM124A	D.I.L.	2(b)	G4
11	LM124	CHIP CARRIER	2(c)	2
12	LM124A	CHIP CARRIER	2(c)	2

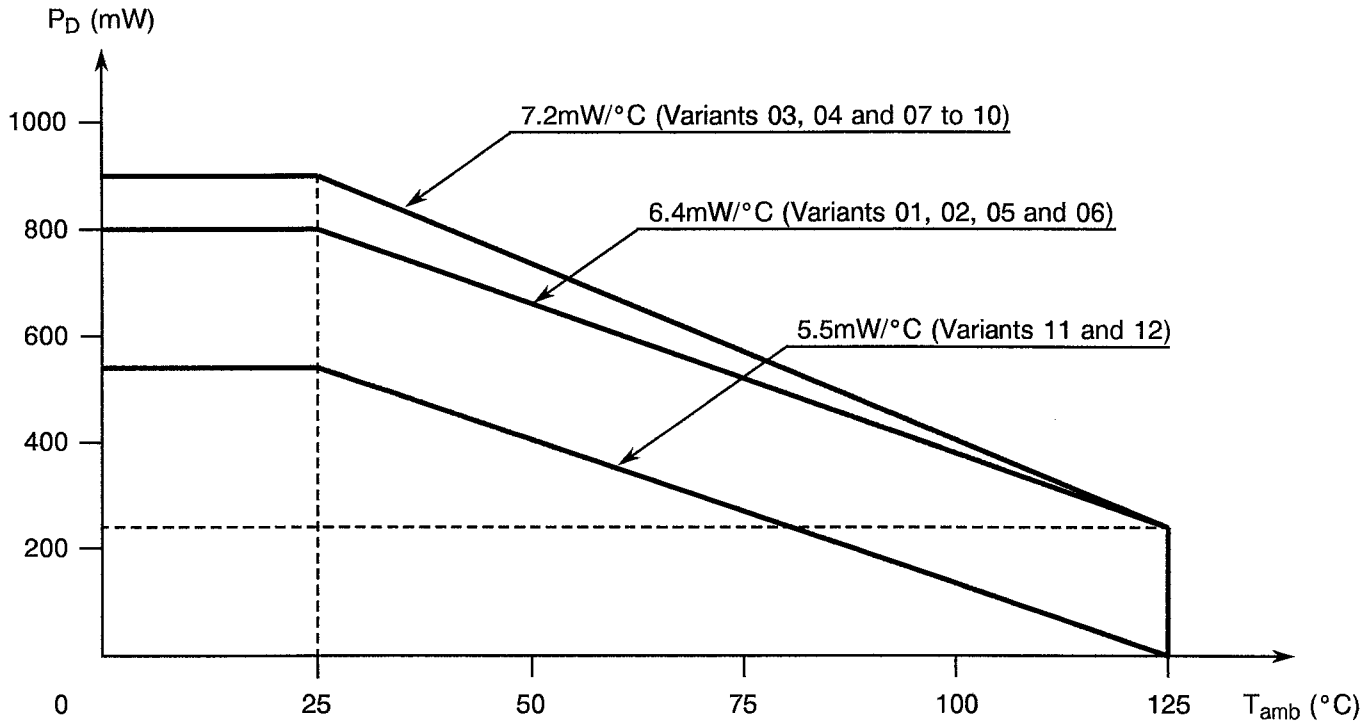
TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage Range	V_{CC}	±32 or ±16	V	-
2	Differential Input Voltage Range	V_{ID}	±32	V	-
3	Input Voltage	V_{IN}	−0.3 to +32	V	Note 1
4	Input Current	I_{IN}	50	mA	Note 2
5	Output Short Circuit Duration	$I_{OS(t)}$	Indefinite		Note 3
6	Power Dissipation Variants 01, 02, 05, 06 Variants 03, 04, 07, 08, 09, 10 Variants 11, 12 Variants 11, 12	P_D	 800 900 550 300	mW	 Note 4 Note 4 Note 5 Note 6
7	Operating Temperature Range	T_{op}	−55 to +125	°C	T_{amb}
8	Storage Temperature Range	T_{stg}	−65 to +150	°C	-
9	Soldering Temperature For FP and DIP For CCP	T_{sol}	 +300 +245	°C	 Note 7 Note 8
10	Junction Temperature	T_J	+150	°C	-

NOTES

1. For supply voltages less than +32V, the absolute maximum input voltage is equal to supply voltage.
2. $V_{IN} < -0.3\ V_{OL}$.
3. Short circuits from the output to $+V_{CC}$ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA, independent of the magnitude of $+V_{CC}$. At $+V_{CC} > +15V$, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.
4. At $T_{amb} = +25°C$. For derating at $T_{amb} > +25°C$, see Figure 1.
5. At $T_{amb} = +25°C$ when mounted on a ceramic substrate of dimensions 15×15×0.6mm. For derating at $T_{amb} > +25°C$, see Figure 1.
6. At $T_{amb} = +25°C$ without substrate.
7. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
8. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

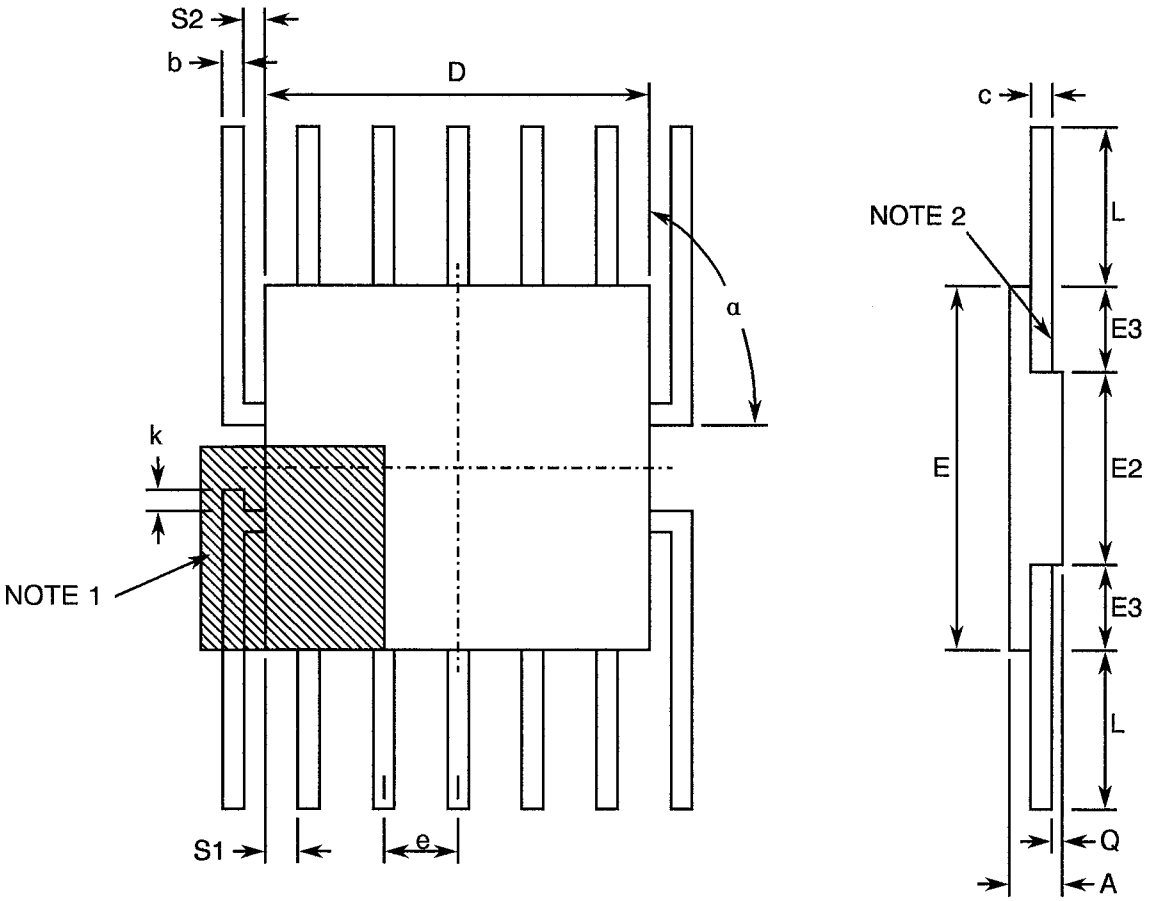
FIGURE 1 - PARAMETER DERATING INFORMATION



Power Dissipation versus Temperature

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE, 14-PIN

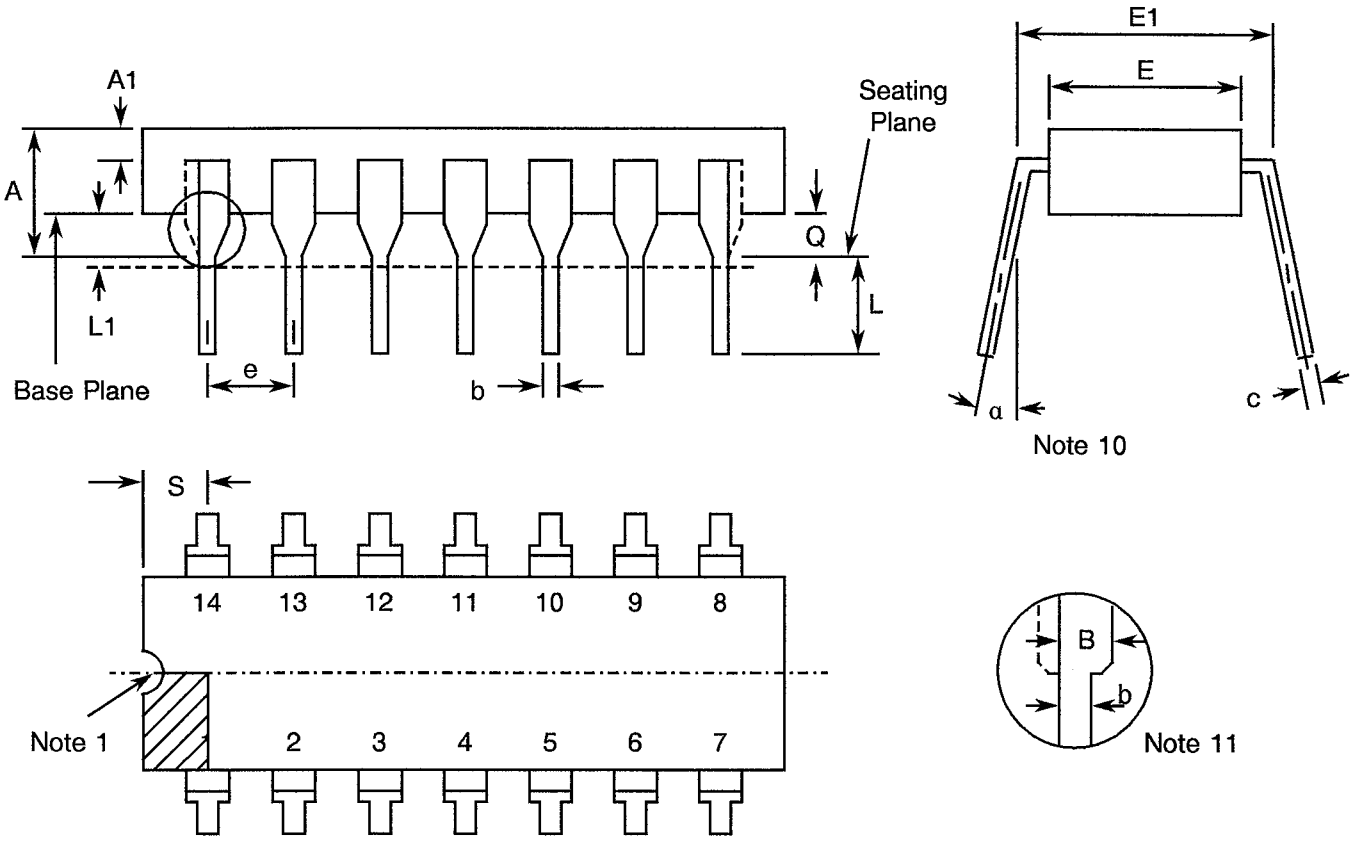


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	0.76	5.08	
b	0.25	0.58	8
c	0.08	0.15	8
D	-	7.11	
E	6.10	6.60	4
E2	3.18	-	
E3	0.76	-	
e	1.27 TYPICAL		5
k	0.20	0.38	
L	6.35	9.40	
Q	0.25	1.02	2
S1	0.13	-	
S2	0.10	-	7
α	30°	90°	

NOTES: See Page 12.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - DUAL-IN-LINE PACKAGE, 14 PIN

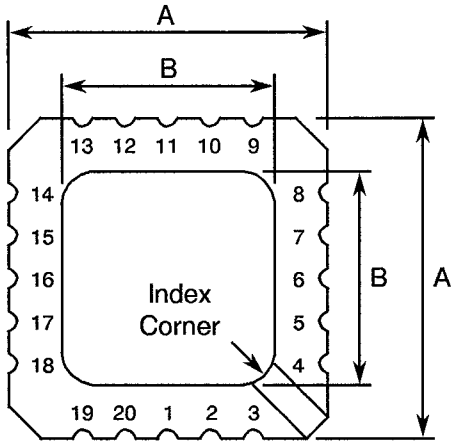


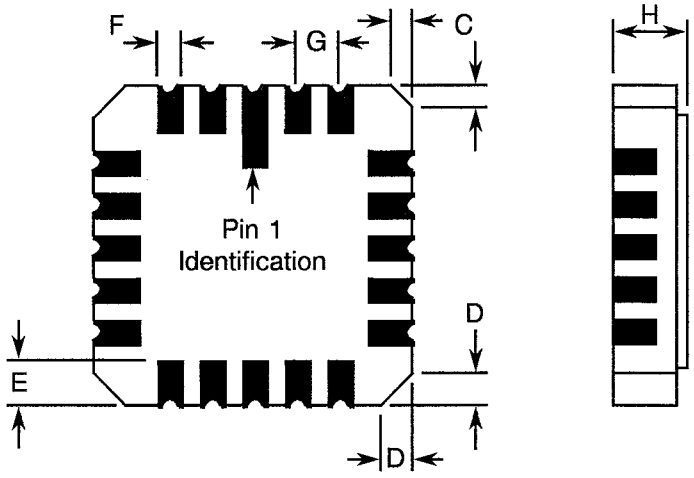
SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	-	5.08	
A1	-	2.03	
b	0.381	0.508	8
B	-	1.77	
c	0.204	0.304	8
e	2.54 TYPICAL		6, 9
E	6.30 TYPICAL		
E1	7.62	8.25	
L	2.5	3.9	8
L1	-	0.76	12
Q	0.51	-	3
S	Note 13	Note 13	7
α	0°	15°	10

NOTES: See Page 12.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(c) - SQUARE CHIP CARRIER PACKAGE (3 LAYER BASE), 20-TERMINAL





SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	8.69	9.09	
B	7.80	9.09	
C	0.25	0.51	14
D	0.89	1.14	15
E	1.14	1.40	8
F	0.56	0.71	8
G	1.27 TYPICAL		5, 9
H	1.63	2.54	

NOTES: See Page 12.

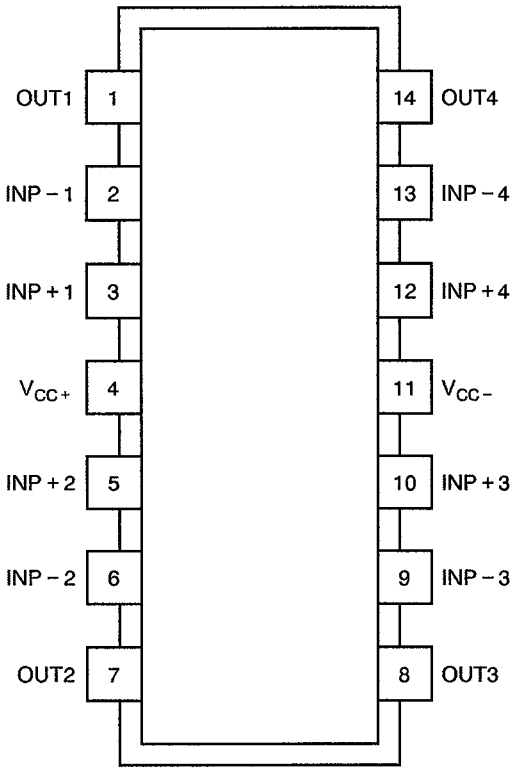
FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURES 2(a) TO 2(c) INCLUSIVE

1. Index area: a notch, letter or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown in Figure 2(c).
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. The dimension shall be measured from the seating plane to the base plane.
4. This dimension allows for off-centre lids, meniscus and glass overrun.
5. The true position pin or terminal spacing is 1.27mm between centrelines. Each pin or terminal centreline shall be located within ±0.13mm of its true longitudinal position relative to Pins 1 and the highest pin number.
6. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to Pins 1 and the highest pin number.
7. Applies to all 4 corners.
8. All leads or terminals.
9. 12 spaces for flat and dual-in-line packages.
   16 spaces for chip carrier packages.
10. Lead centre when α is 0°.
11. The lead profile is not required for the transition from B to b.
    The outline of the end pins in the case of F.105A may differ from that of the others.
12. The spacing between leads is measured within the area of L1.
13. Case F.105 : S between $e/2$ and e ($1.27mm < Z < 2.54mm$).
    Case F.105A : S less than $e/2$ ($S < 1.27mm$).
14. Index corner only - 2 dimensions.
15. 3 non-index corners - 6 dimensions.

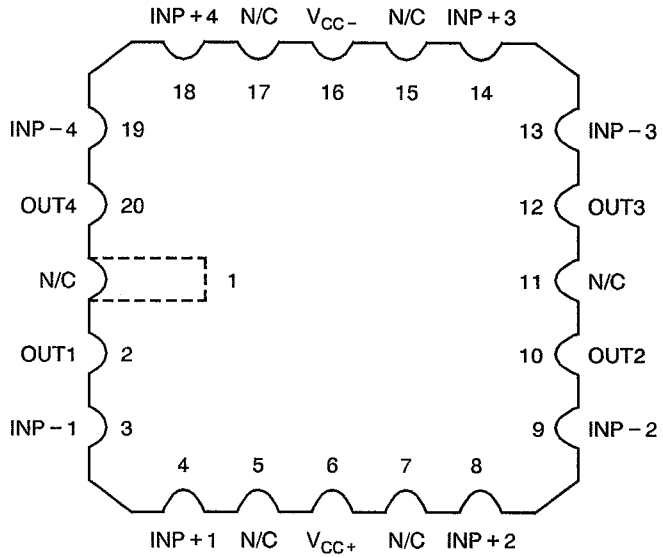
FIGURE 3(a) - PIN ASSIGNMENT

DUAL-IN-LINE AND FLAT PACKAGE



TOP VIEW

CHIP CARRIER PACKAGE



TOP VIEW

FLAT PACKAGE AND DUAL-IN-LINE TO CHIP CARRIER PIN ASSIGNMENT

FLAT PACKAGE AND DUAL-IN-LINE PIN OUTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14
CHIP CARRIER PIN OUTS	2	3	4	6	8	9	10	12	13	14	16	18	19	20

FIGURE 3(b) - TRUTH TABLE

Not applicable.

FIGURE 3(c) - CIRCUIT SCHEMATIC (EACH OPERATIONAL AMPLIFIER)

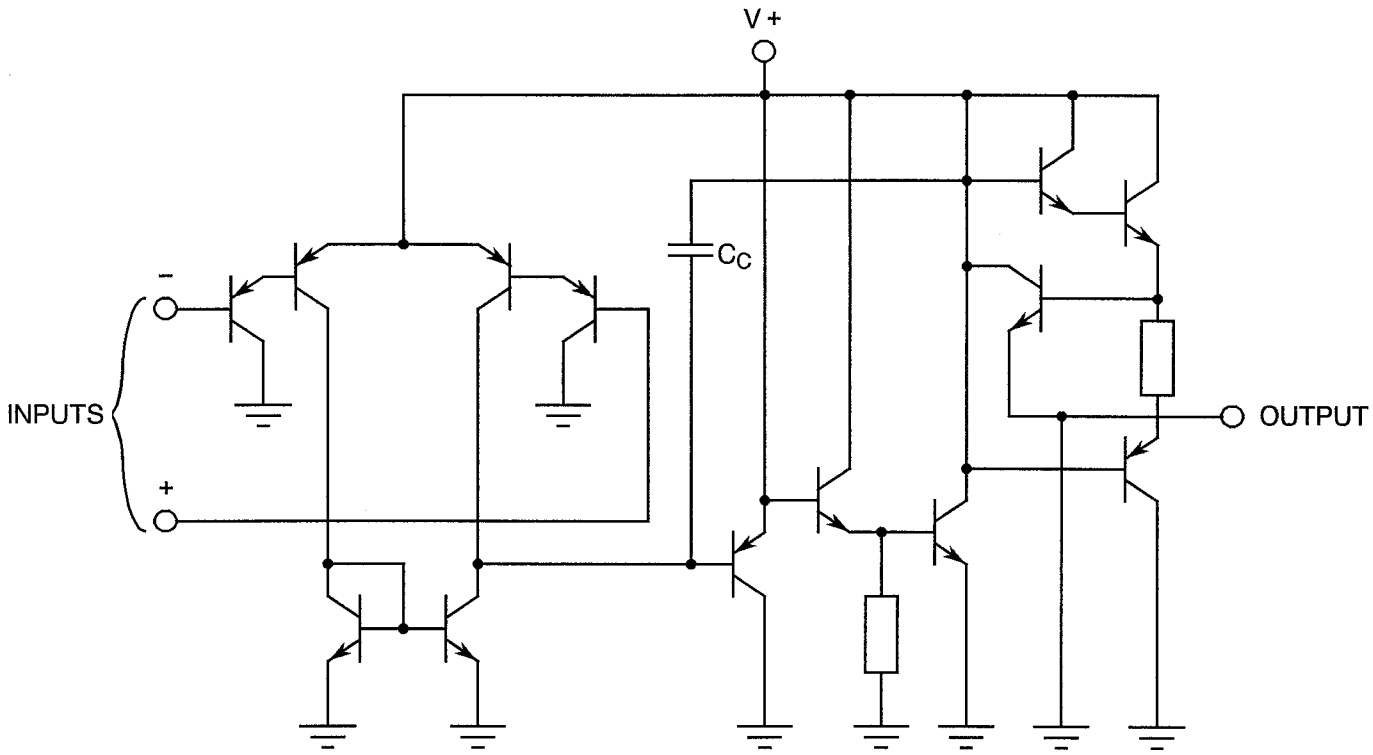
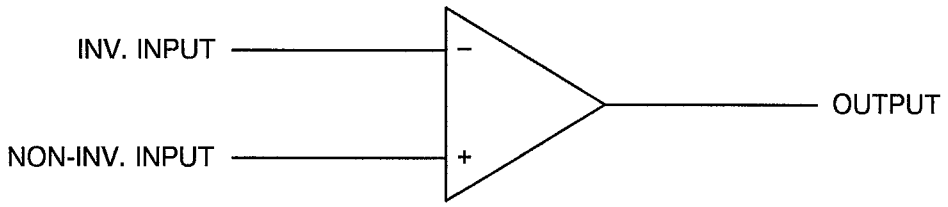


FIGURE 3(d) - FUNCTIONAL DIAGRAM



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2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

V_{CC} = Supply Voltage of the device under test.
PSRR = Power Supply Rejection Ratio.
OS = Overshoot.
t_r = Rise Time.
R_{SU} = Supply Resistance.
I_{CC} = Supply Current.
$I_{OS(t)}$ = Output Short Circuit Duration.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

(a) Para. 7.1.1(a), "High Temperature Reverse Bias" test and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 1.0 grammes for the flat package, 2.0 grammes for the dual-in-line package and 0.6 grammes for the chip carrier package.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed, preform-soldered or glass frit-sealed.

4.4.2 Lead Material and Finish

For dual-in-line and flat packages, the lead material shall be Type 'D' or Type 'G' with either Type '2', Type '3 or 4' or Type '4' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. For chip carrier packages, the finish shall be Type '2' in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700 and the following paragraphs. When the component is too small to accommodate all of the marking as specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence, shall be as follows:-

(a) Lead Identification.

(b) The SCC Component Number.

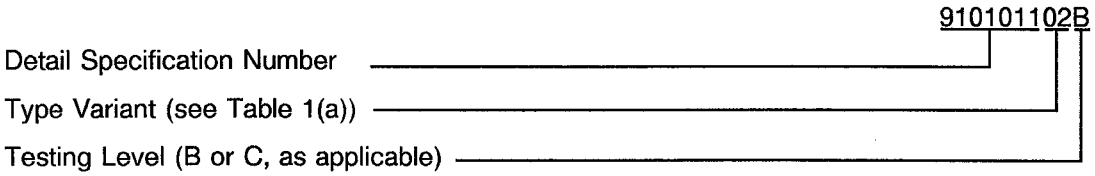
(c) Traceability Information.

4.5.2 Lead Identification

For dual-in-line and flat packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined in Figure 2(c).

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Tables 3(a) and 3(b). The measurements shall be performed at $T_{amb} = +125(+0-5)$ and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-in

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for High Temperature Reverse Bias Burn-in (Figure 5(a))

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

Circuits for use in performing the power burn-in tests are shown in Figure 5(b) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTE 1)	LIMITS (NOTE 6)		UNIT
							MIN	MAX	
1 to 4	Input Offset Voltage 1	V_{IO1}	4001	4(a)	E_1 (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V V_{IN} = −15V	−5.0 (−3.0)	+5.0 (+3.0)	mV
5 to 8	Input Offset Voltage 2	V_{IO2}	4001	4(a)	E_2 (V)	$+V_{CC}$ = 2.0V $-V_{CC}$ = −28V V_{IN} = 13V	−5.0 (−3.0)	+5.0 (+3.0)	mV
9 to 12	Input Offset Voltage 3	V_{IO3}	4001	4(a)	E_3 (V)	$+V_{CC}$ = 5.0V $-V_{CC}$ = 0V V_{IN} = −1.4V	−5.0 (−3.0)	+5.0 (+3.0)	mV
13 to 16	Input Offset Voltage 4	V_{IO4}	4001	4(a)	E_4 (V)	$+V_{CC}$ = 2.5V $-V_{CC}$ = −2.5V V_{IN} = 1.1V	−5.0 (−3.0)	+5.0 (+3.0)	mV
17 to 20	Input Offset Current 1	I_{IO1}	4001	4(b)	E_5 (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V R_S = 20kΩ V_{IN} = −15V	−30 (−20)	+30 (+20)	nA
21 to 24	Input Offset Current 2	I_{IO2}	4001	4(b)	E_6 (V)	$+V_{CC}$ = 2.0V $-V_{CC}$ = −28V R_S = 20kΩ V_{IN} = 13V	−30 (−20)	+30 (+20)	nA
25 to 28	Input Offset Current 3	I_{IO3}	4001	4(b)	E_7 (V)	$+V_{CC}$ = 5.0V $-V_{CC}$ = 0V R_S = 20kΩ V_{IN} = −1.4V	−30 (−20)	+30 (+20)	nA
29 to 32	Input Offset Current 4	I_{IO4}	4001	4(b)	E_8 (V)	$+V_{CC}$ = 2.5V $-V_{CC}$ = −2.5V R_S = 20kΩ V_{IN} = 1.1V	−30 (−20)	+30 (+20)	nA
33 to 36	Input (Plus) Bias Current 1	I_{+IB1}	4001	4(c)	E_9 (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V R_S = 20kΩ V_{IN} = −15V	−150 (−100)	−1.0	nA
37 to 40	Input (Plus) Bias Current 2	I_{+IB2}	4001	4(c)	E_{10} (V)	$+V_{CC}$ = 2.0V $-V_{CC}$ = −28V R_S = 20kΩ V_{IN} = 13V	−150 (−100)	−1.0	nA
41 to 44	Input (Plus) Bias Current 3	I_{+IB3}	4001	4(c)	E_{11} (V)	$+V_{CC}$ = 5.0V $-V_{CC}$ = 0V R_S = 20kΩ V_{IN} = −1.4V	−150 (−100)	−1.0	nA

NOTES: See Page 22.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTE 1)	LIMITS (NOTE 6)		UNIT
							MIN	MAX	
45 to 48	Input (Plus) Bias Current 4	I_{+IB4}	4001	4(c)	E_{12} (V)	$+V_{CC}$ = 2.5V $-V_{CC}$ = −2.5V R_S = 20kΩ V_{IN} = 1.1V	−150 (−100)	−1.0	nA
49 to 52	Input (Minus) Bias Current 1	I_{-IB1}	4001	4(d)	E_{13} (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V R_S = 20kΩ V_{IN} = −15V	−150 (−100)	−1.0	nA
53 to 56	Input (Minus) Bias Current 2	I_{-IB2}	4001	4(d)	E_{14} (V)	$+V_{CC}$ = 2.0V $-V_{CC}$ = −28V R_S = 20kΩ V_{IN} = 13V	−150 (−100)	−1.0	nA
57 to 60	Input (Minus) Bias Current 3	I_{-IB3}	4001	4(d)	E_{15} (V)	$+V_{CC}$ = 5.0V $-V_{CC}$ = 0V R_S = 20kΩ V_{IN} = −1.4V	−150 (−100)	−1.0	nA
61 to 64	Input (Minus) Bias Current 4	I_{-IB4}	4001	4(d)	E_{16} (V)	$+V_{CC}$ = 2.5V $-V_{CC}$ = −2.5V R_S = 20kΩ V_{IN} = 1.1V	−150 (−100)	−1.0	nA
65	Power Supply Current	$I_{CC(-)}$	4005	4(e)	$I_{CC(-)}$	$+V_{CC}$ = 30V $-V_{CC}$ = 0V	-	3.6 (3.0)	mA
66 to 69	Short Circuit Output Current (Plus)	$I_{OS(+)}$	3011	4(f)	I_{OS}	$+V_{CC}$ = 30V $-V_{CC}$ = 0V V_{IN} = −25V Note 2	−70 (−65)	-	mA
70 to 73	Open Loop Voltage Gain (Plus) 1	$+A_{VS1}$	4004	4(g)	E_{17} (V) E_{18} (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V R_L = 11.1kΩ V_{IN} = −26V $+V_{CC}$ = 30V $-V_{CC}$ = 0V R_L = 11.1kΩ V_{IN} = −1.0V	50	-	V/mV
74 to 77	Open Loop Voltage Gain (Plus) 2	$+A_{VS2}$	4004	4(g)	E_{19} (V) E_{20} (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V R_L = 2.05kΩ V_{IN} = −20V $+V_{CC}$ = 30V $-V_{CC}$ = 0V R_L = 2.05kΩ V_{IN} = −5.0V	50	-	V/mV

NOTES: See Page 22.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTE 1)	LIMITS (NOTE 6)		UNIT
							MIN	MAX	
78 to 81	Open Loop Voltage Gain 1	A_{VS1}	4004	4(g)	E_{21} (V) E_{22} (V)	$+V_{CC} = 5.0V$ $-V_{CC} = 0V$ $R_L = 11.1k\Omega$ $V_{IN} = -2.5V$ $+V_{CC} = 5.0V$ $-V_{CC} = 0V$ $R_L = 11.1k\Omega$ $V_{IN} = -1.0V$	10	-	V/mV
82 to 85	Open Loop Voltage Gain 2	A_{VS2}	4004	4(g)	E_{23} (V) E_{24} (V)	$+V_{CC} = 5.0V$ $-V_{CC} = 0V$ $R_L = 2.05k\Omega$ $V_{IN} = -2.5V$ $+V_{CC} = 5.0V$ $-V_{CC} = 0V$ $R_L = 2.05k\Omega$ $V_{IN} = -1.0V$	10	-	V/mV
86 to 89	Power Supply Rejection Ratio (Plus)	+PSRR1	4003	4(h)	E_{25} (V) E_{26} (V)	$+V_{CC} = 30V$ $-V_{CC} = 0V$ $V_{IN} = -1.4V$ $+V_{CC} = 5.0V$ $-V_{CC} = 0V$ $V_{IN} = -1.4V$	-100	100	µV/V
90 to 93	Common Mode Rejection Ratio	CMRR	4003	4(i)	E_{27} (V) E_{28} (V)	$+V_{CC} = 30V$ $-V_{CC} = 0V$ $V_{IN} = -15V$ $+V_{CC} = 2.0V$ $-V_{CC} = -28V$ $V_{IN} = 13V$	65	-	dB
94 to 97	Output Voltage Swing (Plus) 1	$V_{OUT(+)1}$	4004	4(g)	E_{29} (V)	$+V_{CC} = 30V$ $-V_{CC} = 0V$ $V_{IN} = -30V$ $R_L = 11.1k\Omega$	27	-	V
98 to 101	Output Voltage Swing (Plus) 2	$V_{OUT(+)2}$	4004	4(g)	E_{30} (V)	$+V_{CC} = 30V$ $-V_{CC} = 0V$ $V_{IN} = -30V$ $R_L = 2.05k\Omega$	26	-	V
102 to 105	Low Level Output Voltage 1	V_{OL1}	3007	4(j)	E_{31} (V)	$+V_{CC} = 30V$ $-V_{CC} = 0V$ $I_{OUT} = 5.0mA$ $V_{IN} = 5.0V$ Note 3	-	-1.5	V

NOTES: See Page 22.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTE 1)	LIMITS (NOTE 6)		UNIT
							MIN	MAX	
106 to 109	Low Level Output Voltage 2	V_{OL2}	3007	4(j)	E_{32} (V)	$+V_{CC} = 4.5V$ $-V_{CC} = 0V$ $I_{OUT} = 2.0\mu A$ $V_{IN} = 5.0V$ Note 3	-	0.4	V
110 to 113	Low Level Output Voltage 3	V_{OL3}	3007	4(j)	E_{33} (V)	$+V_{CC} = 30V$ $-V_{CC} = 0V$ $V_{IN} = 5.0V$ Notes 3 and 4	-	35	mV
114 to 117	High Level Output Voltage 1	V_{OH1}	3006	4(j)	E_{34} (V)	$+V_{CC} = 30V$ $-V_{CC} = 0V$ $I_{OUT} = 10mA$ $V_{IN} = -30V$ Note 3	27	-	V
118 to 121	High Level Output Voltage 2	V_{OH2}	3006	4(j)	E_{35} (V)	$+V_{CC} = 4.5V$ $-V_{CC} = 0V$ $I_{OUT} = 10mA$ $V_{IN} = -5.0V$ Note 3	2.4	-	V

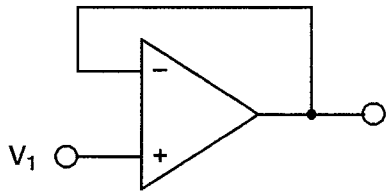
NOTES: See Page 22.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (NOTE 1)	LIMITS		UNIT
						MIN	MAX	
122 to 125	Slew Rate (Plus)	SR(+)	4002	4(k)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V R_L = 2.0kΩ V_{IN} = 5.0V to 15V Square Note 5	0.2	-	V/µs
126 to 129	Slew Rate (Minus)	SR(−)	4002	4(k)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V R_L = 2.0kΩ V_{IN} = 15V to 5.0V Square Note 5	0.2	-	V/µs
130 to 133	Rise Time	t_r	4002	4(k)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V R_L = 2.0kΩ V_{IN} = 50mV (Ref to 5.0V) Note 5	-	1.0	µs
134 to 137	Overshoot	OS	4002	4(k)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V R_L = 2.0kΩ V_{IN} = 50mV (Ref to 5.0V) Note 5	-	40	%

NOTES

1. Each amplifier shall be tested separately except for measurement of $I_{CC(-)}$. The amplifiers not under test shall be either maintained in a V_{IO} configuration such that the inputs are at the same common mode voltage as the DUT, or shall be maintained in the following configuration where V_1 is midway between $+V_{CC}$ and $-V_{CC}$:-



   For a.c. parameters the positive input shall be connected to Ground.

2. The duration of measurement of I_{OS} shall be ≤25ms.
3. Interchange of forcing and measuring function is permitted.
4. For measurement of V_{OL3} a load of 10kΩ shall be connected between output of DUT and Ground.
5. (i) Sample Test Inspection Level = II, AQL = 2.5%.

   (ii) Input pulse rise time shall be ≤50ns.
6. Limits without parenthesis are for all Variants. However, if parenthesised Limits are contained in a Limits Box, the Limits without parenthesis are for Variants 01 to 04, 09 and 11 and the Limits with parenthesis are for Variants 05 to 08, 10 and 12.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTE 1)	LIMITS (NOTE 6)		UNIT
							MIN	MAX	
1 to 4	Input Offset Voltage 1	V_{IO1}	4001	4(a)	E_1 (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V V_{IN} = −15V	−7.0 (−5.0)	+7.0 (+5.0)	mV
5 to 8	Input Offset Voltage 2	V_{IO2}	4001	4(a)	E_2 (V)	$+V_{CC}$ = 2.0V $-V_{CC}$ = −28V V_{IN} = 13V	−7.0 (−5.0)	+7.0 (+5.0)	mV
9 to 12	Input Offset Voltage 3	V_{IO3}	4001	4(a)	E_3 (V)	$+V_{CC}$ = 5.0V $-V_{CC}$ = 0V V_{IN} = −1.4V	−7.0 (−5.0)	+7.0 (+5.0)	mV
13 to 16	Input Offset Voltage 4	V_{IO4}	4001	4(a)	E_4 (V)	$+V_{CC}$ = 2.5V $-V_{CC}$ = −2.5V V_{IN} = 1.1V	−7.0 (−5.0)	+7.0 (+5.0)	mV
17 to 20	Input Offset Current 1	I_{IO1}	4001	4(b)	E_5 (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V R_S = 20kΩ V_{IN} = −15V	−100 (−50)	+100 (+50)	nA
21 to 24	Input Offset Current 2	I_{IO2}	4001	4(b)	E_6 (V)	$+V_{CC}$ = 2.0V $-V_{CC}$ = −28V R_S = 20kΩ V_{IN} = 13V	−100 (−50)	+100 (+50)	nA
25 to 28	Input Offset Current 3	I_{IO3}	4001	4(b)	E_7 (V)	$+V_{CC}$ = 5.0V $-V_{CC}$ = 0V R_S = 20kΩ V_{IN} = −1.4V	−100 (−50)	+100 (+50)	nA
29 to 32	Input Offset Current 4	I_{IO4}	4001	4(b)	E_8 (V)	$+V_{CC}$ = 2.5V $-V_{CC}$ = −2.5V R_S = 20kΩ V_{IN} = 1.1V	−100 (−50)	+100 (+50)	nA
33 to 36	Input (Plus) Bias Current 1	I_{+IB1}	4001	4(c)	E_9 (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V R_S = 20kΩ V_{IN} = −15V	−300 (−200)	−1.0	nA
37 to 40	Input (Plus) Bias Current 2	I_{+IB2}	4001	4(c)	E_{10} (V)	$+V_{CC}$ = 2.0V $-V_{CC}$ = −28V R_S = 20kΩ V_{IN} = 13V	−300 (−200)	−1.0	nA
41 to 44	Input (Plus) Bias Current 3	I_{+IB3}	4001	4(c)	E_{11} (V)	$+V_{CC}$ = 5.0V $-V_{CC}$ = 0V R_S = 20kΩ V_{IN} = −1.4V	−300 (−200)	−1.0	nA

NOTES: See Page 22.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTE 1)	LIMITS (NOTE 6)		UNIT
							MIN	MAX	
45 to 48	Input (Plus) Bias Current 4	I_{+IB4}	4001	4(c)	E_{12} (V)	$+V_{CC}=2.5V$ $-V_{CC}=-2.5V$ $R_S=20k\Omega$ $V_{IN}=1.1V$	−300 (−200)	−1.0	nA
49 to 52	Input (Minus) Bias Current 1	I_{-IB1}	4001	4(d)	E_{13} (V)	$+V_{CC}=30V$ $-V_{CC}=0V$ $R_S=20k\Omega$ $V_{IN}=-15V$	−300 (−200)	−1.0	nA
53 to 56	Input (Minus) Bias Current 2	I_{-IB2}	4001	4(d)	E_{14} (V)	$+V_{CC}=2.0V$ $-V_{CC}=-28V$ $R_S=20k\Omega$ $V_{IN}=13V$	−300 (−200)	−1.0	nA
57 to 60	Input (Minus) Bias Current 3	I_{-IB3}	4001	4(d)	E_{15} (V)	$+V_{CC}=5.0V$ $-V_{CC}=0V$ $R_S=20k\Omega$ $V_{IN}=-1.4V$	−300 (−200)	−1.0	nA
61 to 64	Input (Minus) Bias Current 4	I_{-IB4}	4001	4(d)	E_{16} (V)	$+V_{CC}=2.5V$ $-V_{CC}=-2.5V$ $R_S=20k\Omega$ $V_{IN}=1.1V$	−300 (−200)	−1.0	nA
65	Power Supply Current	$I_{CC(-)}$	4005	4(e)	$I_{CC(-)}$	$+V_{CC}=30V$ $-V_{CC}=0V$	-	4.0	mA
66 to 69	Short Circuit Output Current (Plus)	$I_{OS(+)}$	3011	4(f)	I_{OS}	$+V_{CC}=30V$ $-V_{CC}=0V$ $V_{IN}=-25V$ Note 2	−70 (−65)	-	mA
70 to 73	Open Loop Voltage Gain (Plus) 1	$+A_{VS1}$	4004	4(g)	E_{17} (V) E_{18} (V)	$+V_{CC}=30V$ $-V_{CC}=0V$ $R_L=1.11k\Omega$ $V_{IN}=-26V$ $+V_{CC}=30V$ $-V_{CC}=0V$ $R_L=1.11k\Omega$ $V_{IN}=-1.0V$	25	-	V/mV
74 to 77	Open Loop Voltage Gain (Plus) 2	$+A_{VS2}$	4004	4(g)	E_{19} (V) E_{20} (V)	$+V_{CC}=30V$ $-V_{CC}=0V$ $R_L=2.05k\Omega$ $V_{IN}=-20V$ $+V_{CC}=30V$ $-V_{CC}=0V$ $R_L=2.05k\Omega$ $V_{IN}=-5.0V$	25	-	V/mV

NOTES: See Page 22.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTE 1)	LIMITS (NOTE 6)		UNIT
							MIN	MAX	
78 to 81	Open Loop Voltage Gain 1	A_{VS1}	4004	4(g)	E_{21} (V) E_{22} (V)	$+V_{CC}$ = 5.0V $-V_{CC}$ = 0V R_L = 11.1kΩ V_{IN} = −2.5V $+V_{CC}$ = 5.0V $-V_{CC}$ = 0V R_L = 11.1kΩ V_{IN} = −1.0V	10	-	V/mV
82 to 85	Open Loop Voltage Gain 2	A_{VS2}	4004	4(g)	E_{23} (V) E_{24} (V)	$+V_{CC}$ = 5.0V $-V_{CC}$ = 0V R_L = 2.05kΩ V_{IN} = −2.5V $+V_{CC}$ = 5.0V $-V_{CC}$ = 0V R_L = 2.05kΩ V_{IN} = −1.0V	10	-	V/mV
86 to 89	Power Supply Rejection Ratio (Plus)	+PSRR1	4003	4(h)	E_{25} (V) E_{26} (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V V_{IN} = −1.4V $+V_{CC}$ = 5.0V $-V_{CC}$ = 0V V_{IN} = −1.4V	−100	100	µV/V
90 to 93	Common Mode Rejection Ratio	CMRR	4003	4(i)	E_{27} (V) E_{28} (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V V_{IN} = −15V $+V_{CC}$ = 2.0V $-V_{CC}$ = −28V V_{IN} = 13V	65	-	dB
94 to 97	Output Voltage Swing (Plus) 1	$V_{OUT(+)1}$	4004	4(g)	E_{29} (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V V_{IN} = −30V R_L = 11.1kΩ	27	-	V
98 to 101	Output Voltage Swing (Plus) 2	$V_{OUT(+)2}$	4004	4(g)	E_{30} (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V V_{IN} = −30V R_L = 2.05kΩ	26	-	V
102 to 105	Low Level Output Voltage 1	V_{OL1}	3007	4(j)	E_{31} (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V I_{OUT} = 5.0mA V_{IN} = 5.0V Note 3	-	−1.5	V

NOTES: See Page 22.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTE 1)	LIMITS (NOTE 6)		UNIT
							MIN	MAX	
106 to 109	Low Level Output Voltage 2	V_{OL2}	3007	4(j)	E_{32} (V)	$+V_{CC} = 4.5V$ $-V_{CC} = 0V$ $I_{OUT} = 2.0\mu A$ $V_{IN} = 5.0V$ Note 3	-	0.4	V
110 to 113	Low Level Output Voltage 3	V_{OL3}	3007	4(j)	E_{33} (V)	$+V_{CC} = 30V$ $-V_{CC} = 0V$ $V_{IN} = 5.0V$ Notes 3 and 4	-	35	mV
114 to 117	High Level Output Voltage 1	V_{OH1}	3006	4(j)	E_{34} (V)	$+V_{CC} = 30V$ $-V_{CC} = 0V$ $I_{OUT} = 10mA$ $V_{IN} = -30V$ Note 3	27	-	V
118 to 121	High Level Output Voltage 2	V_{OH2}	3006	4(j)	E_{35} (V)	$+V_{CC} = 4.5V$ $-V_{CC} = 0V$ $I_{OUT} = 10mA$ $V_{IN} = -5.0V$ Note 3	2.4	-	V

NOTES: See Page 22.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTE 1)	LIMITS (NOTE 6)		UNIT
							MIN	MAX	
1 to 4	Input Offset Voltage 1	V_{IO1}	4001	4(a)	E_1 (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V V_{IN} = −15V	−7.0 (−5.0)	+7.0 (+5.0)	mV
5 to 8	Input Offset Voltage 2	V_{IO2}	4001	4(a)	E_2 (V)	$+V_{CC}$ = 2.0V $-V_{CC}$ = −28V V_{IN} = 13V	−7.0 (−5.0)	+7.0 (+5.0)	mV
9 to 12	Input Offset Voltage 3	V_{IO3}	4001	4(a)	E_3 (V)	$+V_{CC}$ = 5.0V $-V_{CC}$ = 0V V_{IN} = −1.4V	−7.0 (−5.0)	+7.0 (+5.0)	mV
13 to 16	Input Offset Voltage 4	V_{IO4}	4001	4(a)	E_4 (V)	$+V_{CC}$ = 2.5V $-V_{CC}$ = −2.5V V_{IN} = 1.1V	−7.0 (−5.0)	+7.0 (+5.0)	mV
17 to 20	Input Offset Current 1	I_{IO1}	4001	4(b)	E_5 (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V R_S = 20kΩ V_{IN} = −15V	−100 (−50)	+100 (+50)	nA
21 to 24	Input Offset Current 2	I_{IO2}	4001	4(b)	E_6 (V)	$+V_{CC}$ = 2.0V $-V_{CC}$ = −28V R_S = 20kΩ V_{IN} = 13V	−100 (−50)	+100 (+50)	nA
25 to 28	Input Offset Current 3	I_{IO3}	4001	4(b)	E_7 (V)	$+V_{CC}$ = 5.0V $-V_{CC}$ = 0V R_S = 20kΩ V_{IN} = −1.4V	−100 (−50)	+100 (+50)	nA
29 to 32	Input Offset Current 4	I_{IO4}	4001	4(b)	E_8 (V)	$+V_{CC}$ = 2.5V $-V_{CC}$ = −2.5V R_S = 20kΩ V_{IN} = 1.1V	−100 (−50)	+100 (+50)	nA
33 to 36	Input (Plus) Bias Current 1	I_{+IB1}	4001	4(c)	E_9 (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V R_S = 20kΩ V_{IN} = −15V	−300 (−200)	−1.0	nA
37 to 40	Input (Plus) Bias Current 2	I_{+IB2}	4001	4(c)	E_{10} (V)	$+V_{CC}$ = 2.0V $-V_{CC}$ = −28V R_S = 20kΩ V_{IN} = 13V	−300 (−200)	−1.0	nA
41 to 44	Input (Plus) Bias Current 3	I_{+IB3}	4001	4(c)	E_{11} (V)	$+V_{CC}$ = 5.0V $-V_{CC}$ = 0V R_S = 20kΩ V_{IN} = −1.4V	−300 (−200)	−1.0	nA

NOTES: See Page 22.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, −55(+5−0) °C (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTE 1)	LIMITS (NOTE 6)		UNIT
							MIN	MAX	
45 to 48	Input (Plus) Bias Current 4	I_{+IB4}	4001	4(c)	E_{12} (V)	$+V_{CC}$ = 2.5V $-V_{CC}$ = −2.5V R_S = 20kΩ V_{IN} = 1.1V	−300 (−200)	−1.0	nA
49 to 52	Input (Minus) Bias Current 1	I_{-IB1}	4001	4(d)	E_{13} (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V R_S = 20kΩ V_{IN} = −15V	−300 (−200)	−1.0	nA
53 to 56	Input (Minus) Bias Current 2	I_{-IB2}	4001	4(d)	E_{14} (V)	$+V_{CC}$ = 2.0V $-V_{CC}$ = −28V R_S = 20kΩ V_{IN} = 13V	−300 (−200)	−1.0	nA
57 to 60	Input (Minus) Bias Current 3	I_{-IB3}	4001	4(d)	E_{15} (V)	$+V_{CC}$ = 5.0V $-V_{CC}$ = 0V R_S = 20kΩ V_{IN} = −1.4V	−300 (−200)	−1.0	nA
61 to 64	Input (Minus) Bias Current 4	I_{-IB4}	4001	4(d)	E_{16} (V)	$+V_{CC}$ = 2.5V $-V_{CC}$ = −2.5V R_S = 20kΩ V_{IN} = 1.1V	−300 (−200)	−1.0	nA
65	Power Supply Current	$I_{CC(-)}$	4005	4(e)	$I_{CC(-)}$	$+V_{CC}$ = 30V $-V_{CC}$ = 0V	-	4.0	mA
66 to 69	Short Circuit Output Current (Plus)	$I_{OS(+)}$	3011	4(f)	I_{OS}	$+V_{CC}$ = 30V $-V_{CC}$ = 0V V_{IN} = −25V Note 2	−70	-	mA
70 to 73	Open Loop Voltage Gain (Plus) 1	$+A_{VS1}$	4004	4(g)	E_{17} (V) E_{18} (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V R_L = 11.1kΩ V_{IN} = −26V $+V_{CC}$ = 30V $-V_{CC}$ = 0V R_L = 11.1kΩ V_{IN} = −1.0V	25	-	V/mV
74 to 77	Open Loop Voltage Gain (Plus) 2	$+A_{VS2}$	4004	4(g)	E_{19} (V) E_{20} (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V R_L = 2.05kΩ V_{IN} = −20V $+V_{CC}$ = 30V $-V_{CC}$ = 0V R_L = 2.05kΩ V_{IN} = −5.0V	25	-	V/mV

NOTES: See Page 22.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, −55(+5−0) °C (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTE 1)	LIMITS (NOTE 6)		UNIT
							MIN	MAX	
78 to 81	Open Loop Voltage Gain 1	A_{VS1}	4004	4(g)	E_{21} (V) E_{22} (V)	$+V_{CC}$ = 5.0V $-V_{CC}$ = 0V R_L = 11.1kΩ V_{IN} = −2.5V $+V_{CC}$ = 5.0V $-V_{CC}$ = 0V R_L = 11.1kΩ V_{IN} = −1.0V	10	-	V/mV
82 to 85	Open Loop Voltage Gain 2	A_{VS2}	4004	4(g)	E_{23} (V) E_{24} (V)	$+V_{CC}$ = 5.0V $-V_{CC}$ = 0V R_L = 2.05kΩ V_{IN} = −2.5V $+V_{CC}$ = 5.0V $-V_{CC}$ = 0V R_L = 2.05kΩ V_{IN} = −1.0V	10	-	V/mV
86 to 89	Power Supply Rejection Ratio (Plus)	+PSRR1	4003	4(h)	E_{25} (V) E_{26} (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V V_{IN} = −1.4V $+V_{CC}$ = 5.0V $-V_{CC}$ = 0V V_{IN} = −1.4V	−100	100	µV/V
90 to 93	Common Mode Rejection Ratio	CMRR	4003	4(i)	E_{27} (V) E_{28} (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V V_{IN} = −15V $+V_{CC}$ = 2.0V $-V_{CC}$ = −28V V_{IN} = 13V	65	-	dB
94 to 97	Output Voltage Swing (Plus) 1	$V_{OUT(+)1}$	4004	4(g)	E_{29} (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V V_{IN} = −30V R_L = 11.1kΩ	27	-	V
98 to 101	Output Voltage Swing (Plus) 2	$V_{OUT(+)2}$	4004	4(g)	E_{30} (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V V_{IN} = −30V R_L = 2.05kΩ	26	-	V
102 to 105	Low Level Output Voltage 1	V_{OL1}	3007	4(j)	E_{31} (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V I_{OUT} = 5.0mA V_{IN} = 5.0V Note 3	-	−1.5	V

NOTES: See Page 22.

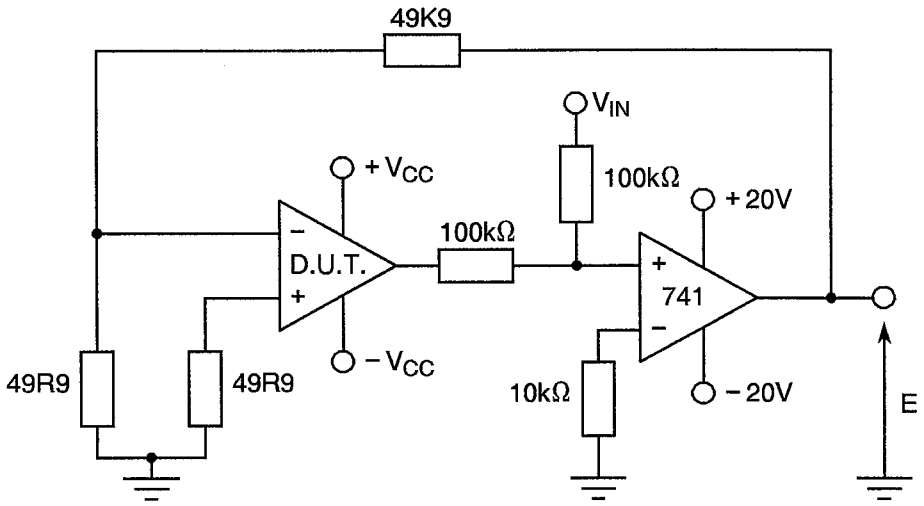
TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, −55(+5−0) °C (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTE 1)	LIMITS (NOTE 6)		UNIT
							MIN	MAX	
106 to 109	Low Level Output Voltage 2	V_{OL2}	3007	4(j)	E_{32} (V)	$+V_{CC}$ = 4.5V $-V_{CC}$ = 0V I_{OUT} = 2.0µA V_{IN} = 5.0V Note 3	-	0.4	V
110 to 113	Low Level Output Voltage 3	V_{OL3}	3007	4(j)	E_{33} (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V V_{IN} = 5.0V Notes 3 and 4	-	35	mV
114 to 117	High Level Output Voltage 1	V_{OH1}	3006	4(j)	E_{34} (V)	$+V_{CC}$ = 30V $-V_{CC}$ = 0V I_{OUT} = 10mA V_{IN} = −30V Note 3	27	-	V
118 to 121	High Level Output Voltage 2	V_{OH2}	3006	4(j)	E_{35} (V)	$+V_{CC}$ = 4.5V $-V_{CC}$ = 0V I_{OUT} = 10mA V_{IN} = −5.0V Note 3	2.3	-	V

NOTES: See Page 22.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - INPUT OFFSET VOLTAGE

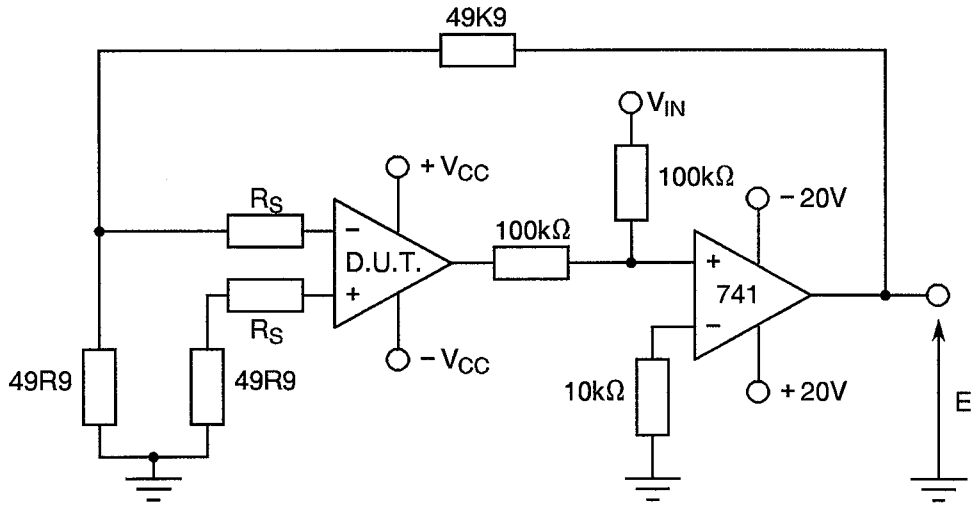


V_{IO1} (mV) = E_1 (V), V_{IO2} (mV) = E_2 (V), V_{IO3} (mV) = E_3 (V), V_{IO4} (mV) = E_4 (V)

NOTES

1. All resistors to be 0.1% tolerance.

FIGURE 4(b) - INPUT OFFSET CURRENT



$$I_{IO1}\ (nA) = \frac{(E_1\ (V) - E_5\ (V))\ 10^6}{R_S\ (k\Omega)} \qquad I_{IO2}\ (nA) = \frac{(E_2\ (V) - E_6\ (V))\ 10^6}{R_S\ (k\Omega)}$$

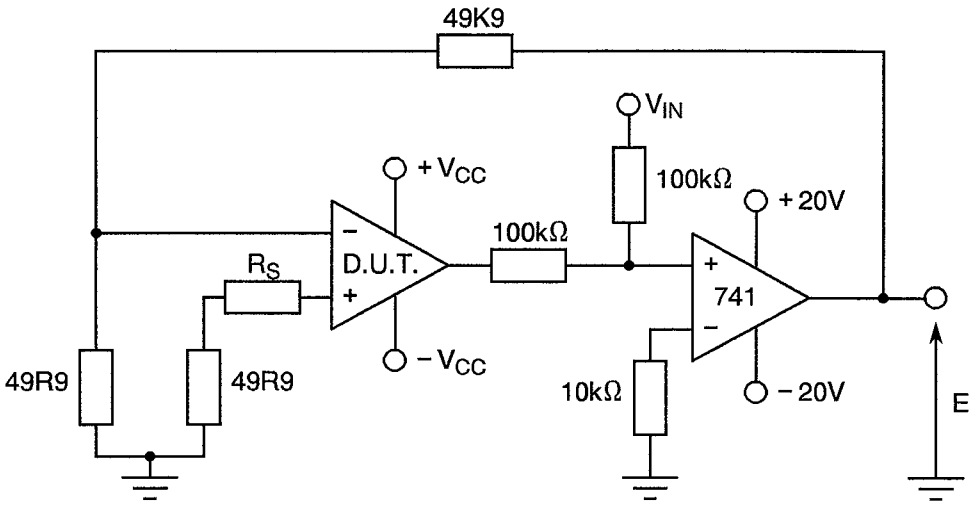
$$I_{IO3}\ (nA) = \frac{(E_3\ (V) - E_7\ (V))\ 10^6}{R_S\ (k\Omega)} \qquad I_{IO4}\ (nA) = \frac{(E_4\ (V) - E_8\ (V))\ 10^6}{R_S\ (k\Omega)}$$

NOTES

1. All resistors to be 0.1% tolerance.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(c) - INPUT (PLUS) BIAS CURRENT



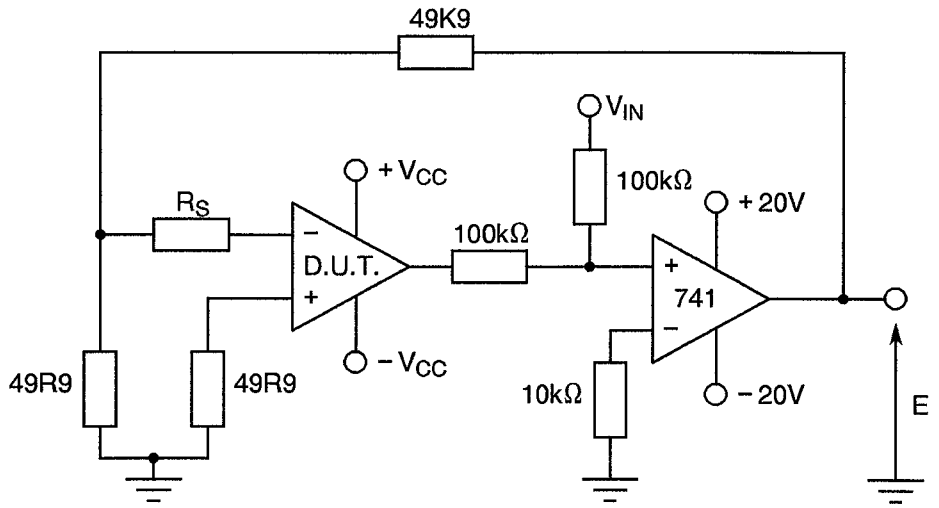
$$I_{+IB1}\ (nA) = \frac{(E_1\ (V) - E_9\ (V))\ 10^6}{R_S\ (k\Omega)} \qquad I_{+IB2}\ (nA) = \frac{(E_2\ (V) - E_{10}\ (V))\ 10^6}{R_S\ (k\Omega)}$$

$$I_{+IB3}\ (nA) = \frac{(E_3\ (V) - E_{11}\ (V))\ 10^6}{R_S\ (k\Omega)} \qquad I_{+IB4}\ (nA) = \frac{(E_4\ (V) - E_{12}\ (V))\ 10^6}{R_S\ (k\Omega)}$$

NOTES

1. All resistors to be 0.1% tolerance.

FIGURE 4(d) - INPUT (MINUS) BIAS CURRENT



$$I_{-IB1}\ (nA) = \frac{(E_{13}\ (V) - E_1\ (V))\ 10^6}{R_S\ (k\Omega)} \qquad I_{-IB2}\ (nA) = \frac{(E_{14}\ (V) - E_2\ (V))\ 10^6}{R_S\ (k\Omega)}$$

$$I_{-IB3}\ (nA) = \frac{(E_{15}\ (V) - E_3\ (V))\ 10^6}{R_S\ (k\Omega)} \qquad I_{-IB4}\ (nA) = \frac{(E_{16}\ (V) - E_4\ (V))\ 10^6}{R_S\ (k\Omega)}$$

NOTES

1. All resistors to be 0.1% tolerance.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(e) - SUPPLY CURRENT

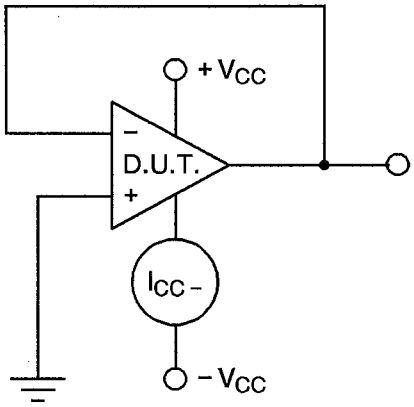
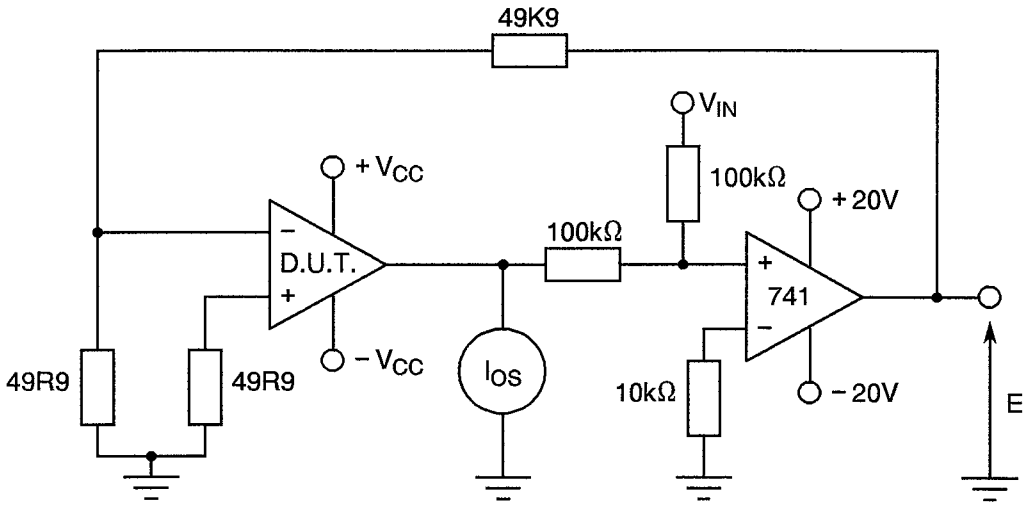


FIGURE 4(f) - SHORT CIRCUIT OUTPUT CURRENT

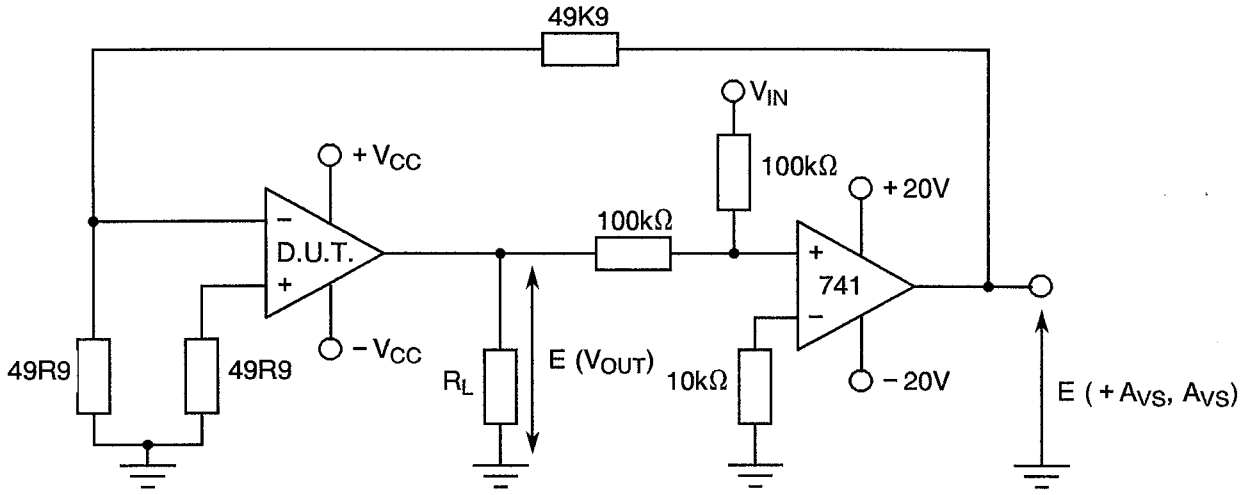


NOTES

1. All resistors to be 0.1% tolerance.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(g) - OUTPUT VOLTAGE SWING AND OPEN LOOP VOLTAGE GAIN



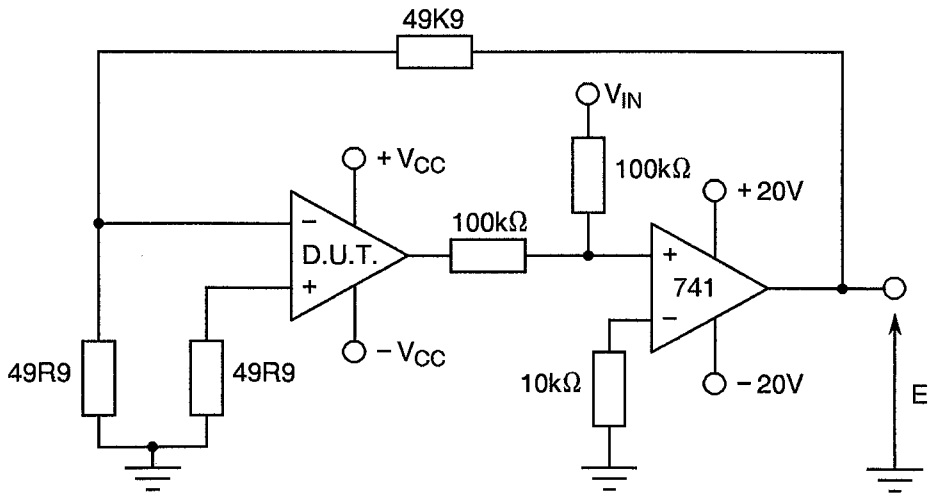
1. V_{OUT} = (E_{29}, E_{30}) V

2. $+A_{VS1} = \frac{25}{E_{18} - E_{17}}$ $+A_{VS2} = \frac{15}{E_{20} - E_{19}}$

3. $A_{VS1} = \frac{2}{E_{22} - E_{21}}$ $A_{VS2} = \frac{2}{E_{24} - E_{23}}$

NOTES
1. All resistors to be 0.1% tolerance.
2. E_{17} to E_{24} inclusive in volts.

FIGURE 4(h) - POWER SUPPLY REJECTION RATIO

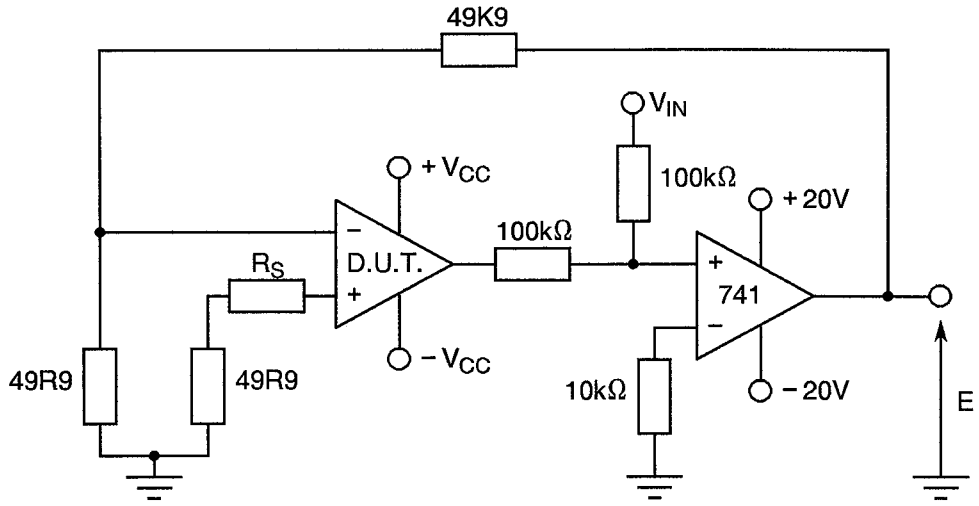


+PSRR (μV/V) = (E_{25} (V) − E_{26} (V)) 40

NOTES
1. All resistors to be 0.1% tolerance.
2. E_{25}, E_{26} are measured to 4 digits tolerance.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - COMMON MODE REJECTION RATIO



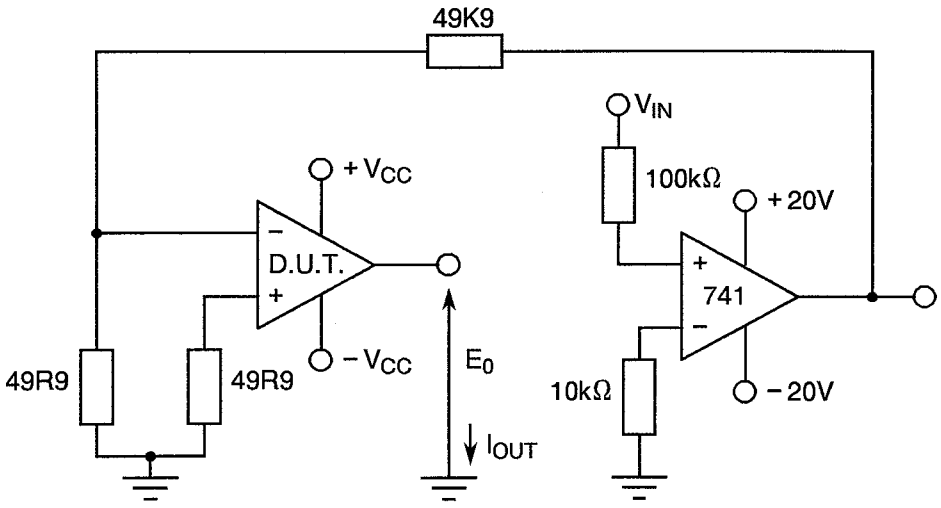
$$CMRR\ (dB) = 20Log\ \frac{2.8 \times 10^4}{E_{27}\ (V)\ -\ E_{28}\ (V)}$$

where $E_{27}\ (V) = E_1\ (V)$ and $E_{28}\ (V) = E_2\ (V)$.

NOTES

1. Resistors of 49R9 at inputs shall be 0.01% tolerance matched to 0.001%. Remaining resistors shall be of 0.1% tolerance.

FIGURE 4(j) - OUTPUT VOLTAGE LOW AND HIGH LEVEL

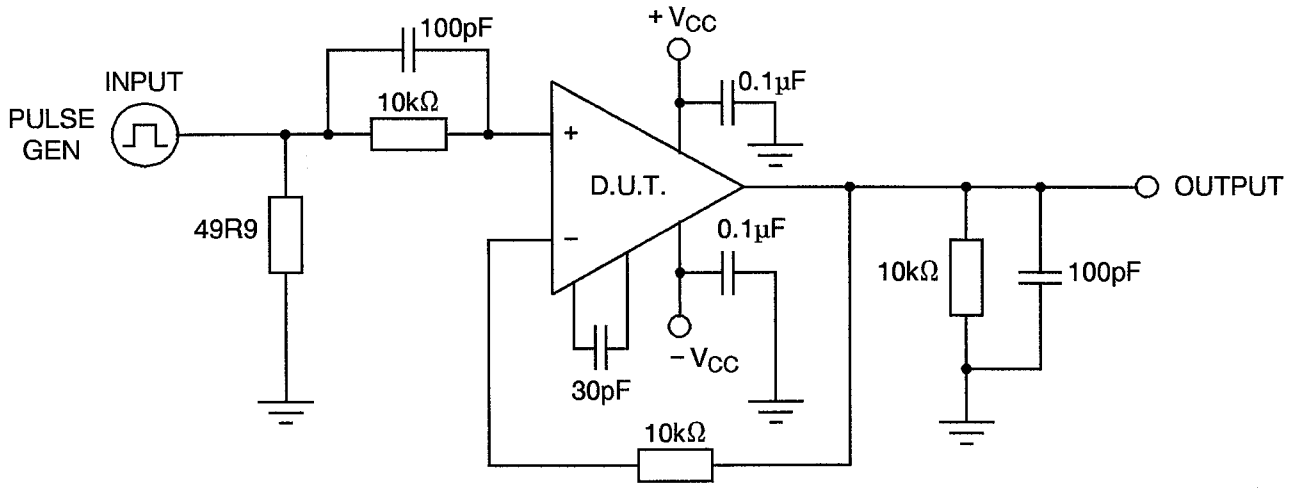


NOTES

1. Resistors of 49R9 at inputs shall be 0.01% tolerance matched to 0.001%. Remaining resistors shall be of 0.1% tolerance.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

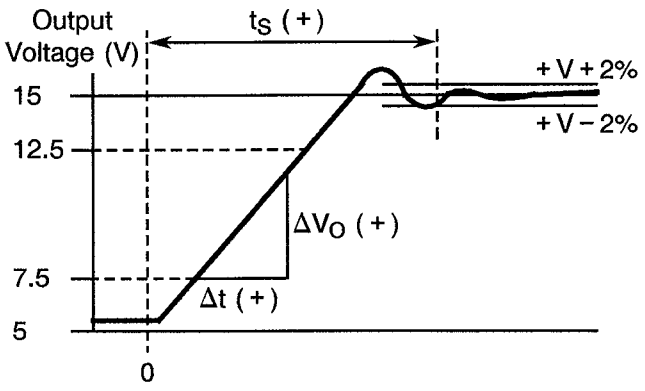
FIGURE 4(k) - DYNAMIC TEST MEASUREMENT CIRCUIT



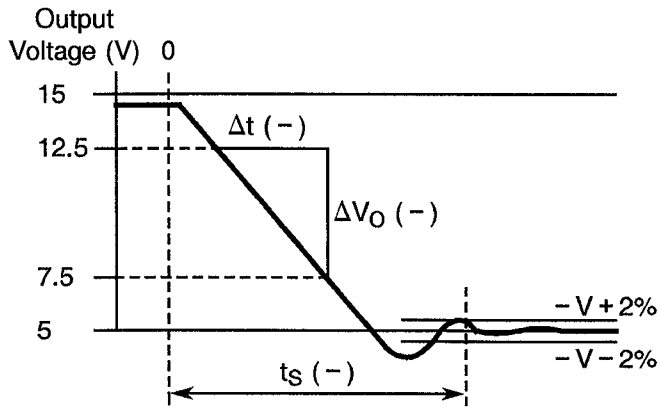
NOTES

1. Pulse Generator: rise time ≤ 50ns, repetition rate 1.0kHz (max.).
2. All resistors are ± 0.1% tolerance and capacitors are ± 10% tolerance.

SLEW RATE WAVEFORMS

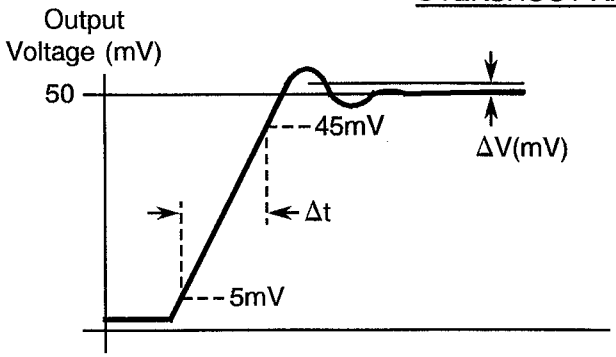


$$SR(+) = \frac{\Delta V_O (+)}{\Delta t (+)} \ (V/\mu s)$$



$$SR(-) = \frac{\Delta V_O (-)}{\Delta t (-)} \ (V/\mu s)$$

OVERSHOOT AND RISE TIME WAVEFORMS



$$t_r = \Delta t$$

$$OS = \frac{\Delta V}{50} \times 100\%$$

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
9 to 12	Input Offset Voltage 3 Change	V_{IO3}	As per Table 2	As per Table 2	± 1.0	mV
25 to 28	Input Offset Current 3 Change	I_{IO3}	As per Table 2	As per Table 2	± 5.0	nA
41 to 44	Input (Plus) Bias Current 3 Change	I_{+IB3}	As per Table 2	As per Table 2	± 50	nA
57 to 60	Input (Minus) Bias Current 3 Change	I_{-IB3}	As per Table 2	As per Table 2	± 50	nA

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

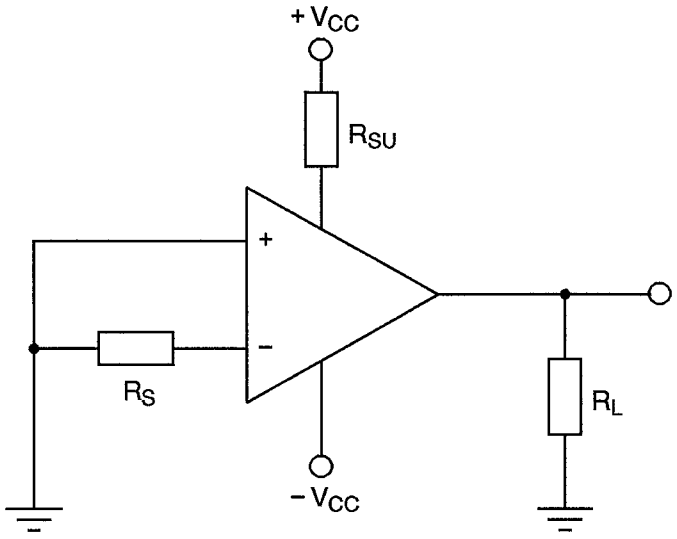
TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+ 125 ± 5	°C
2	Supply Voltage	V_{CC}	± 15	V
3	Load Resistance	R_L	10k	Ω
4	Source Resistance	R_S	1.0k	Ω
5	Supply Resistance	R_{SU}	5.0	Ω

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



NOTES

1. Remaining 3 amplifiers shall be connected as per Figure 5(b).

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests (Part of Endurance Testing)

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(b) of this specification.

4.8.6 Conditions for High Temperature Storage Test (Part of Endurance Testing)

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS (NOTE 1)		UNIT
					MIN.	MAX.	
9 to 12	Input Offset Voltage 3	V_{IO3}	As per Table 2	As per Table 2	−5.0 (−3.0)	+5.0 (+3.0)	mV
25 to 28	Input Offset Current 3	I_{IO3}	As per Table 2	As per Table 2	−30 (−20)	+30 (+20)	nA
41 to 44	Input (Plus) Bias Current 3	I_{+IB3}	As per Table 2	As per Table 2	−150 (−100)	−1.0	nA
65	Power Supply Current	$I_{CC(-)}$	As per Table 2	As per Table 2	-	3.6 (3.0)	mA
70 to 73	Open Loop Voltage Gain (Plus) 1	$+A_{VS1}$	As per Table 2	As per Table 2	50	-	V/mV

NOTES

1. Limits without parenthesis are for all Variants. However, if parenthesised Limits are contained in a Limits Box, the Limits without parenthesis are for Variants 01 to 04, 09 and 11 and the Limits with parenthesis are for Variants 05 to 08, 10 and 12.