european space agency
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Pages 1 to 43

INTEGRATED CIRCUITS, SILICON MONOLITHIC,

BIPOLAR VOLTAGE COMPARATOR

BASED ON TYPE LM111

ESA/SCC Detail Specification No. 9103/002

SCC

space components
coordination group

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		SCCG Chairman	ESA Director General or his Deputy
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DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
		This issue supersedes Issue 2 and incorporates the modifications agreed on the basis of Policy DCR 21019 (Appendices to Detail Specifications), DCR 23058 (new Tables 2, 3(a), 3(b) and Figure 4 format), DCR 24006 (addition of Appendix 'A' for Thomson-CSF alternative circuit) and the following:-		
		P7. Table 1(b)	: Addition of power derating information and max. junction temperature	22104
		P8. Figure 1	: Added	22104
		P14. Figure 3(b)	: Modification of Title	22104
		P16. Para. 3	: Modification of abbreviations	22104
		P20. Table 2	: Output leakage current limit amended	22104
			: I_{OSTB} test replaced by V_{OSTB}	22104
		P21. Table 2	: I_I, I_{OS} and A_{VD} limits amended	22104
		P23. Table 3(a)	: Output leakage current limit amended	22104
			: I_{OSTB} test replaced by V_{OSTB}	22104
		P24. Table 3(a)	: I_I, I_{OS} and A_{VD} limits amended	22104
		P25. Table 3(b)	: Output leakage current limit deleted	22104
			: I_{OSTB} test replaced by V_{OSTB}	22104
		P26. Table 3(b)	: I_I, I_{OS} and A_{VD} limits amended	22104
		P35. Figure 5	: New burn-in circuit	22104
		P37. Table 6	: Modification of A_{VD} limit	22104
'A'	Jun. '81	P1. Cover page		None
		P2. DCN		None
		P21. Table 2	: Modification of Test 15 input conditions	23070
		P22. Table 2	: Amendment of Title	23070
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		P26. Table 3(b)	: Modification of test 15 input conditions	23070

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference	CHANGE Item	Approved DCR No.
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		P2A. DCN	: Page added	None
		P6. Table 1(a)	: Lead material and finish re-defined	21025
		P7. Table 1(b)	: Note 2, 3 and 4 derating factors amended. Format amended	22293
		P8. Figure 1	: Amended	22293
		P16. Para. 2	: MIL-STD-1276 deleted	21025
		Para. 4.2.2	: PIND test added	22240
		P18. Para. 4.4.2	: Paragraph re-written	21025
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		P2A. DCN		None
		P3. T of C	: Para. 4.3.3 deleted	None
		P6. Table 1(a)	: Variant 07 added	22912
		P7. Table 1(b)	: No. 5, Characteristics amended to include Variant 07	22912
		P16. Para. 4.2.2	: Deviation deleted, "None." added	21048
		P17. Para. 4.2.4	: Deviation deleted, "None." added	22919
		Para. 4.2.5	: Deviation deleted, "None." added	22919
		Para. 4.3.2	: Paragraph amended to include Variant 07	22912
		Para. 4.3.3	: Paragraph deleted	22921
		P18. Para. 4.4.2	: Paragraph amended	22912
		Para. 4.5.2	: Paragraph amended to include Variant 07	22912
'D'	Oct. '94	P1. Cover page		None
		P2A. DCN		None
		P6. Table 1(a)	: Variant 08, "Chip Carrier" added	221109
		P7. Table 1(b)	: Item 5, Variant 08 added	221109
		P8. Figure 1	: Note 1, Variant 08 added	221109
		P9. Figure 2(a)	: Imperial dimensions deleted, number of pins added	221109
		P10. Figure 2(b)	: Imperial dimensions deleted, number of pins added	221109
		P11. Figure 2(c)	: Imperial dimensions deleted, number of pins added	221109
		P12/ Figure 2(d) P12A	: "Chip Carrier Package" added, old Page 12 renumbered "12A" and Chip Carrier Package added	221109
		P13. Figure 3(iii)	: Renumbered to 3(iv)	221109
		P17. Para. 4.3.2	: Variant 08 added	221109
		P18. Para. 4.4.2	: Variant 08 added and text rewritten	221109
		Para. 4.5.2	: Variant 08 added and text rewritten	221109
		This specification has been transferred from hardcopy to electronic format. The content is unchanged but minor differences in presentation exist.		

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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, bipolar voltage compatator, based on Type LM111. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

As per Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the integrated circuits specified herein are shown in Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

Not applicable.

1.8 CIRCUIT SCHEMATIC

As per Figure 3(b).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(c).

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	FLAT	2(a)	D2
02	FLAT	2(a)	D3 or D4
03	TO99	2(b)	D2
04	TO99	2(b)	D3 or D4
05	DIL	2(c)	D2
06	DIL	2(c)	D3 or D4
07	TO99	2(b)	D9
08	CHIP CARRIER	2(d)	2

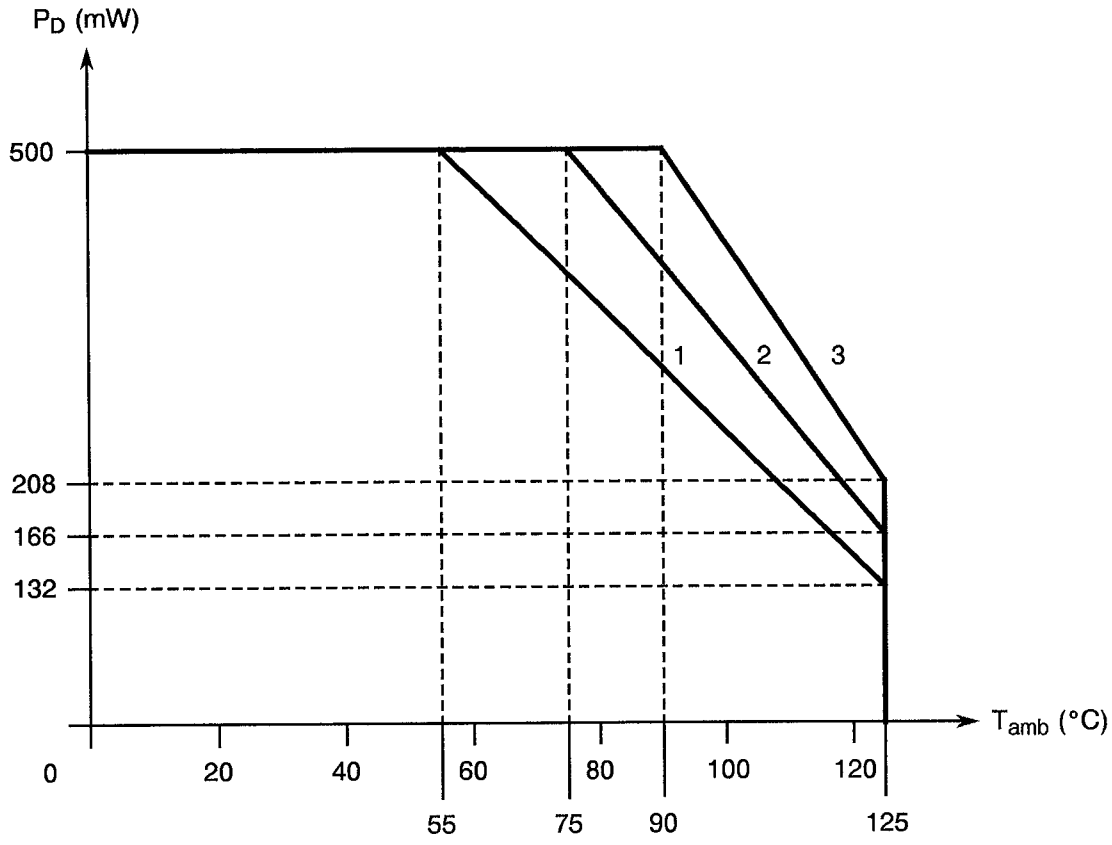
TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNITS	REMARKS
1	Supply Voltage Range	V_S	36	V	
2	Differential Input Voltage Range	V_{ID}	±30	V	
3	Voltage to Negative Supply Voltage	V 1-4 V 7-4	30 50	V	
4	Input Voltage Range	V_I	±15	V	Note 1
5	Device Power Dissipation - Type Variants 01-02-08 - Type Variants 03-04-07 - Type Variants 05-06	P_D	500	mW	 Note 2 Note 3 Note 4
6	Output Short Circuit Duration	-	10	sec.	
7	Operating Temperature Range	T_{amb}	−55 to +125	°C	
8	Storage Temperature Range	T_{stg}	−55 to +150	°C	
9	Soldering Temperature	T_{sol}	+300	°C	Note 5
10	Junction Temperature	T_j	+150	°C	

NOTES

1. This rating applies to ±15V supplies. The positive input voltage limit is 30V higher than the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V lower than the positive supply, whichever is less.
2. Derate above T_{amb} = +55°C at 5.26mW/°C.
3. Derate above T_{amb} = +75°C at 6.67mW/°C.
4. Derate above T_{amb} = +90°C at 8.33mW/°C.
5. Duration: 2 to 5 seconds

FIGURE 1 - DEVICE DISSIPATION DERATING WITH TEMPERATURE

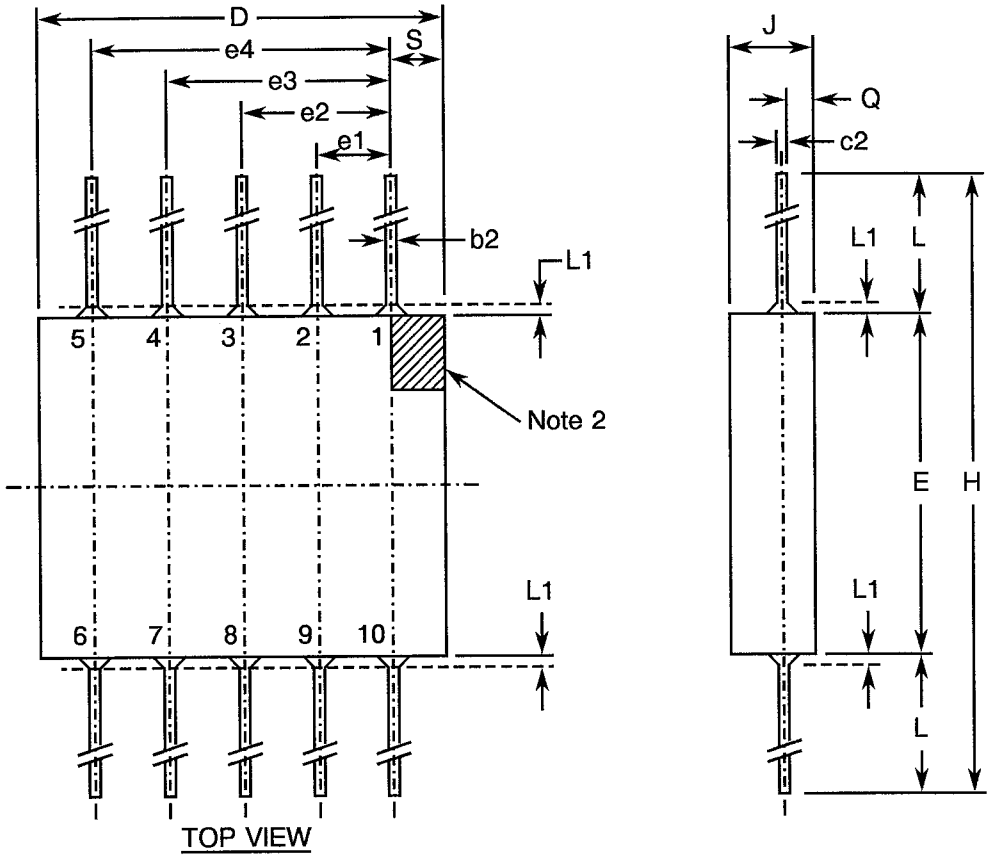


NOTES

1. Derating for type variants 01, 02 and 08.
2. Derating for type variants 03 and 04.
3. Derating for type variants 05 and 06.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE, 10-PIN



TOP VIEW

SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
b2	0.254	0.482	
c2	0.077	0.152	
D	6.10	6.98	
E	6.10	6.60	
e1	1.15	1.39	1
e2	2.42	2.66	1
e3	3.69	3.93	1
e4	4.96	5.20	1
H	13.72	19.81	
J	0.77	1.77	
L	3.81	6.60	
L1	-	0.38	
Q	0.13	0.88	
S	0.51	0.88	

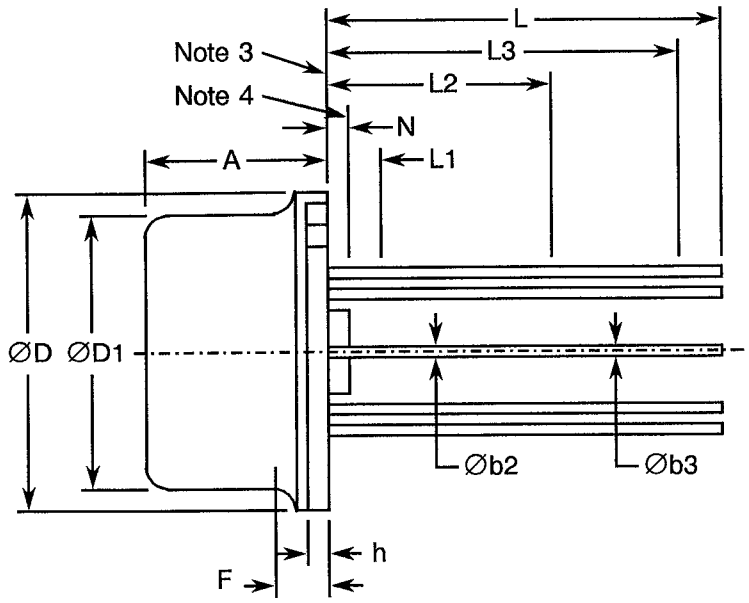
NOTES

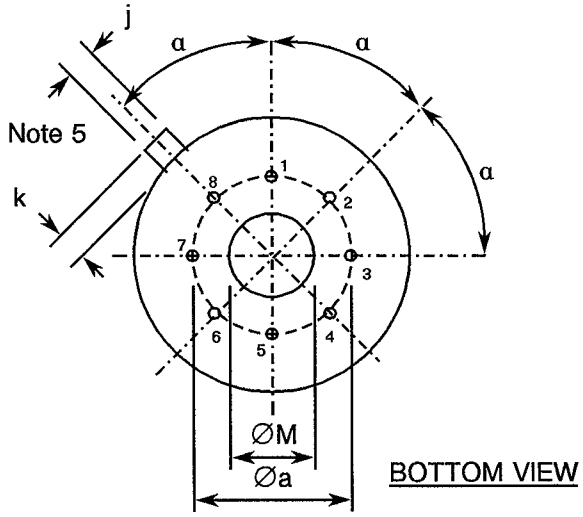
1. The space between terminals has to be measured at a distance of 0.76mm maximum away from the case.
2. The top face and Pin No. 1 are marked.

The metric dimensions are calculated from the original dimensions in inches.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - TO99 PACKAGE, 8-PIN





BOTTOM VIEW

SYMBOL	MILLIMETRES			DEGR. NOM.	NOTES
	MIN.	NOM.	MAX.		
Øa	-	5.08 (*)	-		1
A	4.20	-	4.69		
Øb2	0.407	-	0.508		
Øb3	-	-	0.53		
ØD	8.51	-	9.39		
ØD1	7.75	-	8.50		
F	-	-	1.27		
h	0.15	-	1.01		
j	0.712	-	0.863		
k	0.74	-	1.14		2
L	12.50	-	14.50		
L1	-	-	1.27		
L2	6.35	-	-		
L3	12.70	-	-		
ØM	3.56	-	4.06		
N	0.26	-	1.01		
α				45° (*)	1

NOTES

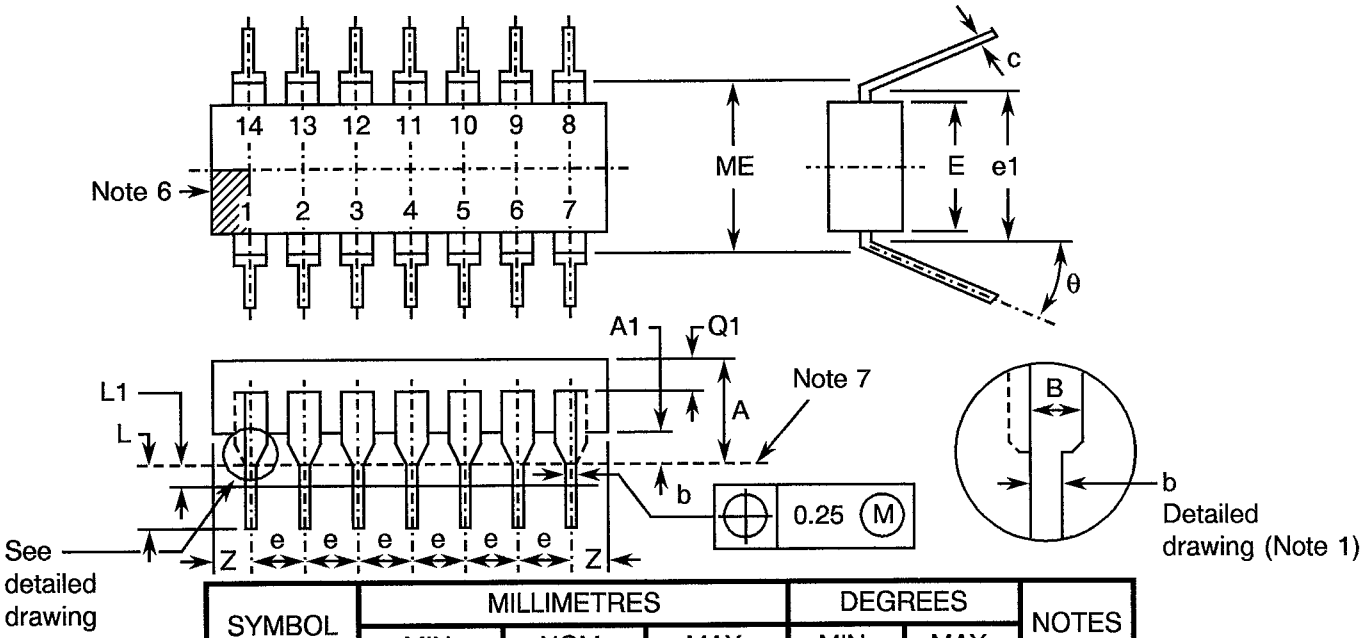
1. The section of each terminal, from a distance of 1.37mm to the reference plane, shall be located in a ring whose diameter is 0.99mm, centred on the accurate geometrical point defining the terminal axis.
2. Measured from the D diameter.
3. Reference plane.
4. Base plane.
5. Reference index of Pin 8.

* = accurate geometrical location.

The metric dimensions are calculated from the original dimensions in inches.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(c) - DUAL-IN-LINE PACKAGE, 14-PIN



SYMBOL	MILLIMETRES			DEGREES		NOTES
	MIN.	NOM.	MAX.	MIN.	MAX.	
A	-	-	5.08			
A1	0.51	-	-			
B	-	-	1.77			1
b	0.381	-	0.508			1
c	0.204	-	0.304			
E	-	6.3	-			
e	-	2.54 *	-			2
e1	-	7.62 *	-			3
L	2.5	-	3.9			(a)
L1	-	-	0.76			
ME	7.62	-	8.25			3
Q1	-	-	2.03			
Z						4
θ				0	15	
n =	7×2					5

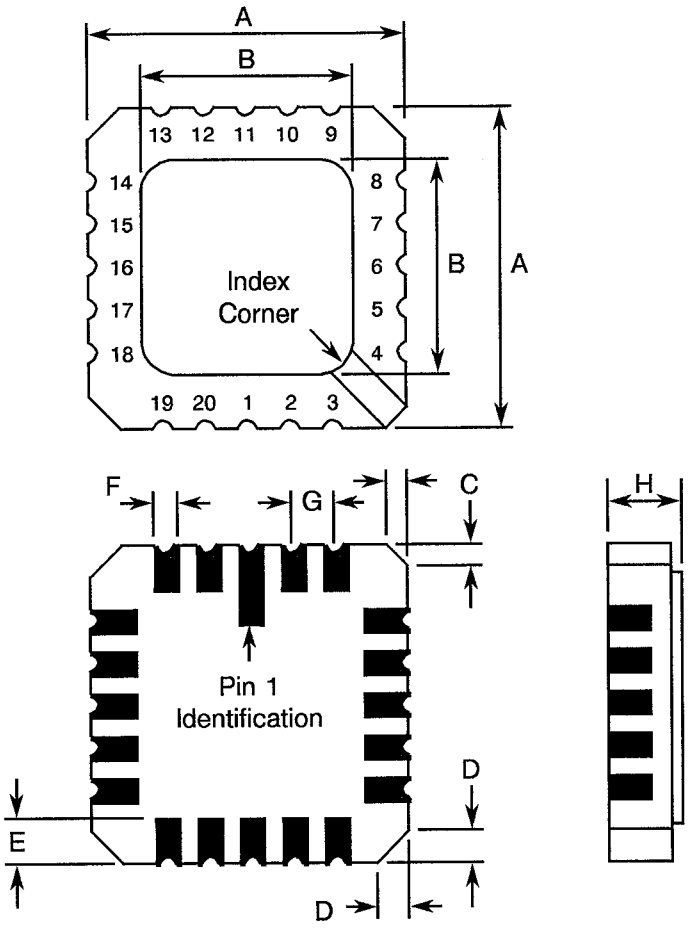
NOTES

1. The lead profile is not required for transition from B to b. The outline of the extreme outputs in the case of F.105A may differ from that of the others, as shown in the Figure.
2. The space between leads is measured on the area L1.
3. Measured when the value of the angle θ is zero.
4. Case F.105: Z between e/2 and e (1.27mm < Z < 2.54mm).
   Case F.105A: Z less than e/2 (Z < 1.27mm).
5. n = quantity of leads.
6. Area for visible reference mark on top face.
7. Base plane.
   * = accurate geometrical location.

(a) Recommended dimensions for the future: minimum 3.0mm.
maximum 3.9mm.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(d) - CHIP CARRIER PACKAGE, 20-TERMINAL



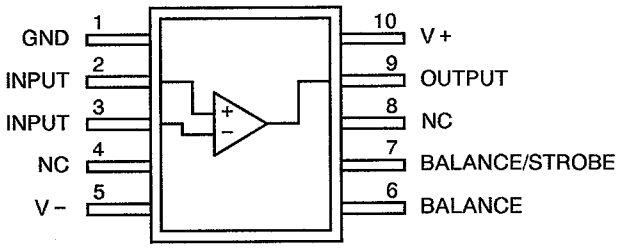
SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	8.69	9.09	-
B	7.80	9.09	-
C	0.25	0.51	4
D	0.89	1.14	5
E	1.14	1.40	2
F	0.56	0.71	2
G	1.27 TYPICAL		1, 3
H	1.63	2.54	-

NOTES

1. The true position pin or terminal spacing is 1.27mm between centrelines. Each pin or terminal centreline shall be located within ±0.13mm of its true longitudinal position relative to Pins 1 and the highest pin number.
2. All terminals.
3. 16 spaces.
4. Index corner only - 2 dimensions.
5. 3 non-index corners - 6 dimensions.

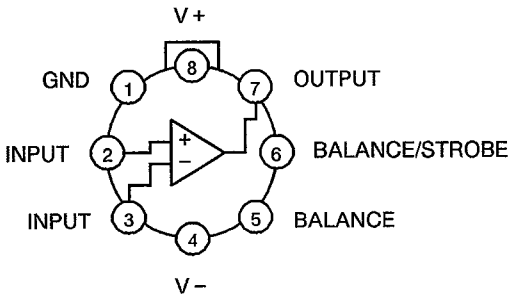
FIGURE 3(a) - PIN SCHEMATICS

FIGURE 3(a) i - FLAT PACKAGE



TOP VIEW

FIGURE 3(a) ii - TO99 PACKAGE



TOP VIEW

FIGURE 3(a) iii - CHIP CARRIER PACKAGE

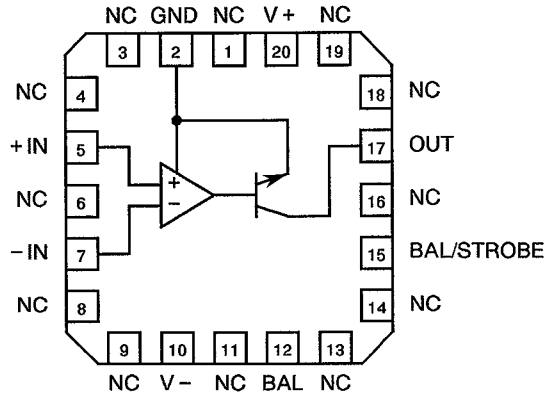


FIGURE 3(a) - PIN SCHEMATICS (CONTINUED)

FIGURE 3(a) iv - DUAL-IN-LINE PACKAGE

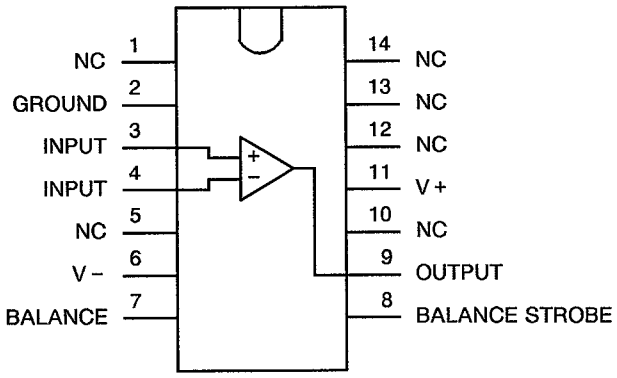
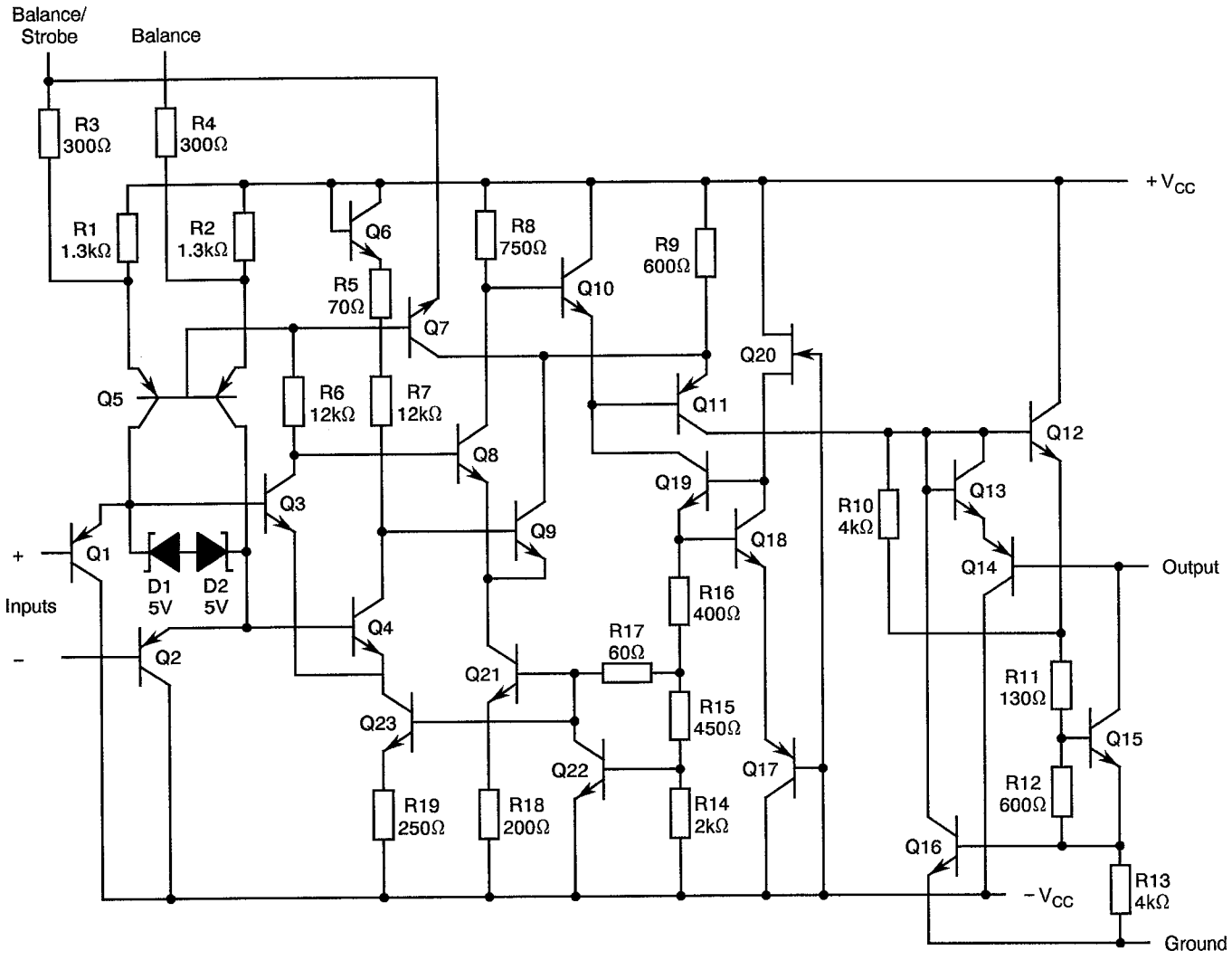


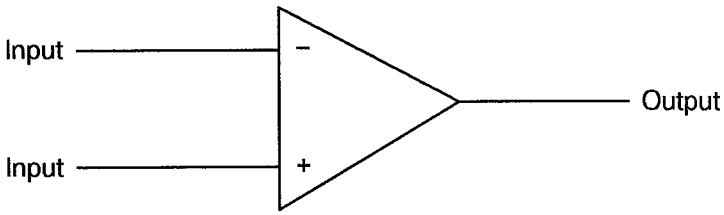
FIGURE 3(b) - CIRCUIT SCHEMATIC (FOR INFORMATION ONLY)



NOTES

1. All resistance values are nominal

FIGURE 3(c) - FUNCTIONAL DIAGRAM



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

I_{CC} = Supply Current.
I_{OS} = Output Short Circuit Current.
I_O = Output Leakage Current.
I_I = Input Leakage Current.
I_{STB} = Strobe Current.
V_{OSTB} = Collector Output Voltage (strobe).

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

The following deviations from ESA/SCC Generic Specification No. 9000 shall apply:-

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

Subpara. 7.1.1(a), "High Temperature Reverse Bias" test and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification, Environmental and Endurance Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be for:-

Variants 01 and 02: 0.35 grammes.
Variants 03, 04 and 07: 1.50 grammes.
Variants 05 and 06: 2.00 grammes.
Variant 08: 0.60 grammes.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed, preform-soldered or glass frit-sealed.

4.4.2 Lead Material and Finish

For flat, TO99 and dual-in-line packages, the lead material shall be Type 'D' with either Type '2', Type '3 or 4' or Type '9' finish in accordance with ESA/SCC Basic Specification No. 23500. For chip carrier packages, the finish shall be Type '2' in accordance with ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

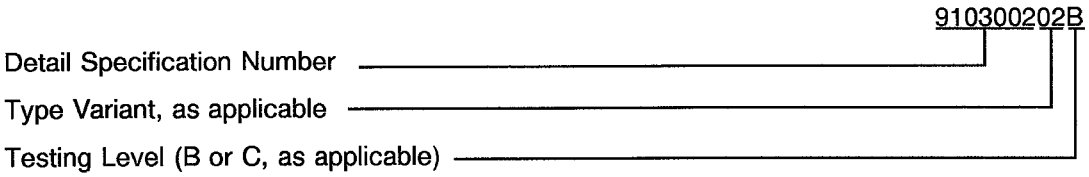
(c) Traceability Information.

4.5.2 Lead Identification

For flat and dual-in-line packages, an index shall be located at the top of the package as defined in Note 2 to Figure 2(a) and Note 6 to Figure 2(c) or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering shall be read with the index or tab on the left-hand side. For TO99 packages, a tab shall be used to identify Pin No. 8 as defined in Note 5 to Figure 2(b). For chip carrier packages, the index shall be as defined in Note 4 to Figure 2(d).

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with ESA/SCC Basic Specification No. 21700.

4.5.5 Marking of Small Components

When it is considered that the component is too small to accommodate the marking as specified above, as much as space permits shall be marked. The order of precedence shall be as follows:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

The marking information in full shall accompany each component in its primary package.

4.6 ELECTRICAL CHARACTERISTICS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Tables 3(a) and 3(b). The measurements shall be performed at $T_{amb} = +125$°C and -55°C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for Burn-in

The requirements for burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for burn-in shall be as specified in Table 5 of this specification.

4.7.3 Electrical Circuits for Burn-in

Circuits for use in performing the burn-in tests are shown in Figure 5 of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions	Limits		Unit
							Min	Max	
1	Input Offset Voltage	V_{IO1}	4001	4(a)	E_1	$V_{CC} = \pm 15V$, $V_{IC} = 0$ $R_S = 50\Omega$	-	2.0	mV
2		V_{IO2}			E_2	$V_{CC} = \pm 2.5V$, $V_{IC} = 0$ $R_S = 50\Omega$	-	2.0	
3		V_{IO3}			E_3	$V_{CC} = \pm 15V$, $V_{IC} = 0$ $R_S = 50\Omega$ $V_{BAL} = V_{BAL}/STB = +V_{CC}$	-	2.0	
4	Input Offset Current	I_{IO1}	4001	4(b)	E_4	$V_{CC} = \pm 15V$, $V_{IC} = 0$ $R_S = 100k\Omega$	-	10	nA
5		I_{IO2}			E_5	$V_{CC} = \pm 15V$, $V_{IC} = -14.5V$ $R_S = 100k\Omega$	-	10	
6		I_{IO3}			E_6	$V_{CC} = \pm 15V$, $V_{IC} = 0$ $R_S = 100k\Omega$ $V_{BAL} = V_{BAL}/STB = +V_{CC}$	-	10	
7	Input Bias Current	I_{IB1}	4001	4(c)	E_7	$V_{CC} = \pm 15V$ V_{IN} = Open $R_1 = 0$ $R_2 = 100k\Omega$	-	100	nA
					E_8	$V_{CC} = \pm 15V$ V_{IN} = Open $R_1 = 100k\Omega$ $R_2 = 0$			
8		I_{IB2}			E_9	$V_{CC} = \pm 15V$ $V_{IN} = -14.5V$ $R_1 = 0$ $R_2 = 100k\Omega$			
					E_{10}	$+V_{CC} = 29.5V$ $-V_{CC} = -0.5V$ $V_{IN} = -14.5V$ $R_1 = 100k\Omega$ $R_2 = 0$			
9	Collector Output Voltage (Strobed)	$V_{O(STB)}$	4001	4(d)	E_{11}	$V_{CC} = \pm 15V$ $V_{IN1} = 15V$ $V_{IN2} = 0V$ $I_{STB} = -3.0mA$	14	-	V
10	Output Leakage Current	I_O	4001	4(e)	I_O	$V_{CC} = \pm 18V$ $V_{OUT} = 32V$ $V_{ID} = 5.0mV$ $R_L = 5.0k\Omega$	-	10	A

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions	Limits		Unit
							Min	Max	
11	Input Leakage Current	I_I	-	4(f)	E_{12}	$V_{CC} = \pm 18V$ $V_{OUT} = 32V$ $V_{IN1} = +17V$ $V_{IN2} = -12V$	-	20	nA
12	Positive Supply Current	I_{CC1}	3005	4(g)	$+I_{CC}$	$V_{CC} = \pm 15V$	0.5	4.0	mA
13	Negative Supply Current	I_{CC2}	3005	4(g)	$-I_{CC}$	$V_{CC} = \pm 15V$	-4.0	-0.5	mA
14	Short Circuit Output Current	I_{OS}	3011	4(h)	E_{13}	$V_{CC} = \pm 15V$ $V_{OUT} = 5.0V$ $V_{IN1} = 125mV$ $V_{IN2} = 0$ Duration: 10ms	0	200	mA
15	Saturation Voltage	V_{OL1}	3007	4(i)	E_{14}	$+V_{CC} = 4.5V$ $-V_{CC} = 0$ $V_{IN1} = 0.506V$ $V_{IN2} = 0.5V$ $I_{OUT} = 8.0mA$	-	0.4	V
16		V_{OL2}				$V_{CC} = \pm 15V$ $V_{IN1} = -14V$ $V_{IN2} = -14.005V$ $I_{OUT} = 50mA$	-	1.5	
17	Differential Mode Voltage Gain (Collector Output)	A_{VD}	4004	4(j)	E_{16}	$V_{CC} = \pm 15V$ $V_{IN} = -30V$ $R_L = 1.0k\Omega$	80	-	V/mV
					E_{17}	$V_{CC} = \pm 15V$ $V_{IN} = +10V$ $R_L = 1.0k\Omega$			
18	Differential Mode Voltage Gain (Emitter Output)	A_{VD}	4004	4(k)	E_{18}	$V_{CC} = \pm 15V$ $V_{IN} = -10V$ $R_L = 600\Omega$	10	-	V/mV
					E_{19}	$V_{CC} = \pm 15V$ $V_{IN} = +10V$ $R_L = 600\Omega$			
19	Common Mode Rejection Ratio	CMRR	4003	4(l)	E_{20}	$+V_{CC} = 29.5V$ $-V_{CC} = -0.5V$ $V_{IN} = -14.5V$	80	-	dB
					E_{21}	$+V_{CC} = 2.0V$ $-V_{CC} = -28V$ $V_{IN} = 13V$			

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions	Limits		Unit
							Min	Max	
20	Response Time (Low to High) (Collector Output)	t_r	-	4(m)	-	$V_{CC} = \pm 15V$ $V_{OD} = -5.0mV$ $\Delta V_{IN} = 100mV$ Note 1	-	300	ns
21	Response Time (High to Low) (Collector Output)	t_f	-	4(m)	-	$V_{CC} = \pm 15V$ $V_{OD} = 5.0mV$ $\Delta V_{IN} = 100mV$ Note 1	-	300	ns

NOTES

1. Sample test Inspection Level II, AQL = 2.5%.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0−5) °C

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions	Limits		Unit
							Min	Max	
1	Input Offset Voltage	V_{IO1}	4001	4(a)	E_1	$V_{CC} = \pm 15V$, $V_{IC} = 0$ $R_S = 50\Omega$	-	3.0	mV
2		V_{IO2}			E_2	$V_{CC} = \pm 2.5V$, $V_{IC} = 0$ $R_S = 50\Omega$	-	3.0	
3		V_{IO3}			E_3	$V_{CC} = \pm 15V$, $V_{IC} = 0$ $R_S = 50\Omega$ $V_{BAL} = V_{BAL}/STB = +V_{CC}$	-	3.0	
4	Input Offset Current	I_{IO1}	4001	4(b)	E_4	$V_{CC} = \pm 15V$, $V_{IC} = 0$ $R_S = 100k\Omega$	-	15	nA
5		I_{IO2}			E_5	$V_{CC} = \pm 15V$, $V_{IC} = -14.5V$ $R_S = 100k\Omega$	-	15	
6		I_{IO3}			E_6	$V_{CC} = \pm 15V$, $V_{IC} = 0$ $R_S = 100k\Omega$ $V_{BAL} = V_{BAL}/STB = +V_{CC}$	-	15	
7	Input Bias Current	I_{IB1}	4001	4(c)	E_7	$V_{CC} = \pm 15V$ V_{IN} = Open $R_1 = 0$ $R_2 = 100k\Omega$	-	125	nA
					E_8	$V_{CC} = \pm 15V$ V_{IN} = Open $R_1 = 100k\Omega$ $R_2 = 0$			
8		I_{IB2}			E_9	$V_{CC} = \pm 15V$ $V_{IN} = -14.5V$ $R_1 = 0$ $R_2 = 100k\Omega$			
					E_{10}	$+V_{CC} = 29.5V$ $-V_{CC} = -0.5V$ $V_{IN} = -14.5V$ $R_1 = 100k\Omega$ $R_2 = 0$			
9	Collector Output Voltage (Strobed)	$V_{O(STB)}$	4001	4(d)	E_{11}	$V_{CC} = \pm 15V$ $V_{IN1} = 15V$ $V_{IN2} = 0V$ $I_{STB} = -3.0mA$	14	-	V
10	Output Leakage Current	I_O	4001	4(e)	I_O	$V_{CC} = \pm 18V$ $V_{OUT} = 32V$ $V_{ID} = 5.0mV$ $R_L = 5.0k\Omega$	-	500	nA

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0-5) °C (CONT'D)

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions	Limits		Unit
							Min	Max	
11	Input Leakage Current	I_I	-	4(f)	E_{12}	$V_{CC} = \pm 18V$ $V_{OUT} = 32V$ $V_{IN1} = +17V$ $V_{IN2} = -12V$	-	20	nA
12	Positive Supply Current	I_{CC1}	3005	4(g)	$+I_{CC}$	$V_{CC} = \pm 15V$	0	25	mA
13	Negative Supply Current	I_{CC2}	3005	4(g)	$-I_{CC}$	$V_{CC} = \pm 15V$	-3.0	0	mA
14	Short Circuit Output Current	I_{OS}	3011	4(h)	E_{13}	$V_{CC} = \pm 15V$ $V_{OUT} = 5.0V$ $V_{IN1} = 125mV$ $V_{IN2} = 0$ Duration: 10ms	0	150	mA
15	Saturation Voltage	V_{OL1}	3007	4(i)	E_{14}	$+V_{CC} = 4.5V$ $-V_{CC} = 0$ $V_{IN1} = 0.506V$ $V_{IN2} = 0.5V$ $I_{OUT} = 8.0mA$	-	0.4	V
16		V_{OL2}			E_{15}	$V_{CC} = \pm 15V$ $V_{IN1} = -14V$ $V_{IN2} = -14.005V$ $I_{OUT} = 50mA$	-	1.5	
17	Differential Mode Voltage Gain (Collector Output)	A_{VD}	4004	4(j)	E_{16}	$V_{CC} = \pm 15V$ $V_{IN} = -30V$ $R_L = 1.0k\Omega$	35	-	V/mV
					E_{17}	$V_{CC} = \pm 15V$ $V_{IN} = +10V$ $R_L = 1.0k\Omega$			
18	Differential Mode Voltage Gain (Emitter Output)	A_{VD}	4004	4(k)	E_{18}	$V_{CC} = \pm 15V$ $V_{IN} = -10V$ $R_L = 600\Omega$	8.0	-	V/mV
					E_{19}	$V_{CC} = \pm 15V$ $V_{IN} = +10V$ $R_L = 600\Omega$			
19	Common Mode Rejection Ratio	CMRR	-	4(l)	E_{20}	$+V_{CC} = 29.5V$ $-V_{CC} = -0.5V$ $V_{IN} = -14.5V$	80	-	dB
					E_{21}	$+V_{CC} = 2.0V$ $-V_{CC} = -28V$ $V_{IN} = 13V$			

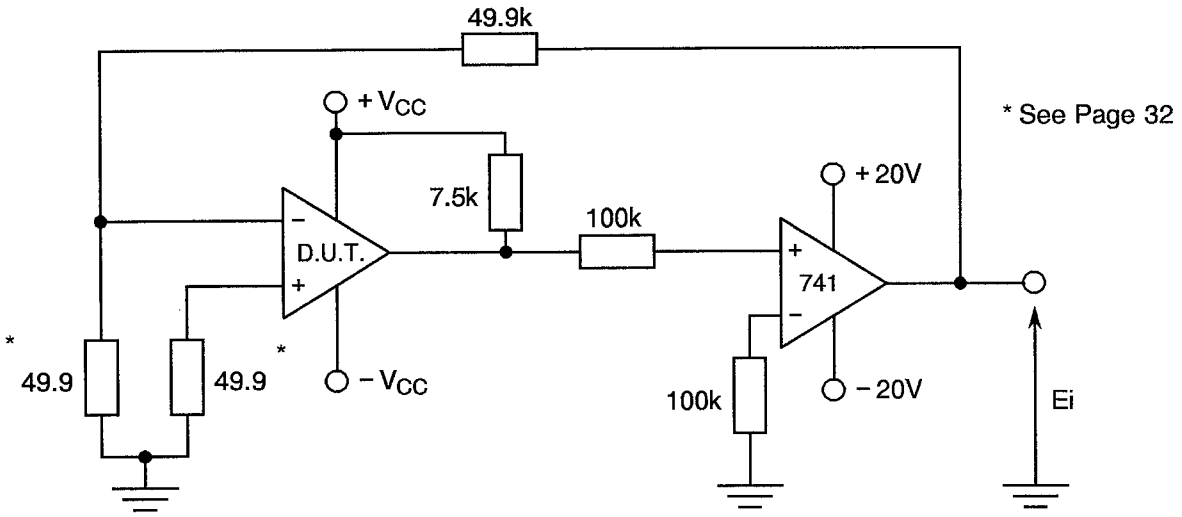
TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, −55(+5−0) °C

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions	Limits		Unit
							Min	Max	
1	Input Offset Voltage	V_{IO1}	4001	4(a)	E_1	$V_{CC} = \pm 15V$, $V_{IC} = 0$ $R_S = 50\Omega$	-	3.0	mV
2		V_{IO2}			E_2	$V_{CC} = \pm 2.5V$, $V_{IC} = 0$ $R_S = 50\Omega$	-	3.0	
3		V_{IO3}			E_3	$V_{CC} = \pm 15V$, $V_{IC} = 0$ $R_S = 50\Omega$ $V_{BAL} = V_{BAL}/STB = +V_{CC}$	-	3.0	
4	Input Offset Current	I_{IO1}	4001	4(b)	E_4	$V_{CC} = \pm 15V$, $V_{IC} = 0$ $R_S = 100k\Omega$	-	15	nA
5		I_{IO2}			E_5	$V_{CC} = \pm 15V$, $V_{IC} = -14.5V$ $R_S = 100k\Omega$	-	15	
6		I_{IO3}			E_6	$V_{CC} = \pm 15V$, $V_{IC} = 0$ $R_S = 100k\Omega$ $V_{BAL} = V_{BAL}/STB = +V_{CC}$	-	15	
7	Input Bias Current	I_{IB1}	4001	4(c)	E_7	$V_{CC} = \pm 15V$ $V_{IN} = Open$ $R_1 = 0$ $R_2 = 100k\Omega$	-	125	nA
					E_8	$V_{CC} = \pm 15V$ $V_{IN} = Open$ $R_1 = 100k\Omega$ $R_2 = 0$			
8		I_{IB2}			E_9	$V_{CC} = \pm 15V$ $V_{IN} = -14.5V$ $R_1 = 0$ $R_2 = 100k\Omega$			
					E_{10}	$+V_{CC} = 29.5V$ $-V_{CC} = -0.5V$ $V_{IN} = -14.5V$ $R_1 = 100k\Omega$ $R_2 = 0$			
9	Collector Output Voltage (Strobed)	$V_{O(STB)}$	4001	4(d)	E_{11}	$V_{CC} = \pm 15V$ $V_{IN1} = 15V$ $V_{IN2} = 0V$ $I_{STB} = -2.0mA$	14	-	V

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, −55(+5−0) °C (CONT'D)

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions	Limits		Unit
							Min	Max	
11	Input Leakage Current	I_I	-	4(f)	E_{12}	$V_{CC} = \pm 18V$ $V_{OUT} = 32V$ $V_{IN1} = +17V$ $V_{IN2} = -12V$	-	20	nA
12	Positive Supply Current	I_{CC1}	3005	4(g)	$+I_{CC}$	$V_{CC} = \pm 15V$	0.5	6.0	mA
13	Negative Supply Current	I_{CC2}	3005	4(g)	$-I_{CC}$	$V_{CC} = \pm 15V$	−5.0	−0.5	mA
14	Short Circuit Output Current	I_{OS}	3011	4(h)	E_{13}	$V_{CC} = \pm 15V$ $V_{OUT} = 5.0V$ $V_{IN1} = 125mV$ $V_{IN2} = 0$ Duration: 10ms	0	250	mA
15	Saturation Voltage	V_{OL1}	3007	4(i)	E_{14}	$+V_{CC} = 4.5V$ $-V_{CC} = 0$ $V_{IN1} = 0.506V$ $V_{IN2} = 0.5V$ $I_{OUT} = 8.0mA$	-	0.4	V
16		V_{OL2}			E_{15}	$V_{CC} = \pm 15V$ $V_{IN1} = -14V$ $V_{IN2} = -14.005V$ $I_{OUT} = 50mA$	-	1.5	
17	Differential Mode Voltage Gain (Collector Output)	A_{VD}	4004	4(j)	E_{16}	$V_{CC} = \pm 15V$ $V_{IN} = -30V$ $R_L = 1.0k\Omega$	35	-	V/mV
					E_{17}	$V_{CC} = \pm 15V$ $V_{IN} = +10V$ $R_L = 1.0k\Omega$			
18	Differential Mode Voltage Gain (Emitter Output)	A_{VD}	4004	4(k)	E_{18}	$V_{CC} = \pm 15V$ $V_{IN} = -10V$ $R_L = 600\Omega$	8.0	-	V/mV
					E_{19}	$V_{CC} = \pm 15V$ $V_{IN} = +10V$ $R_L = 600\Omega$			
19	Common Mode Rejection Ratio	CMRR	-	4(l)	E_{20}	$+V_{CC} = 29.5V$ $-V_{CC} = -0.5V$ $V_{IN} = -14.5V$	80	-	dB
					E_{21}	$+V_{CC} = 2.0V$ $-V_{CC} = -28V$ $V_{IN} = 13V$			

FIGURE 4(a) - INPUT OFFSET VOLTAGE

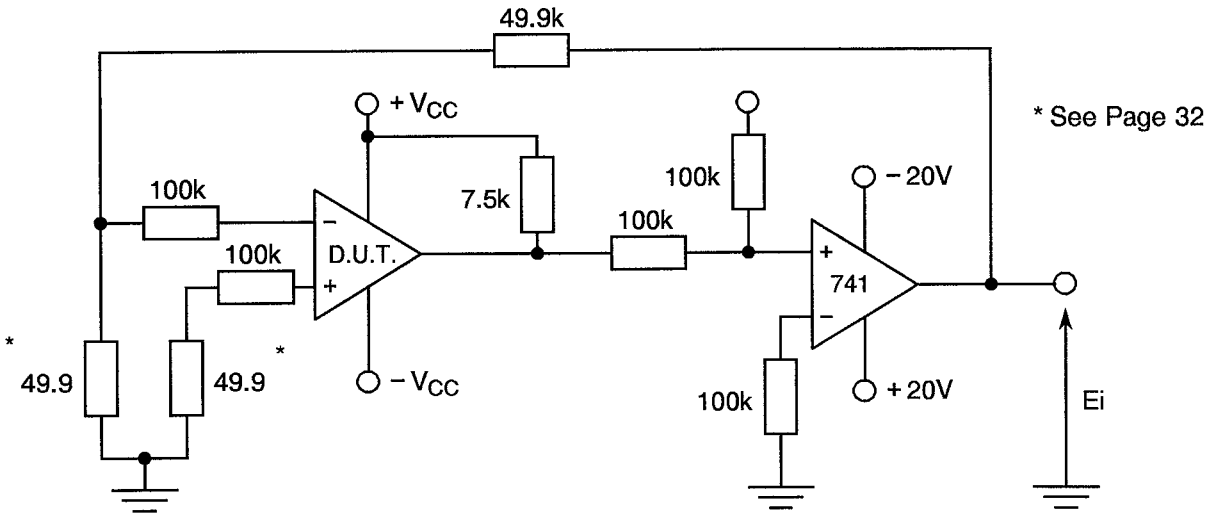


* See Page 32

NOTES

1. $V_{IO1} = E_1$; $V_{IO2} = E_2$; $V_{IO3} = E_3$.
2. For measurement of V_{IO1}, V_{IO2}, balance and balance strobe inputs open. For V_{IO3}, balance and balance strobe are connected to $+V_{CC}$.
3. For all tests: ground terminal is connected to $-V_{CC}$ through a 300Ω resistor.

FIGURE 4(b) - INPUT OFFSET CURRENT

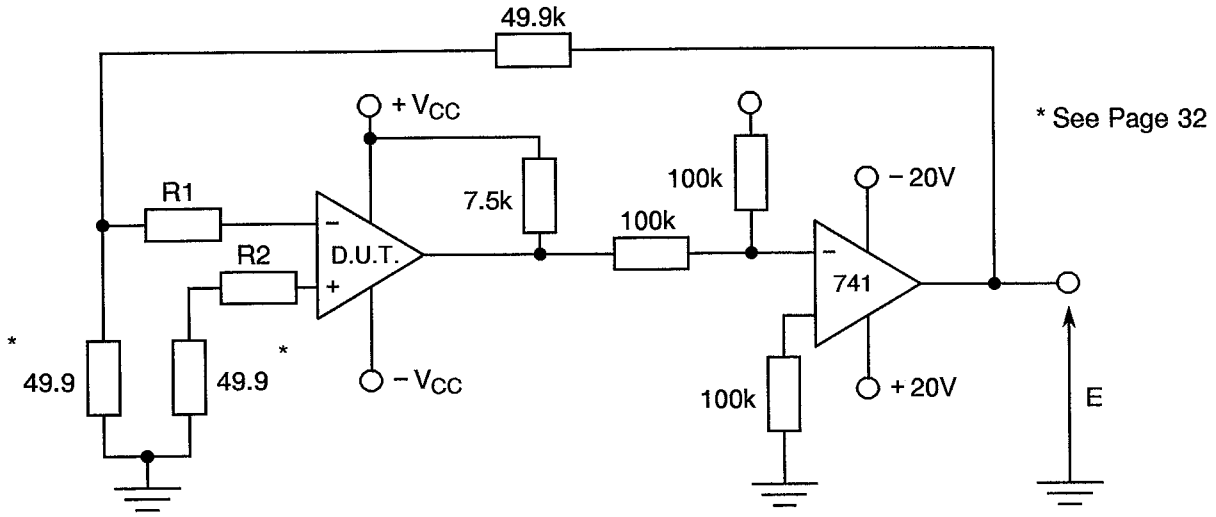


* See Page 32

NOTES

1. $I_{IO1} = (E_1 - E_4)/100$; $I_{IO2} = (E_1 - E_5)/100$; $I_{IO3} = (E_3 - E_6)/100$.
2. For I_{IO1} and I_{IO2}: balance and balance strobe inputs open. For I_{IO3}, balance and balance strobe are connected to $+V_{CC}$.
3. For all tests: ground terminal is connected to $-V_{CC}$ through a 300Ω resistor.

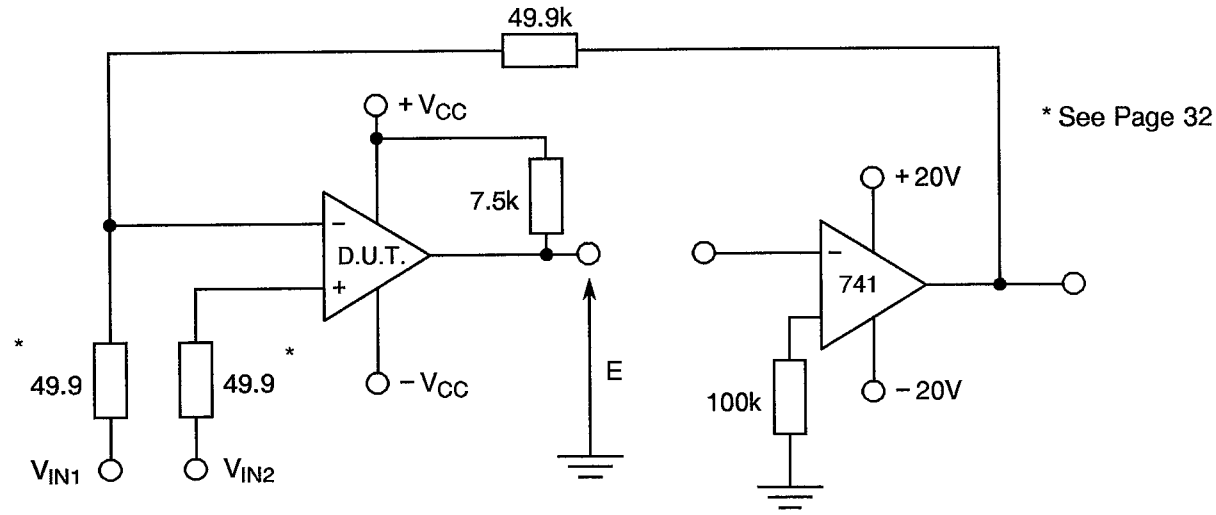
FIGURE 4(c) - INPUT BIAS CURRENT



NOTES

1. $I_{IB1} = (E_7 - E_8)/200$; $I_{IB2} = (E_9 - E_{10})/200$.
2. For both measurements: balance and balance strobe inputs open.
3. For both tests: ground is connected to $-V_{CC}$ through a 300Ω resistor.

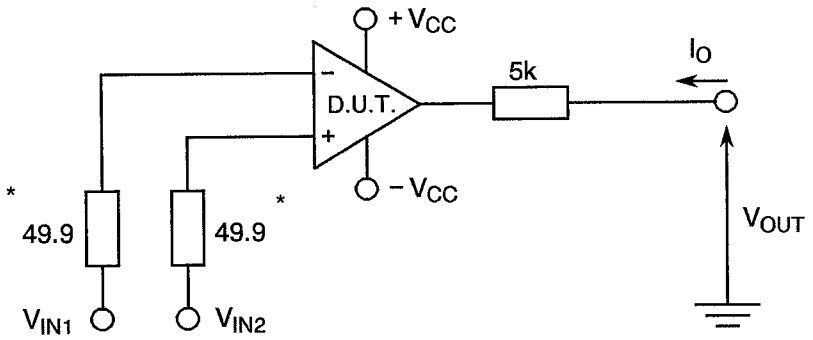
FIGURE 4(d) - COLLECTOR OUTPUT VOLTAGE (STROBED)



NOTES

1. Balance input is connected to $+V_{CC}$.
2. Balance strobe is connected to ground.
3. Ground terminal is connected to $-V_{CC}$ through a 600Ω resistor.

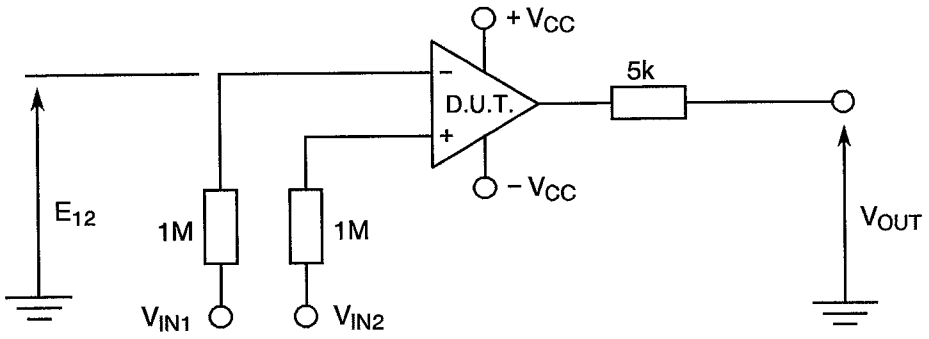
FIGURE 4(e) - OUTPUT LEAKAGE CURRENT



* See Page 32

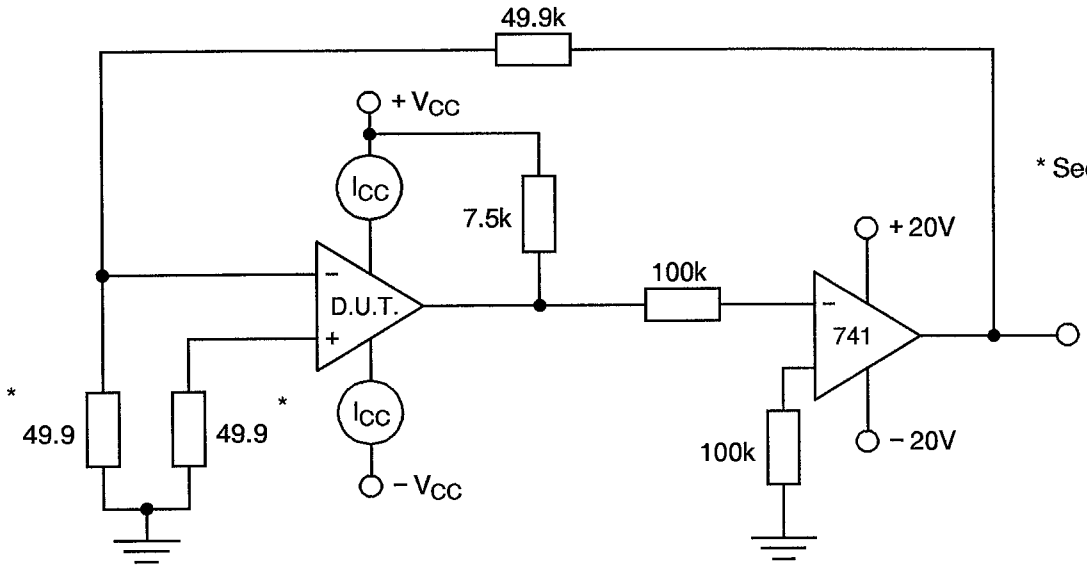
NOTES
1. Balance and balance strobe connected to ground via an ammeter (I = −5.0mA).
2. Ground terminal connected to ground.

FIGURE 4(f) - INPUT LEAKAGE CURRENT



NOTES
1. $I_I = E_{12}$.
2. Balance and balance strobe connected to ground via an ammeter (I = −5.0mA).
3. Ground terminal connected to ground.

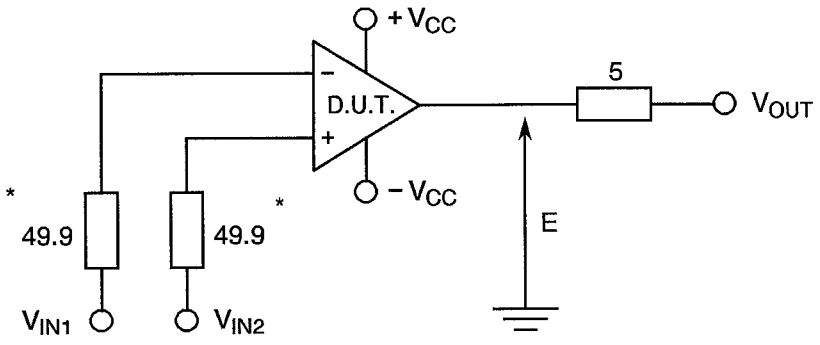
FIGURE 4(g) - SUPPLY CURRENT



* See Page 32

NOTES
1. Balance and balance strobe inputs open.
2. Ground terminal connected to $-V_{CC}$ through a 300Ω resistor.

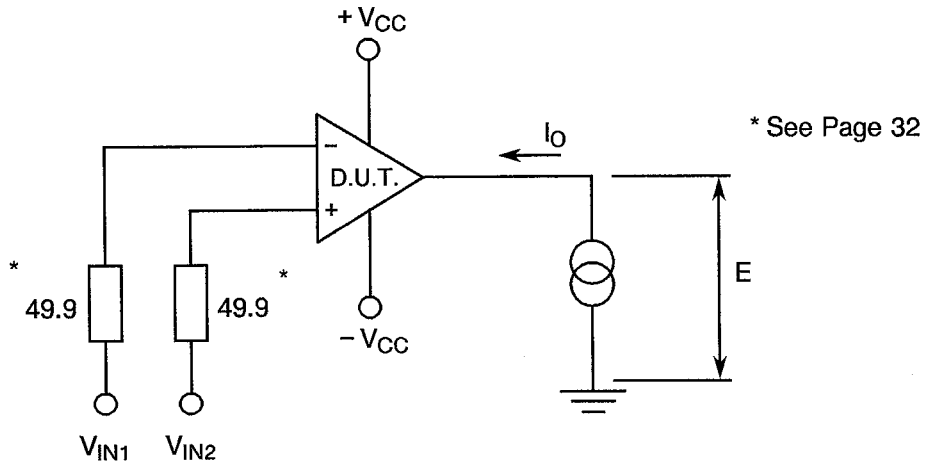
FIGURE 4(h) - SHORT CIRCUIT OUTPUT CURRENT



* See Page 32

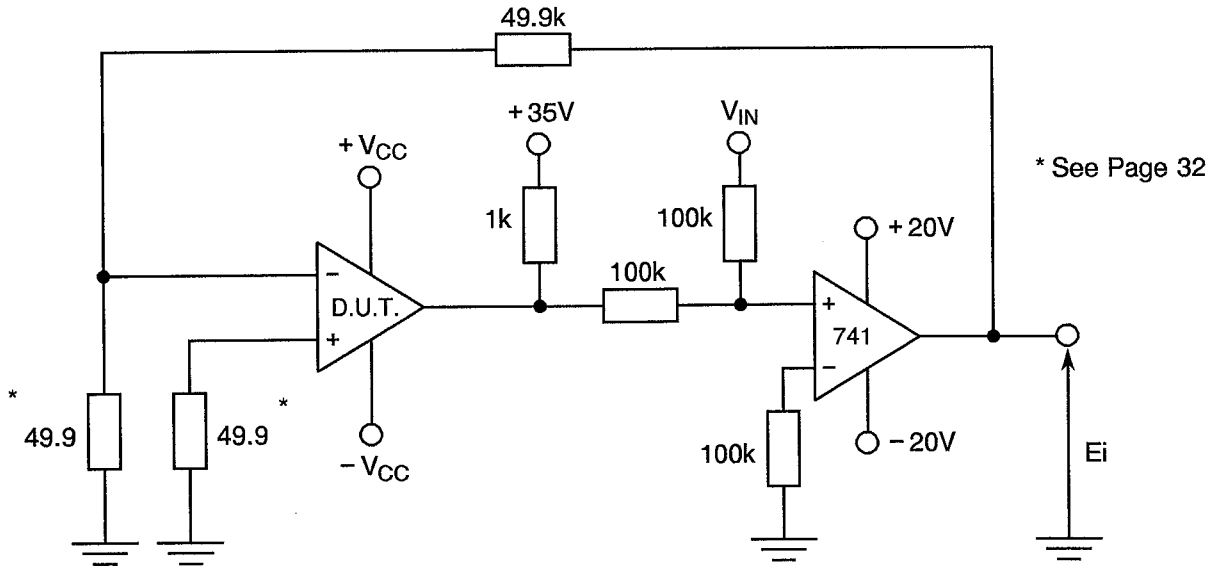
NOTES
1. $I_{OS} = (5000 - E)/5$.
2. Duration of test: 10ms maximum.
3. Balance and balance strobe inputs open.
4. Ground terminal connected to ground.

FIGURE 4(i) - SATURATION VOLTAGE



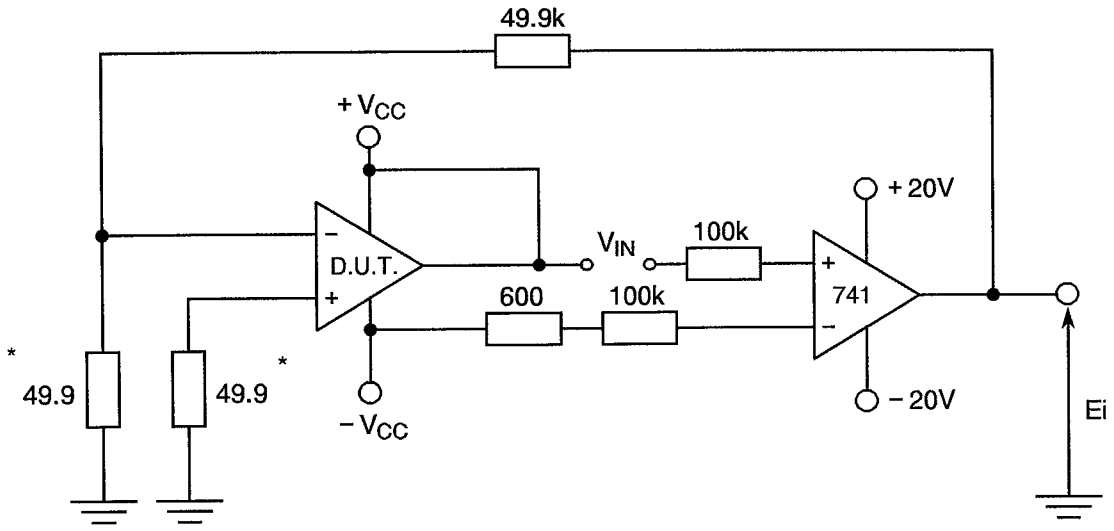
NOTES
1. $V_{OL} = E$.
2. Balance and balance strobe open.
3. Ground terminal connected to $-V_{CC}$.

FIGURE 4(j) - DIFFERENTIAL MODE VOLTAGE GAIN (COLLECTOR OUTPUT)



NOTES
1. $A_{VD} = 40000/E_{16} - E_{17}$.
2. Balance and balance strobe open.
3. Ground terminal connected to $-V_{CC}$.

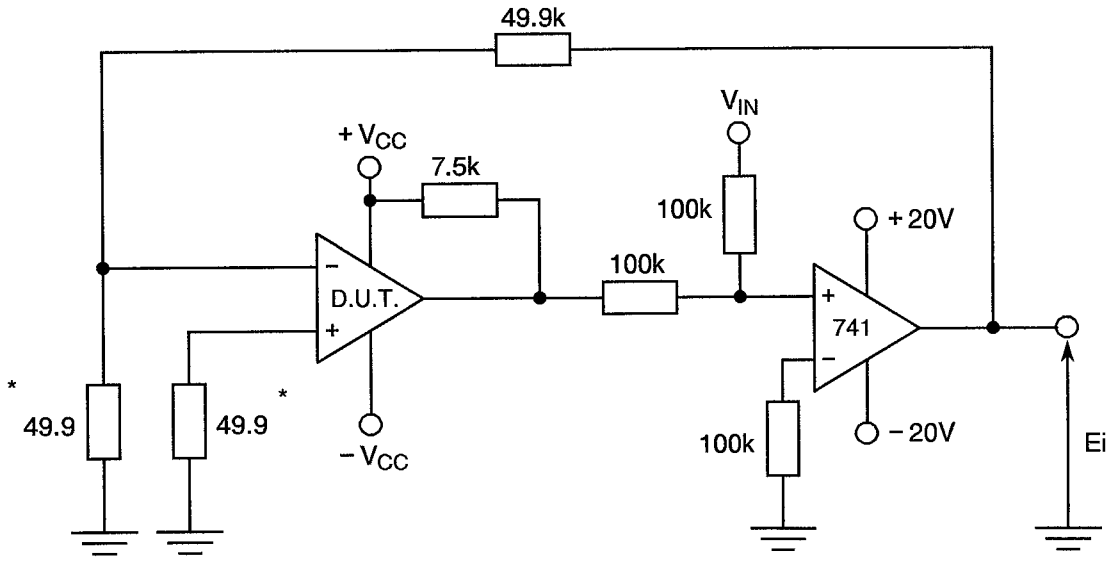
FIGURE 4(k) - DIFFERENTIAL MODE VOLTAGE GAIN (EMITTER OUTPUT)



NOTES

1. $A_{VD} = 20000/E_{18} - E_{19}$.
2. Balance and balance strobe open.
3. Ground terminal connected to $-V_{CC}$ through the 600Ω resistor.

FIGURE 4(l) - COMMON MODE REJECTION RATIO

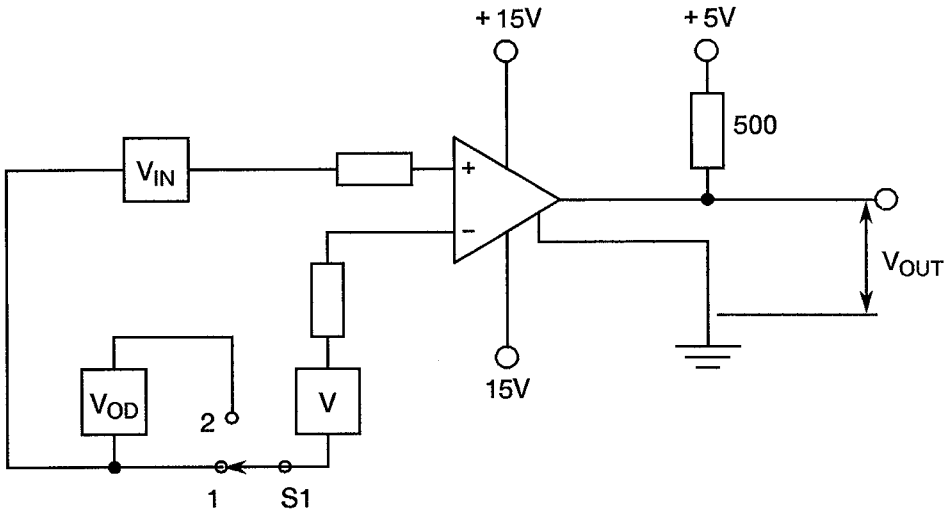


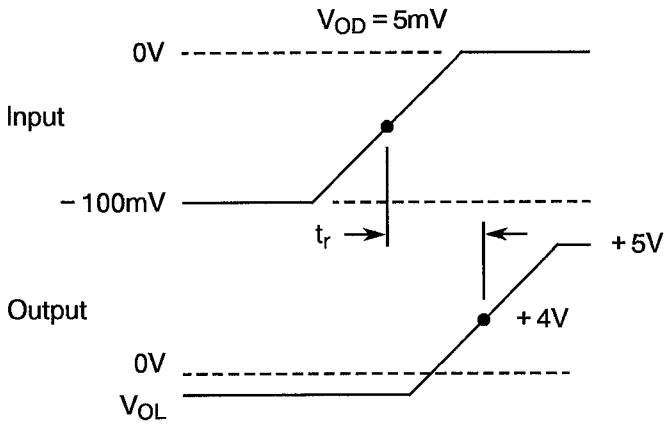
NOTES

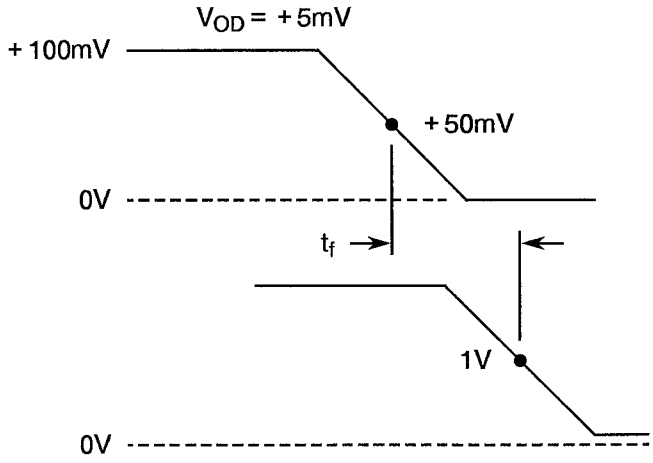
1. CMRR = 20 log $\left| \frac{27.5 \times 10^6}{E_{20} - E_{21}} \right|$ (measure E_{20} and E_{21} to four place accuracy).
2. Balance and balance strobe open.
3. Ground terminal connected to $-V_{CC}$ through the 300Ω resistor.

* These are 0.1% resistors matched to 0.01%. The tolerance for all other resistors is 1.0%.

FIGURE 4(m) - RESPONSE TIME







NOTES

1. V_{IN} = 10µs pulse width at 50kHz, t_{LH} and $t_{HL} \leq$ 10ns.
2. Set-up procedure:-
   A. With S1 in position 1, adjust V for V_{OUT} = 0.
   B. Adjust V_{OD} to −5mV for t_r or +5mV for t_f.
   C. Switch S1 to position 2.

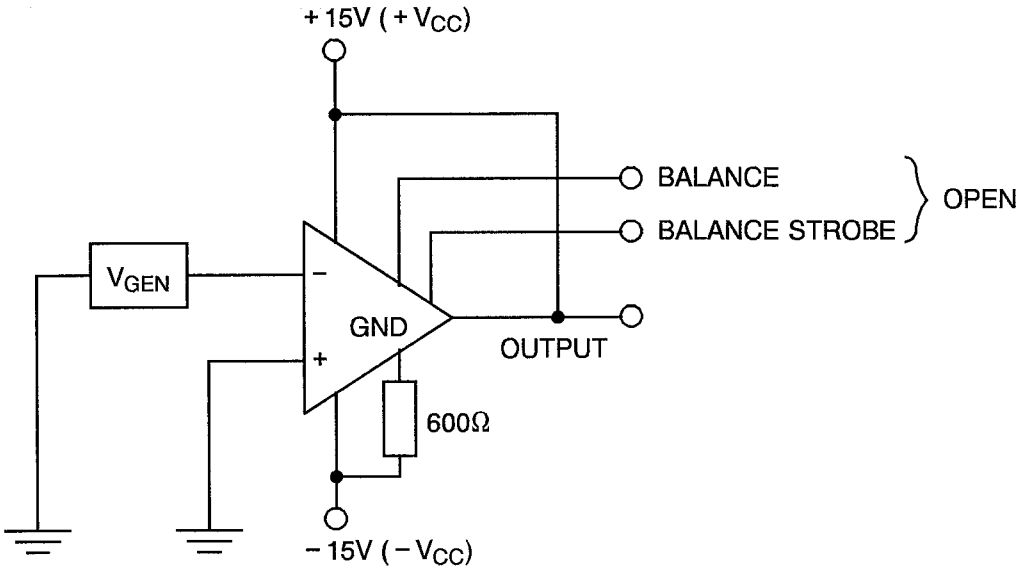
TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
1	Input Offset Voltage Change	V_{IO}	As per Table 2	As per Table 2	± 0.5	mV
4	Input Offset Current Change	I_{IO}	As per Table 2	As per Table 2	± 1.5	nA
7	Input Bias Current Change	I_{IB}	As per Table 2	As per Table 2	± 25	nA

TABLE 5 - CONDITIONS FOR BURN-IN

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+ 125 ± 5	°C
2	Supply Voltage	V_{CC}	± 15	V

FIGURE 5 - ELECTRICAL CIRCUIT FOR BURN-IN AND OPERATING LIFE



NOTES

1. V_{GEN} : square wave V = ± 8V, f = 5kHz.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5 of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The conditions for high temperature storage shall be $T_{amb} = +150 \pm 5$ °C.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

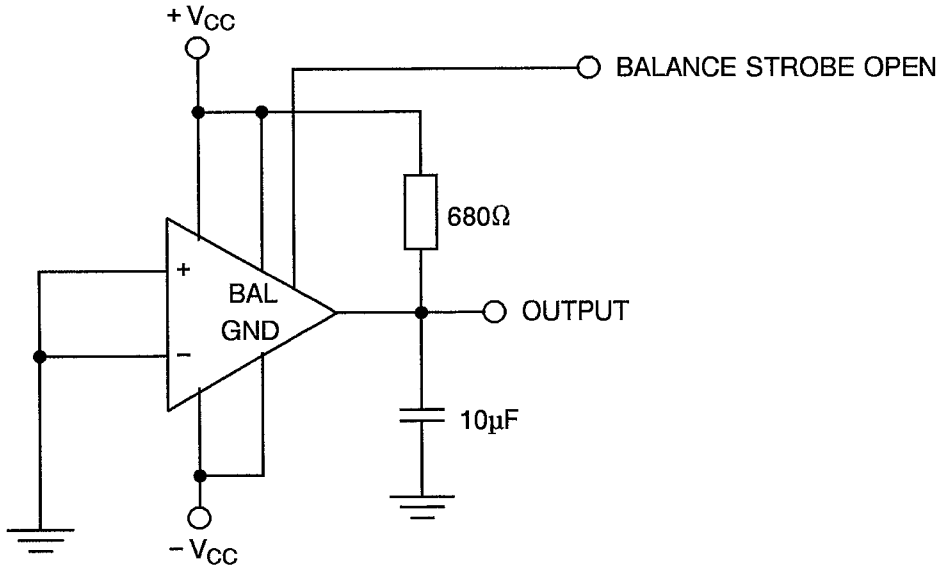
No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
1	Input Offset Voltage	V_{IO}	As per Table 2	As per Table 2	-	2.0	mV
4	Input Offset Current	I_{IO}	As per Table 2	As per Table 2	-	10	nA
7	Input Bias Current	I_{IB}	As per Table 2	As per Table 2	-	100	nA
12	Positive Supply Current	I_{CC1}	As per Table 2	As per Table 2	0.5	4.0	mA
13	Negative Supply Current	I_{CC2}	As per Table 2	As per Table 2	−4.0	−0.5	mA
17	Differential Mode Voltage Gain (Collector Output)	A_{VD}	As per Table 2	As per Table 2	80	-	V/mV

APPENDIX 'A'

AGREED DEVIATIONS FOR THOMSON-CSF (F)

It has been agreed for this Manufacturer that an alternative electrical circuit for burn-in and operating life (Figure 5) may be applied.

The alternative Figure 5 is as shown below.



APPENDIX 'A'

AGREED DEVIATIONS FOR THOMSON-CSF (F)

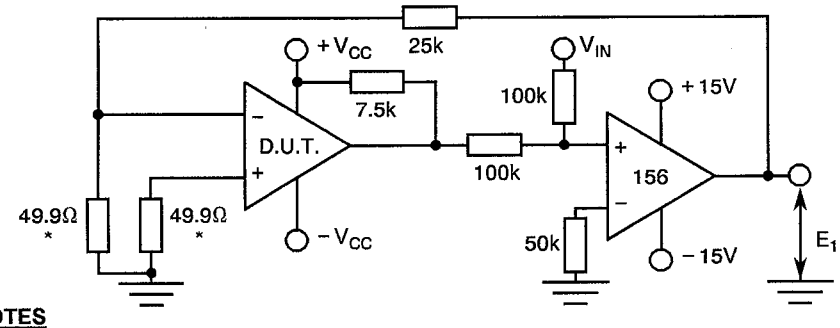
ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Tables 2, 3(a) and 3(b)	The measurements listed may be performed with test conditions amended as follows:- Test Nos. 1, 2, 3, 4 and 6: $V_{IC} = V_{IN} = 0V$. Test No. 5: $+V_{CC} = 29.5V$, $-V_{CC} = -0.5V$, $V_{IC} = V_{IN} = -14.5V$. Test No. 7: $V_{IN} = 0V$. Test No. 8: $+V_{CC} = 29.5V$, $-V_{CC} = -0.5V$ for E_9 measured value. Test No. 10: $+V_{CC} = -14V$, $-V_{CC} = -50V$, $V_{OUT} = 0V$. (Not in Table 3(b)): $V_{IN1} = V_{IN2} = -32V$, $V_e = -29.5V$, $R_L = 5.0k\Omega$, $V_{GND} = -32V$. Test No. 11: $+V_{CC} = 1.0V$, $-V_{CC} = -35V$, V_{OUT} = Open, $V_{IN1} = 0V$, $V_{IN2} = -29V$, $V_{GND} = -17V$. Test Nos. 12 and 13: $V_{IN} = 0V$. Test No. 15 $+V_{CC} = 4.0V$, $-V_{CC} = -0.5V$, $V_{IN1} = V_{IN2} = 0V$, $V_{GND} = -0.5V$, $V_e = 3.0V$, $I_{OUT} = 8.0mA$. Test No. 16: $+V_{CC} = 29V$, $-V_{CC} = -1.0V$, $V_{IN1} = V_{IN2} = 0V$, $V_{GND} = -1.0V$, $V_e = 2.5V$, $I_{OUT} = 50mA$.
Figure 4	The figures defined on the following sheets may be used for the Table 2, 3(a) and 3(b) electrical testing. The figure numbers correspond to those defined in the test tables.

APPENDIX 'A'

AGREED DEVIATIONS FOR THOMSON-CSF (F)

CIRCUITS FOR ELECTRICAL MEASUREMENTS

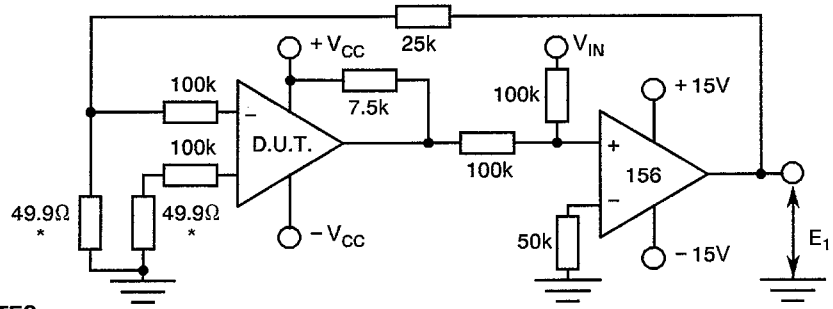
FIGURE 4(a) - INPUT OFFSET VOLTAGE



NOTES

1. $V_{IO1} = E_1/500$, $V_{IO2} = E_2/500$, $V_{IO3} = E_3/500$.
2. For measurement of V_{IO1}, V_{IO2}, balance and balance strobe inputs open. For V_{IO3}, balance and balance strobe are connected to $+V_{CC}$.
3. For all tests, ground terminal is connected to $-V_{CC}$ through a 300Ω resistor.

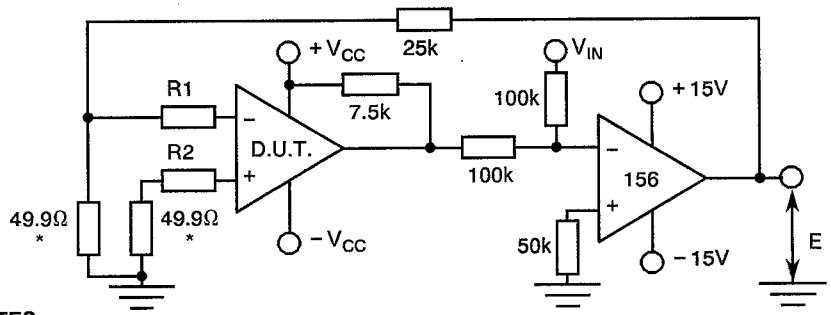
FIGURE 4(b) - INPUT OFFSET CURRENT



NOTES

1. $I_{IO1} = (E_1 - E_4)/5 \times 10^7$, $I_{IO2} = (E_1 - E_5)/5 \times 10^7$, $I_{IO3} = (E_3 - E_6)/5 \times 10^7$,
2. For I_{IO1} and I_{IO2}, balance and balance strobe inputs open; for I_{IO3}, balance and balance strobe are connected to $+V_{CC}$.
3. For both tests, ground terminal is connected to $-V_{CC}$ through a 300Ω resistor.

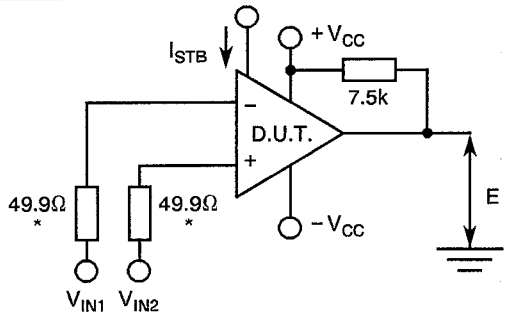
FIGURE 4(c) - INPUT BIAS CURRENT



NOTES

1. $I_{IB1+} = (E_1 - E_7)/5 \times 10^7$, $I_{IB1-} = (E_1 - E_8)/5 \times 10^7$.
   $I_{IB2+} = (E_1 - E_9)/5 \times 10^7$, $I_{IB2-} = (E_1 - E_{10})/5 \times 10^7$.
   $E_1 = 500\ V_{IO}$ ($V_{CM} = 14.5V$).
2. For both measurements, balance and strobe inputs open.
3. For both tests, ground is connected to $-V_{CC}$ through a 300Ω resistor.

FIGURE 4(d) - COLLECTOR OUTPUT UNIT VOLTAGE (STROBED)



NOTES

1. Balance input is connected to $+V_{CC}$.
2. Balance strobe is connected to ground.
3. Ground terminal is connected to $-V_{CC}$ through a 600Ω resistor.

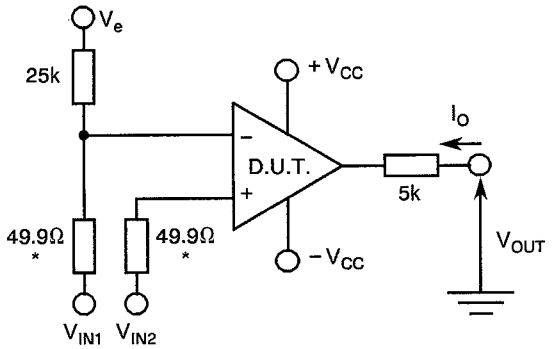
* See Page 42.

APPENDIX 'A'

AGREED DEVIATIONS FOR THOMSON-CSF (F)

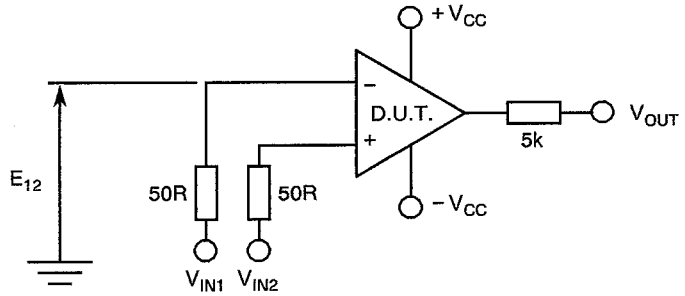
CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(e) - OUTPUT LEAKAGE CURRENT



NOTES
1. Balance and balance strobe connected to ground via an ammeter (I = −5.0mA).
2. Ground terminal connected to ground.

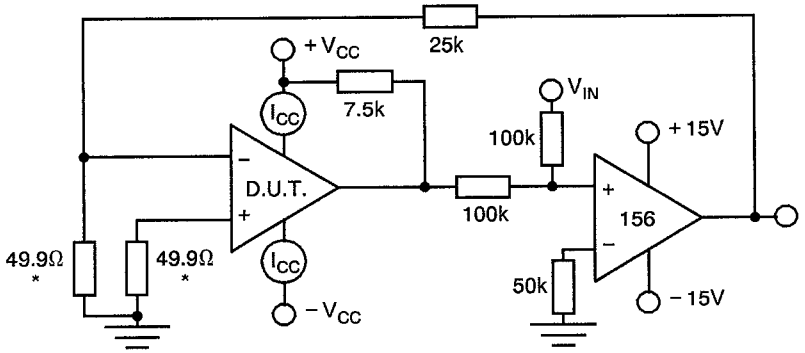
FIGURE 4(f) - INPUT LEAKAGE CURRENT



NOTES
1. $I_I = E_{12}$.
2. Balance and balance strobe connected to ground via an ammeter (I = −5.0mA).
3. Ground terminal connected to ground.

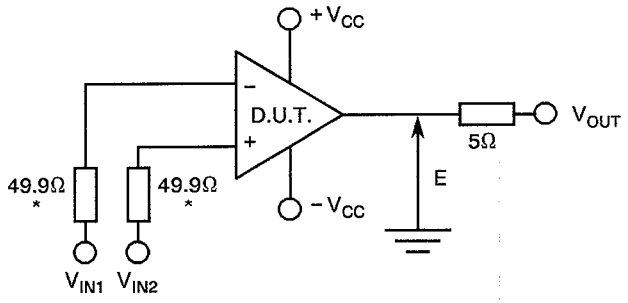
* See Page 42.

FIGURE 4(g) - SUPPLY CURRENT



NOTES
1. Balance and balance strobe inputs open.
2. Ground terminal is connected to $-V_{CC}$ through a 300Ω resistor.

FIGURE 4(h) - SHORT CIRCUIT OUTPUT CURRENT



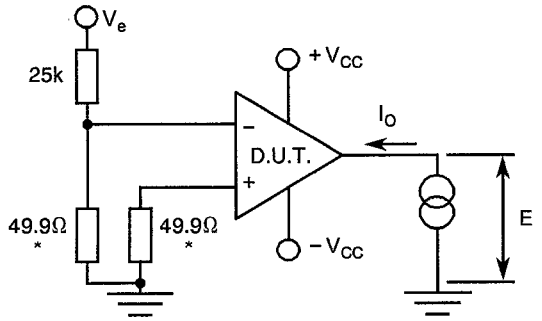
NOTES
1. $I_{OS} = (5000 - E)/5$.
2. Duration of test: 10ms maximum.
3. Balance and balance strobe inputs open.
4. Ground terminal is connected to ground.

APPENDIX 'A'

AGREED DEVIATIONS FOR THOMSON-CSF (F)

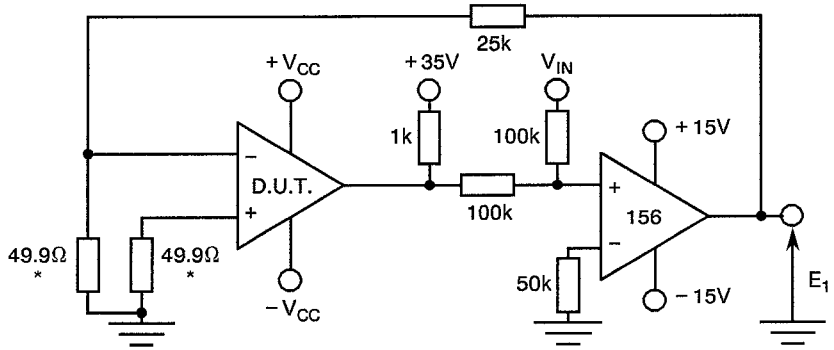
CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - SATURATION VOLTAGE



NOTES
1. $V_{OL} = E + 0.5V$.
2. Balance and balance strobe open.
3. Ground terminal connected to $-V_{CC}$.

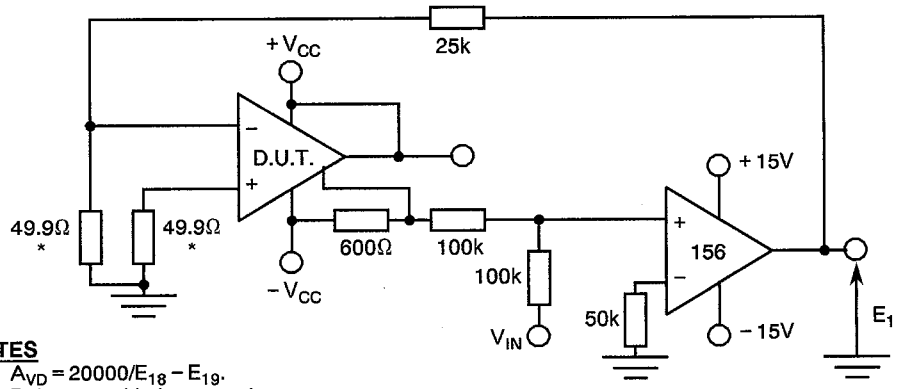
FIGURE 4(j) - DIFFERENTIAL MODE VOLTAGE GAIN (COLLECTOR OUTPUT)



NOTES
1. $A_{VD} = 40000/E_{16} - E_{17}$.
2. Balance and balance strobe open.
3. Ground terminal connected to $-V_{CC}$.

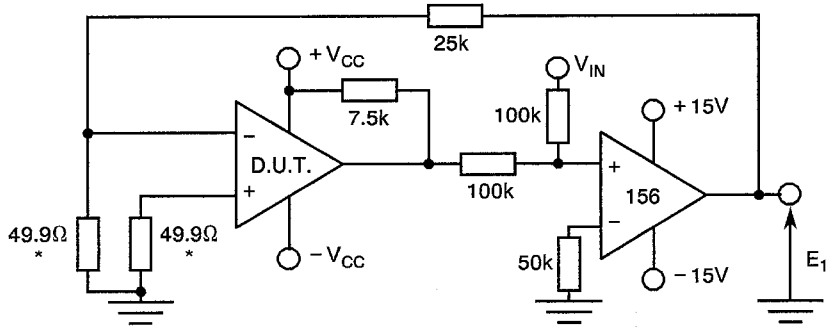
* These are 0.1% resistors matched to 0.01%. The tolerance for all other resistors is 1%.

FIGURE 4(k) - DIFFERENTIAL MODE VOLTAGE GAIN (EMITTER OUTPUT)



NOTES
1. $A_{VD} = 20000/E_{18} - E_{19}$.
2. Balance and balance strobe open.
3. Ground terminal connected to $-V_{CC}$ through a 600Ω resistor.

FIGURE 4(l) - COMMON MODE REJECTION RATIO



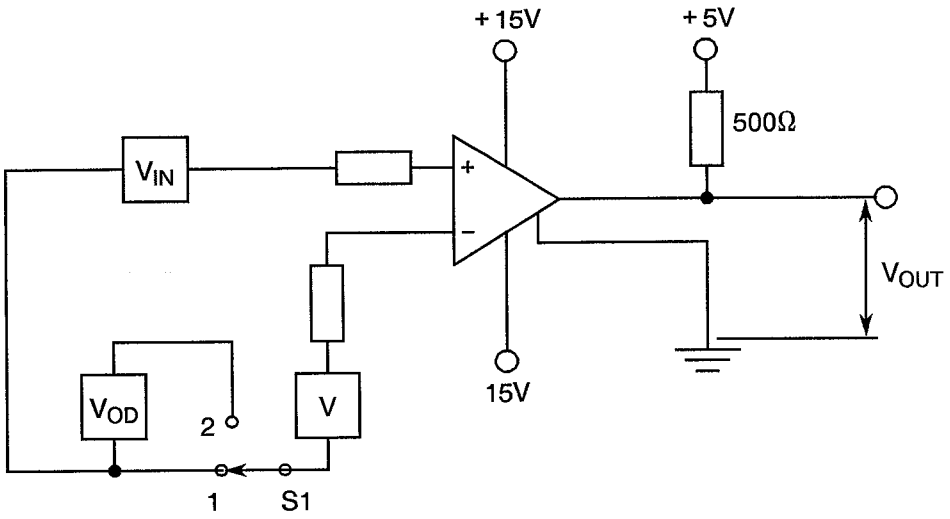
NOTES
1. CMRR = 20 log $\left| \frac{27.5 \times 10^6}{E_{20} - E_{21}} \right|$ (measure E_{20} and E_{21} to four place accuracy).
2. Balance and balance strobe open.
3. Ground terminal connected to $-V_{CC}$ through a 300Ω resistor.

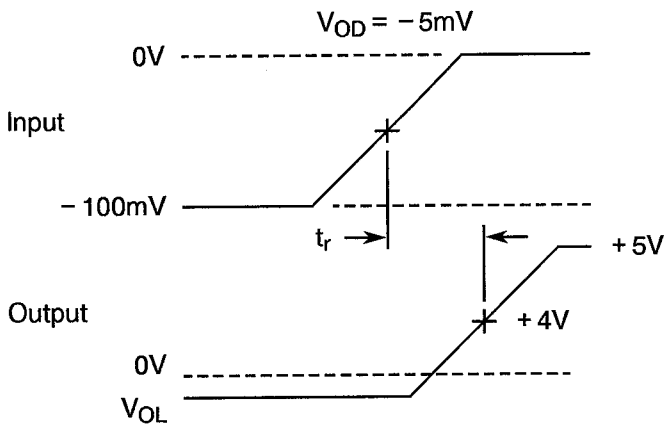
APPENDIX 'A'

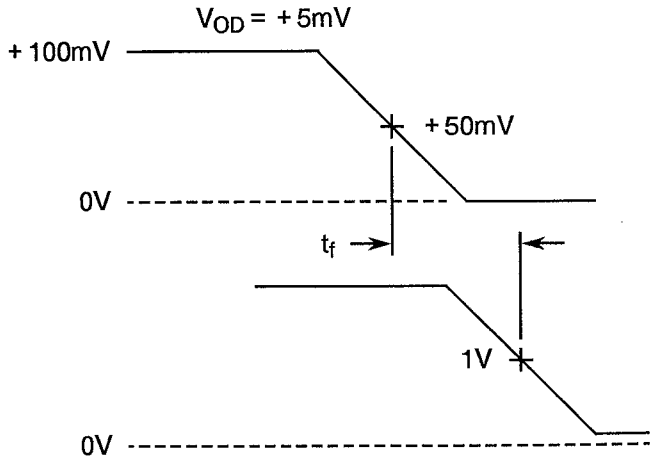
AGREED DEVIATIONS FOR THOMSON-CSF (F)

CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(m) - RESPONSE TIME







NOTES

1. V_{IN} = 10µs pulse width at 50kHz, t_{LH} and $t_{HL} \leq$ 10ns.
2. Set-up procedure:-
   A. With S1 in position 1, adjust V for V_{OUT} = 0.
   B. Adjust V_{OD} to −5mV for t_r or +5mV for t_f.
   C. Switch S1 to position 2.